Circuit Models for the Inductance of Eight-Terminal Decoupling Capacitors

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***Abstract*— The series inductance associated with decoupling capacitors can contribute significantly to the impedance of the power distribution network. The eight-terminal capacitors considered in this article have a lower self-inductance than two-terminal capacitors and are commonly used in IC packages. Manufacturers typically specify the inductance of the capacitor using some type of equivalent series inductance (ESL), but this ESL may not accurately predict the inductance seen during use because it does not account for the coupling between the capacitor and nearby structures like the return plane. To adequately determine the inductance associated with an eight-terminal capacitor, models of typical eight-terminal capacitors were developed in Dassault Systèmes CST Studio Suite. The partial element equivalent circuit (PEEC) method was used to construct simple models that can be simulated in SPICE. PEEC provides analytic insight into the source of inductance. Modeling the electrode stack as a solid block rather than a multilayer structure was shown to only change the computed inductance by 3% (∼1 pH) and to substantially reduce the compute time. CST and PEEC models agreed within 9% (∼3 pH), demonstrating the adequacy of the simpler PEEC models. Studies of the impact of the design parameters demonstrate that the distance between the capacitor and the reference plane has the greatest influence on inductance and that the placement of vias within the pads is important.**

***Index Terms*— Equivalent series inductance (ESI), multilayer ceramic capacitor, parasitic inductance, partial element equivalent circuit (PEEC) method, power distribution network (PDN).**

I. Introduction

DECOUPLING capacitors (decaps) are typically used to keep the impedance of the power distribution network (PDN) acceptably low in the package and printed circuit board (PCB) designs [1], [2]. These capacitors consequently reduce power supply noise and associated signal and/or power integrity issues [3], [4]. The PDN impedance is typically kept below a target impedance to ensure that voltage fluctuations on the PDN are smaller than an allowable limit [2], [5]. The PDN impedance is often specified to be in the milliohm range up to several gigahertz for high-performance designs [6], [7]. The ability to maintain this impedance to such high frequencies with on-PCB decoupling capacitors is limited by the high connection inductance that is inherent to mounting on a PCB. On-package decoupling capacitors, on the other hand, may also be used to reduce high-frequency noise up to several hundreds of megahertz.

The ability of decoupling capacitors to impact the PDN impedance at higher frequencies is limited by the series connection inductance to the power and return planes [8]–[10]. Eight-terminal capacitors have up to an 80% lower inductance than similar two-terminal capacitors [11], [12].

A good electrical model for a decoupling capacitor is a series *RLC* circuit, where R is the equivalent series resistance (ESR), L is inductance, and C is the capacitor's nominal value [6]. Manufacturers usually provide a single value for the capacitor's equivalent series inductance (ESL) [2], [13]. The values for ESL are based on measurements performed on a specific test fixture [12], [14], and can depend on the measurement fixture characteristics [2], [14], [15]. More complicated models are available for modeling capacitor behavior above the first *RLC* circuit resonance frequency [6], [16], [17]. None of these representations of inductance, however, take into account the layout and associated coupling to structures in the surrounding environment, such as the ground plane and pads. The actual inductance, however, is dependent on this coupling [5], [13], [18], [19].

Full-wave modeling of the complete connection geometry, including capacitor, traces, vias, return plane, etc., can accurately predict the connection inductance of the decoupling capacitors [16]. The partial element equivalent circuit (PEEC) method allows the development of full-wave models which can easily be incorporated into SPICE models of the rest of the PDN design [20]–[22]. This circuit approach gives insight into behavior as well as allowing the engineer to quickly make changes within the SPICE model to incorporate changes made to the actual layout.

Typical package design with a flip-chip IC and decoupling capacitor is shown in Fig. 1 [2], [9]. The decoupling

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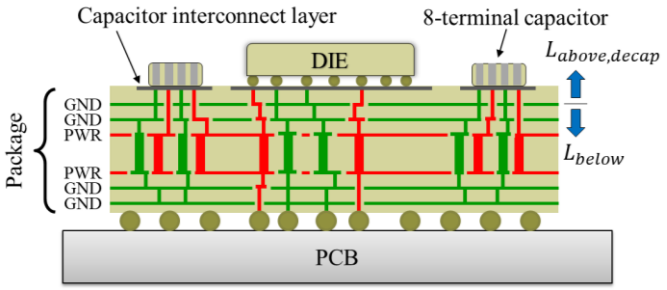


Fig. 1. Cross section of a typical PDN with decoupling capacitors [20].

capacitor is connected to the PDN through traces and vias. The connection to the topmost reference plane, usually a ground plane, is a good place to partition the inductance associated with the capacitor from the inductance associated with the package and PCB [5]. We call the inductance looking into the capacitor from the via antipads in the ground plane $L_{\text{above,decap}}$, as shown in Fig. 1. The total equivalent inductance of the PCB and package, L_{below}, is associated with the current loop below the partitioning ground plane through all the layers up to the IC [4]. These two inductances can be calculated separately, and the results combined after calculation to obtain the complete PDN impedance.

Models for the inductance of the eight-terminal capacitor and its connections to the power and the return plane are developed in this article. The model is developed first using a full representation of the electrode stack and then is simplified using a solid conductive block to represent the body of the capacitor, without significantly sacrificing model accuracy. A similar model is shown which uses the PEEC method [22] to create circuit-level models which can be simulated in a SPICE solver along with the rest of the PDN. This model is further simplified to develop analytical models for the inductance. These analytic models allow for a deeper understanding of how inductance changes with design. The impact of specific design parameters on $L_{\text{above,decap}}$ such as height above the return plane or via placement is then demonstrated using these models.

II. Structure Under Test

Eight-terminal capacitors minimize the connection inductance by reducing the size of the package, minimizing the distance between pins, and by alternating the power and return pins to maximize the influence of mutual inductance [11], [12]. Eight-terminal capacitors are manufactured by AVX, TDK, and Murata [12], [23], [24]. AVX and Murata use the same internal and terminal connections, but the internal connections used by TDK are different. The Murata LLA series capacitors are not evaluated here because of their similarity with the AVX capacitors. Eight-terminal capacitors by AVX and TDK are analyzed in Sections II-A–II-C.

A. AVX Eight-Terminal Capacitor

AVX makes interdigitated capacitor (IDC) [12], [25]. The internal architecture of this capacitor is shown in Fig. 2(a). The AVX IDC will be referred to as the "consolidated"

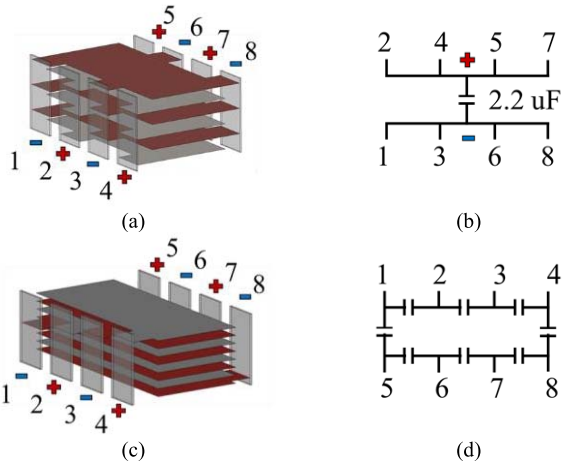


Fig. 2. (a) Internal structure and (b) equivalent circuit of AVX's IDC "consolidated" capacitor [12], [20]. (c) Internal structure and (d) equivalent circuit of TDK's CLL "divided" capacitor [20], [23].

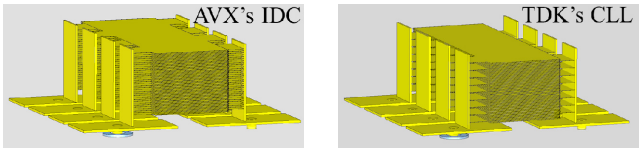
capacitor throughout the text, since all of the positive pins (pins 2, 4, 5, and 7) are connected together internally, as are all the return pins (pins 1, 3, 6, and 8). Effectively, there is a single capacitance between the positive pins (2, 4, 5, and 7) and negative pins (1, 3, 6, and 8) as shown in Fig. 2(b).

B. TDK Eight-Terminal Capacitor

TDK produces the CLL series eight-terminal multilayer ceramic capacitor [23]. Reduced inductance is achieved in a similar manner as the "consolidated" capacitor, but the capacitor pin configuration is different. The internal architecture of the capacitor is shown in Fig. 2(c). A corresponding equivalent circuit is shown in Fig. 2(d). The TDK CLL capacitor is made so that there is a unique capacitance between each set of neighboring pins. The TDK design will be referred to as the "divided" capacitor, since the pins are electrically isolated at dc. When used as a decoupling capacitor, however, pins 1, 3, 6, and 7 of the TDK CLL should be connected to one supply and pins 2, 4, 5, and 7 to the other [23]. Connected in this way, the divided and consolidated capacitors perform very similarly. If the TDK CLL capacitor is used to decouple more than one supply, so that the pins are connected differently, the overall inductance may be much larger than when properly connected to decouple a single supply. In this article, the TDK CLL capacitor is assumed to be used to decouple a single supply with the positive supply connected to pins 1, 3, 6, and 8 and the negative supply connected to pins 2, 4, 5, and 7, much like the consolidated capacitor.

C. Inductance Models

To study the inductance of the eight-terminal capacitor, detailed models of the consolidated and divided capacitors with pads and vias connecting to power planes were built in Dassault Systèmes CST Studio Suite, as shown in Fig. 3. To accurately determine the internal structure, examples of the AVX IDC and TDK CLL capacitors were cut, polished, and observed under a microscope, as shown in Fig. 4. The length and width of the electrode plates were measured from



(a) (b)

Fig. 3. Detailed 3-D models of (a) AVX IDC "consolidated" capacitor and (b) TDK CLL "divided" capacitor with interconnects [20].

Fig. 4. Cross section of the divided 0603 capacitor under a microscope with 5× magnification [20].

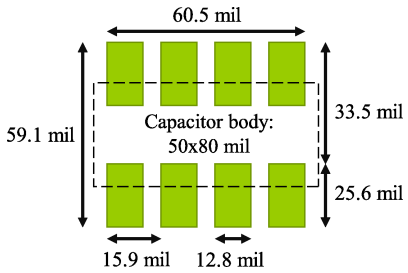


Fig. 5. Eight-terminal capacitor footprint [23], [25].

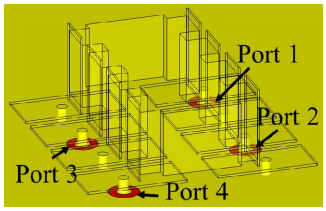


Fig. 6. Port defined between power vias and top ground plane.

the cut-capacitors, as was the number of plates and the closest distance between the electrode and the outside of the capacitor. The size of the plates and the distance between the inner plate and the outer shape boundary are critical parameters for determining the capacitor model inductance. The individual 0603 capacitors studied here had over 100 plates to achieve a large value of capacitance. The average plate thickness was 0.05 mil and the distance between the plates was 0.1 mil. To avoid long compute times due to the high dielectric constants (>1000), discrete capacitors were placed between the layers during the initial simulations. The dimensions of the eight-terminal capacitor footprint [23], [25] are shown in Fig. 5.

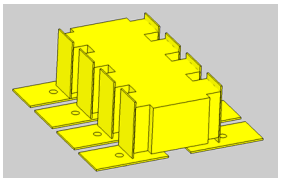
Inductance was calculated among all power pins from the simulation model. Ports were placed across the antipad, at the point each power via penetrated the reference plane, as shown in Fig. 6. There are four power and ground pins, the overall capacitor inductance can be characterized by a four-by-four inductance matrix.

The inductance matrices obtained from CST simulations for the detailed models of the AVX IDC and TDK CLL capacitors

$$\begin{bmatrix} 130 & 8 & 11 & 4 \\ 8 & 99 & 7 & 11 \\ 11 & 7 & 99 & 8 \\ 4 & 11 & 8 & 130 \end{bmatrix} pH \qquad \begin{bmatrix} 133 & 9 & 11 & 4 \\ 9 & 102 & 7 & 11 \\ 11 & 7 & 101 & 9 \\ 4 & 11 & 9 & 132 \end{bmatrix} pH$$

(a) (b)

Fig. 7. Inductance matrix calculated for (a) AVX IDC consolidated capacitor and (b) TDK CLL divided capacitor.



(a)

$$\begin{bmatrix} 133 & 8 & 12 & 4 \\ 8 & 100 & 7 & 12 \\ 12 & 7 & 100 & 8 \\ 4 & 12 & 8 & 133 \end{bmatrix} pH$$

(b)

Fig. 8. (a) 3-D model and (b) inductance matrix associated with the capacitor when electrodes are represented as a solid block.

are shown in Fig. 7. These inductance matrices are calculated at the point where the power via passes through the return plane, and includes the traces, pads, vias, and the capacitor package. The inductance matrix was extracted at 100 MHz.

Modeling all the electrode layers of the capacitor requires significant computational resources and large compute times. The dense multilayer geometry could be approximated as a solid conducting block for inductance calculations [20]. At the frequencies of interest, the conductive block approximation is valid since the current flows in the same direction through all the electrode plates and the plates are close together, so the total flux between the plates is small. This approximation can be applied to both the AVX IDC consolidated and TDK CLL divided capacitors. The inductance matrix found using this approximation is shown in Fig. 8. Approximating the capacitor body with a conductive block results in a maximum 3-pH difference in matrix elements compared to the detailed capacitor models with multilayer electrodes. The approximation of the electrodes as a solid conductive block maintains sufficient accuracy in the estimated inductance and substantially reduces the computational time.

The overall inductance associated with a decoupling capacitor can be approximated with a single value, $L_{\text{above,decap}}$, rather than using a matrix [15]. The relation between the inductance matrix, the port voltage, and the port current is given by

$$j2\pi f \cdot \begin{bmatrix} L_{11} & L_{12} & L_{13} & L_{14} \\ L_{21} & L_{22} & L_{23} & L_{24} \\ L_{31} & L_{32} & L_{33} & L_{34} \\ L_{41} & L_{42} & L_{43} & L_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \quad (1)$$

where f is frequency, and I_n and V_n are the current and voltage at the nth port. A single value for inductance can be found from this relationship by assuming all ports are at the same voltage (i.e., the capacitor being used for decoupling and is electrically small), that the current through the single equivalent inductance is equal to the sum of currents through each port [20]

$$I = I_1 + I_2 + I_3 + I_4 \quad (2)$$

$$V = V_1 = V_2 = V_3 = V_4 \quad (3)$$

TABLE I
ESTIMATED VALUES FOR $L_{\text{above,decap}}$

Solver	Model	Inductance
CST	Detailed AVX IDC model (Fig. 3a)	35.2 pH
CST	Detailed TDK CLL model (Fig. 3b)	36.0 pH
CST	A solid block approximation (Fig. 8)	35.1 pH
PEEC	AVX IDC capacitor (Fig. 10 and Fig. 11a)	32.0 pH
PEEC	TDK CLL capacitor (Fig. 10 and Fig. 11b)	33.2 pH
PEEC	Simplified inductance circuit (Fig. 12a)	31.4 pH

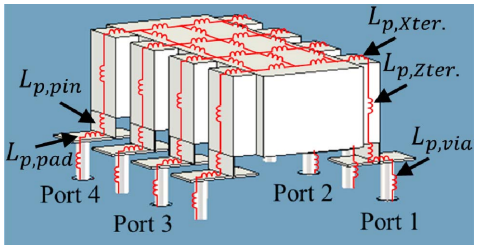


Fig. 9. Eight-terminal capacitor with a layout subdivided into simple geometrical objects with the corresponding PEEC.

and using the relation

$$j2\pi f L_{\text{above,decap}} = \frac{V}{I}. \tag{4}$$

The relationship in (3) assumes the voltages at all four ports are the same, which is not necessarily true in practical PDN designs. From PEEC modeling, it is impossible to connect the four pins without adding inductances between the contacts. Hence, the combined result in (4) is a lower bound for the total inductance associated with the decoupling capacitor above the plane. While (1) is more accurate, this single value is useful for approximating inductance and evaluating the relative behavior of designs.

The inductance matrices shown in Figs. 7 and 8(b) were converted into a single value for inductance, $L_{\text{above,decap}}$, using (4), and these values are listed in Table I. The difference between the capacitor approximated as a solid conductive block and the multilayer detailed capacitor models are about 3% (~1 pH). The results in Table I will be further considered in Section III when discussing the PEEC models of the capacitors.

III. PEEC EQUIVALENT CIRCUIT MODEL

The capacitor and its connections to the reference plane were modeled using the PEEC method to obtain an equivalent circuit representation for its inductance. Partial inductances for each portion of the design were found using analytical formulas available in the literature [19], [21]. The solid conductive block representing the capacitor body was meshed using rectangular partial inductances as indicated in Fig. 9. The pads and pins were represented with similar elements. The vias were modeled with an approximate partial inductance [20], [22]. To model the important impact of the ground-plane, we used an image solution. The simplified model for the geometry at hand is shown in Fig. 9 and the equivalent circuit

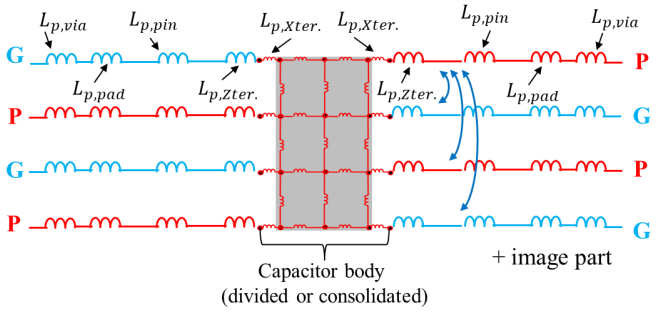


Fig. 10. Equivalent circuit model for partial inductance of eight-terminal capacitor and its connections to PDN developed using PEEC.

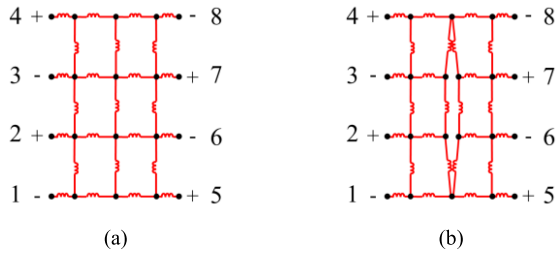


Fig. 11. PEEC inductance circuit models of the internal structures of (a) AVX IDC consolidated capacitor and (b) TDK CLL divided capacitor, corresponding to the circuit models shown in Fig. 2(b) and (d).

is shown in Fig. 10. The partial self- and mutual inductances for the simple geometrical cells are given in [22]. Values for finite or zero thickness rectangular prism objects were found using (C.8), (C.15), (C.26), (C.36), and (C.40) in [22].

The capacitor body was modeled using vertical and horizontal mesh cells. The mesh used for the consolidated and the divided capacitors was different since the connections to their internal electrodes are different. Fig. 10 shows the PEEC inductance circuit for a consolidated capacitor. The inductance mesh representing the body is shown in Fig. 11(a). The structure allows current to flow from one pin to any other through the capacitor electrodes which are "shorted" at high frequency. Since the current can only flow to neighboring pins in TDK's divided capacitor [see Fig. 2(d)], the mesh structure reflects this restriction as shown in Fig. 11(b).

The partial self-inductance representing the vias is referred to as $L_{p,\text{via}}$. All eight vias have the same partial self-inductance since the geometry is the same. The partial self-inductance of the pads, $L_{p,\text{pad}}$, is described using zero-thickness rectangular sheets. The partial self-inductance of the vertical pin that connects the capacitor's electrode to the pad, $L_{p,\text{pin}}$, is also described using a zero-thickness rectangular sheet. The current flowing vertically through the terminal that connects the capacitor pin to the electrodes is represented with partial self-inductance, $L_{p,\text{Zter.}}$. The terminal current reduces linearly with height as the current flows from the terminal into (or out of) the electrodes. It can be shown by integrating current over the height of the pin that the impact of the changing current can be accounted for by representing the terminal inductance as one half the partial self- or mutual inductance of a conductor of the size as the full terminal. The inductance associated with currents that flow horizontally

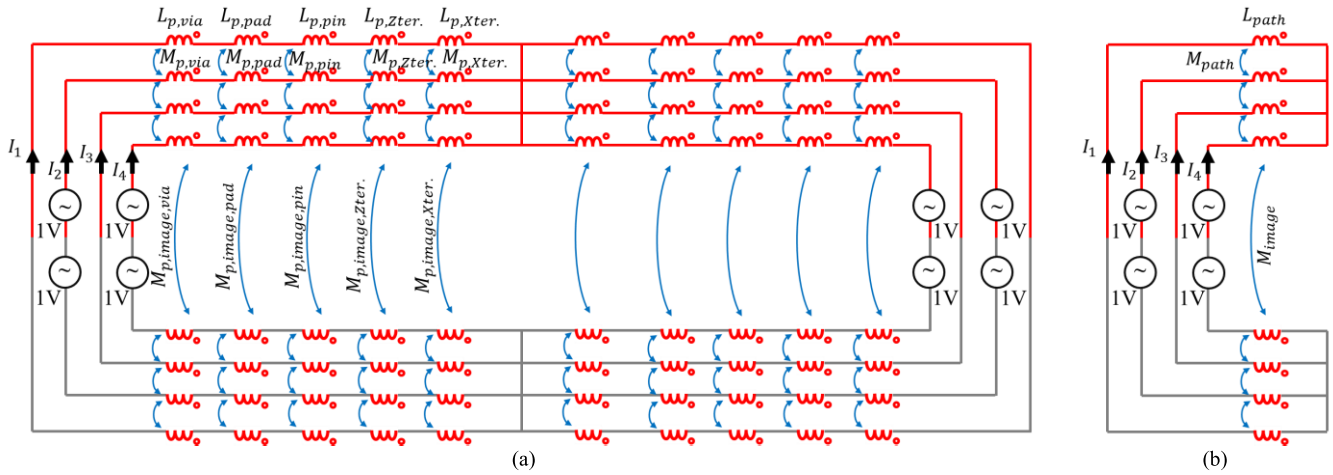


Fig. 12. (a) Simplified inductance circuit including partial self-inductance of the vias, pads, pins, and terminals of the capacitor electrodes and including the partial mutual inductances between the neighboring elements. (b) Left side of the circuit, which is symmetrical to the right side of the circuit in Fig. 12(a).

from the terminal into the electrodes is represented with partial inductance $L_{p,\text{Xter.}}$.

Partial mutual inductances were included between parallel structures (i.e., between vertical and horizontal terminals, $M_{p,\text{Zter.}}$ and $M_{p,\text{Xter.}}$, between pins, $M_{p,\text{pin}}$, between pads, $M_{p,\text{pad}}$, and between vias, $M_{p,\text{via}}$). Partial mutual terms between perpendicular inductances are equal to zero as they do not couple.

The reference plane was accounted for using an image of the capacitor and its connections in the return plane. The concept is illustrated in Fig. 12(a) for a simplified version of the circuit. The "sources," as well as the capacitor and its connections, were mirrored in the image. Including mutual coupling between the original circuit and its image is critical to accurately describe the total inductance of the structure. The inductance matrix describing the PEEC model has 104 partial self-inductances. The inductance circuit was solved using modified nodal analysis (MNA) [22]. Circuit construction and calculation take less than a minute.

Table I shows values for $L_{\text{above,decap}}$ found using PEEC and using CST for the consolidated and divided capacitors. The values for $L_{\text{above,decap}}$ found using PEEC and CST differ by 3.1 pH (8.8%) or less. The values for $L_{\text{above,decap}}$ found using PEEC for the TDK and AVX capacitors differ by 1.2 pH, which is also consistent with the CST simulations (see Fig. 7). The close correlation between the PEEC and CST results gives confidence in the results from both models.

A. Analytical PEEC Solution

The PEEC can be further simplified to obtain an analytical approximation for the overall inductance of the capacitor. An analytical equation allows a better understanding of the main contributors to the inductance and allows $L_{\text{above,decap}}$ to be quickly approximated for different designs. A simplified model of the PEEC inductance circuit is shown in Fig. 12(a). The part of the mesh representing the capacitor, that is marked with a gray rectangle in Fig. 10, could be ignored because the magnetic flux surrounding the body is close to zero when accounting for the nearly equal and opposite currents flowing through it (e.g., from V_{dd} down to V_{ss} on one side and from V_{dd} up to V_{ss} on the other). The model was derived by combining the series inductances in Fig. 9, ignoring part of the mesh, and accounting for only the mutual inductance between neighboring objects and with the return plane. Due to the symmetry of the circuit in Fig. 12(a), the right and left sides of the circuit can be combined as shown in Fig. 12(b) to solve for $L_{\text{above,decap}}$. The inductance L_{path} in Fig. 12(b) is given by

$$L_{\text{path}} = L_{p,\text{via}} + L_{p,\text{pad}} + L_{p,\text{pin}} + L_{p,\text{Zter.}} + L_{p,\text{Xter.}} \quad (5)$$

M_{path} and M_{image} are similarly given by

$$M_{\text{path}} = M_{p,\text{via}} + M_{p,\text{pad}} + M_{p,\text{pin}} + M_{p,\text{Zter.}} + M_{p,\text{Xter.}} \quad (6)$$

$$M_{\text{image}} = M_{p,\text{image,via}} + M_{p,\text{image,pad}} + M_{p,\text{image,pin}} + M_{p,\text{image,Zter.}} + M_{p,\text{image,Xter.}} \quad (7)$$

The circuit in Fig. 12(b) can be further simplified as shown in Fig. 13, where the self- and mutual inductances are given by

$$L = 2(L_{\text{path}} + M_{\text{image}}) \quad (8)$$

$$M = 2M_{\text{path.}} \quad (9)$$

The overall inductance, $L_{\text{above,decap}}$, is then given by

$$L_{\text{above,decap}} = \frac{L^2 - LM - M^2}{2L + M}. \quad (10)$$

Equation (10) is calculated from 15 partial self- and mutual inductances. Equations for each element are given in [22] (equations C.8, C.15, C.26, C.36, and C.40). Values for each element were calculated and are shown in Table II. Using these values in (10) gives a value of $L_{\text{above,decap}}$ of 31.4 pH. This value is 0.6 pH smaller than the inductance of the consolidated capacitor calculated by the complete PEEC model due to ignoring the inductance of the capacitor body and the mutual inductance to structures farther away than the neighboring pins. The individual values of inductance in Table II illustrate the importance of each structure to the overall inductance. The partial self-inductance of the terminal, $L_{p,\text{Zter}}$, is nearly as large as all other contributions combined.

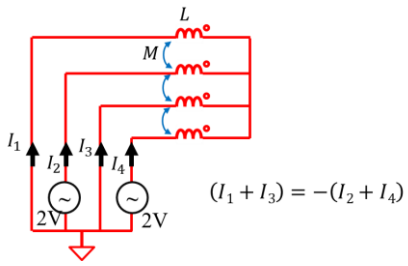


Fig. 13. Simplified circuit to solve for $L_{\text{above,decap}}$ inductance.

TABLE II
CIRCUIT INDUCTANCES FOR SIMPLIFIED CIRCUIT IN FIG. 12(A) IN pH

$L_{p,via}$	14.1	$M_{p,via}$	-0.2	$M_{p,image,via}$	4.6
$L_{p,pad}$	10.0	$M_{p,pad}$	-1.4	$M_{p,image,pad}$	2.8
$L_{p,pin}$	4.7	$M_{p,pin}$	-0.6	$M_{p,image,pin}$	0.9
$L_{p,Zter.}$	40.3	$M_{p,Zter.}$	-11.6	$M_{p,image,Zter.}$	8.9
$L_{p,Xter.}$	13.9	$M_{p,Xter.}$	-5.0	$M_{p,image,Xter.}$	2.8

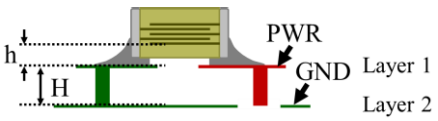


Fig. 14. Geometry of the mounted eight-terminal capacitor.

IV. INFLUENCE OF LAYOUT

The height of the capacitor above the return plane, the placement of vias, and the use of connecting traces can have a significant impact on the overall value of $L_{\text{above,decap}}$. Design curves for $L_{\text{above,decap}}$ for different layouts or manufacturing variations are shown in Section V. Importantly, the distance between pads and ground plane will change for different PCB designs as shown in Fig. 14. The distance between the pads and the closest electrode also varies due to the capacitor mounting process. The distance between the reference plane and the pads (H), and distance from the pads to the closest internal capacitor plate (h) are shown in Fig. 14. The dependence of $L_{\text{above,decap}}$ on the parameters, H and h are shown in Fig. 15(a) and (b), respectively. According to Fig. 15, the value of $L_{\text{above,decap}}$ will not exceed 78 pH if the thickness of the dielectric (H) is less than 10 mil. The distance between the pad and the first electrode plate may change the inductance by up to 10 pH for values of h from 1 to 5 mil. This height may vary depending on the thickness of the solder.

The value of $L_{\text{above,decap}}$ is also impacted by the design of the via connections. Intuitively, the closer the vias are to the capacitor electrodes the smaller the inductance. The distance, D, between the vias and capacitor terminals was varied from 2.77 to 12.77 mil as shown in Fig. 16(a). The resulting change in $L_{\text{above,decap}}$ is shown in Fig. 17(a). $L_{\text{above,decap}}$ changed by up to 10 pH when $h = 1.75$ mil and $H = 3$ mil.

The impact of not centering the capacitor on its footprint was also investigated as shown in Fig. 16(b). During the soldering process, a mounted capacitor might shift by S mil as indicated by the capacitor outlined in Fig. 16(b). As shown in Fig. 17(b), the impact of the capacitor position

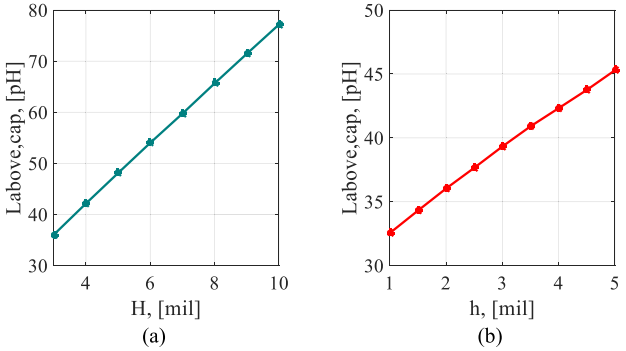


Fig. 15. Dependence of the overall capacitor inductance on (a) height, H, between the ground plane and pads, when $h = 2$ mil and (b) height, h, between the pads and capacitor's closest electrode, when $H = 3$ mil.

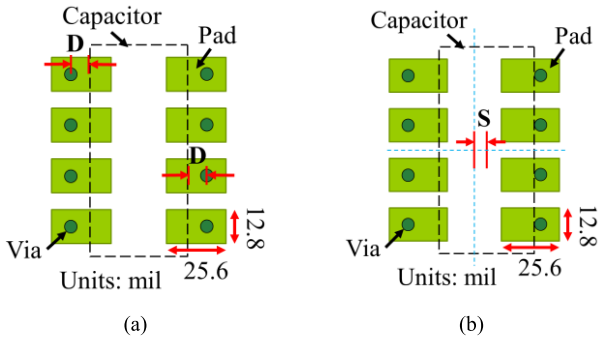


Fig. 16. (a) Distance, D, between center of the vias and the capacitor. (b) Mounted capacitor shifted a distance S from the footprint center.

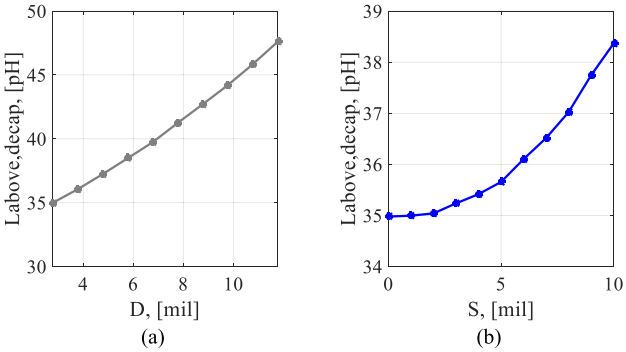


Fig. 17. Effect on $L_{\text{above,decap}}$ of (a) changing the distance D between the vias and the capacitor body and (b) shifting center of the capacitor by a distance S the footprint center, when $h = 1.75$ mil and $H = 3$ mil.

was relatively small compared to other parameters, up to 3 pH for the configuration studied here.

Maintaining a small value of $L_{\text{above,decap}}$ depends on the symmetry of currents between neighboring pins, as is suggested by the relatively large value of M_{path} shown in Table II (18.8 pH). Changes to the layout which impact this symmetry can increase the overall inductance associated with the capacitor. Asymmetry can be introduced by shifting even one of the via connections. For example, the via connecting to pin 3 was moved by 6.7 mil as shown in Fig. 18(a). The asymmetry introduced by moving this one via increased the $L_{\text{above,decap}}$ value by 3.9 pH (11.1%). Shifting all of the vias as shown

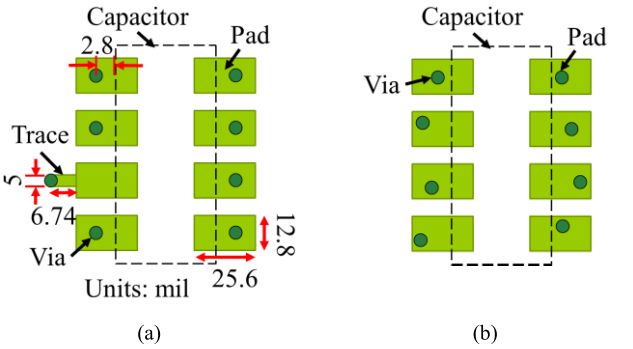


Fig. 18. Impact of asymmetries in layout. (a) Layout with an additional trace connecting via and pad. (b) Vias connecting pads to the planes are randomly placed.

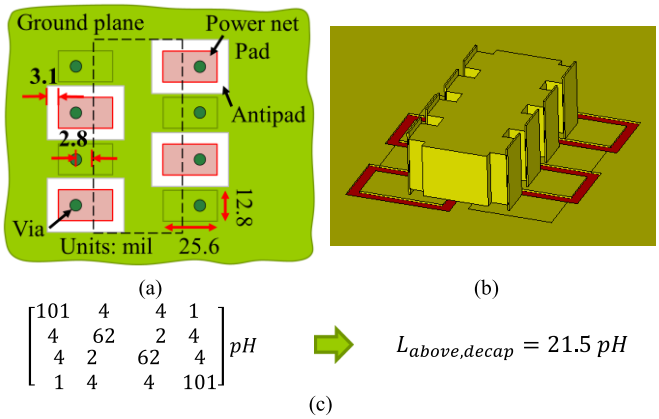


Fig. 19. (a) Footprint and (b) 3-D model of the layout design with a ground plane placed on the first layer of the package or PCB. (c) Four-by-four inductance matrix converted to a single-value inductance.

in Fig. 18(b) will have a larger impact. To study this effect, the values of $L_{\text{above,decap}}$ were modeled for five different sets of randomly placed vias. The resulting inductance varied between 32 and 42 pH when $h = 1.75$ mil and $H = 3$ mil, or by about 10 pH (31%).

As a final study, the case where the capacitor is directly mounted on the ground and power pads was considered. This reduces the distance $H = 0$. An example of such a design is shown in Fig. 19. In this case, the closest distance between the capacitor electrodes and the reference plane is $h = 1.75$ mil. To ensure that the loop created by the capacitor body and the reference plane is not coupled with the internal layers of the package, the antipad between the power pads and the ground plane should not exceed 3.1 mil [23]. The inductance for the eight-terminal capacitor design shown in Fig. 19 was calculated to be 21.5 pH. The inductance matrix is also given in Fig. 19(c) for this case. As expected, the values of inductance are significantly smaller for this direct connection than for the conventional connections shown in Fig. 7.

V. Conclusion

Models were developed to analyze the inductance associated with an eight-terminal decoupling capacitor mounted on a package or PCB. While a single value of inductance was used to evaluate the accuracy of the models and to compare layout configurations, the inductance associated with the capacitor should be characterized using a four-by-four inductance matrix in most practical applications. A single value for inductance is given based on an assumption that the voltages at all ports are the same, or effectively that the inductance between the connections below the plane is zero.

Comparing models which included all electrode plates to one where the electrode plate stack was replaced by a solid conductor block showed that using the solid block model substantially reduced the time and effort required to model the inductance while having minimal impact on accuracy. The solid conductive block produced values of inductance within 3% of those found using the complete electrode model. Inductance models developed in CST and PEEC were within 9% of one another. The PEEC models have the advantage that they naturally give a circuit-level description of parasitic effects that can be directly incorporated into SPICE simulations of the overall PDN. By simplifying the PEEC model, a closed-form approximation for the overall inductance was developed that can be used to obtain better insight into the major causes of inductance and how design changes will influence the inductance. This closed-form approximation returned values of inductance within 0.5 pH (2%) of the more complete PEEC model. The simplified PEEC model demonstrated that the partial self-inductance of the terminal, $L_{p,\text{Zter}}$, had a substantial impact on the overall inductance.

Studies of the impact of different capacitor connections and manufacturing variations on the inductance showed that the distance to the return plane has the greatest impact on inductance. The total inductance of the mounted eight-terminal capacitor varies between 35 and 50 pH if the dielectric thickness between the capacitor and the reference plane varies from 3 to 5 mil. The position of vias within the pads, however, was not insignificant, resulting in a change in inductance as much as 10 pH. The influence of solder height becomes particularly important when the capacitor is mounted directly on the reference plane.

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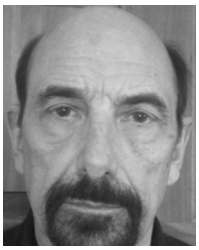

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