Commercial USB IC Soft-Failure Sensitivity Measurement Method and Trend Analysis

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***Abstract*—An electrostatic discharge (ESD) happening on a commercial electronic device such as at the USB interface can induce soft-failure in the IC and disturb the normal operation of the device. This paper investigates the soft-failure behaviors of 14 commercial USB devices in order to obtain an insight into the overall sensitivity trend of such systems and into the severity of different soft-failures. A new analysis method is proposed in this paper. The considered parameters in this study include: injected pulse widths, pulse rise time, current levels, USB standard of the DUTs, etc. Soft-failures started to occur at a current of around 1 A, and nearly all configurations would show errors above 6 A.**

Keywords— electrostatic discharge, soft-failure, USB IC susceptibility

I. INTRODUCTION

Commercial electronic devices may occasionally suffer from soft-failures or hard-failures caused by transient events such as electrostatic discharges (ESD). Soft failures are recoverable by a power cycle process and will not leave permanent hardware damage. USB is one of the most widely used interface, and USB ICs are commonly installed in the commercial electronic devices. An ESD event on an active USB link can corrupt the data stream and/or the link, which are observed by the users as sudden interruption of normal device operations and possibly the dismounting of the device. The observed errors are listed in TABLE I, which include bit errors that can be corrected by the computer software and are not recorded by our observation, soft-failures with popped-out error messages that give user some information about the interrupted operations, and hardware damage which cannot be recovered by rebooting the system. The interest of this study is in the second type of failures: soft-failures, for which the users can observe the errors during the operations, but the device does not suffer from hardware damage.

TABLE I. OBSERVED ERRORS DURING TESTING

Failure Types	Observed by Users
Software-corrected errors	Transfer speed drop/burst
Soft-failures	Error: "not enough memory"
	Error: "could not find this item"
	Error: "an error has occurred"
	…
Hard-failures	Client device cannot be recognized by the computer anymore

ESD induced noise can result from direct discharges to PINs or the connector shell, from inserting a charged cable (plug-in event), from discharges to USB connected devices, or from discharges to the other parts of the system. These events can cause soft-failures. However, the plug-in event is not considered in this study, as there cannot be any data traffic the moment when the USB cable is inserted [1]. The worst disturbance occurs during the discharge to a USB connected device when there is active data communication.

The IC susceptibility to ESD can also vary under different operating conditions [2]. Under certain test conditions, the VDD core voltage, CPU loading, and PDN impedance and noise margin can have somewhat a direct effect on the IC sensitivity against coupled ESD stress.

This work provides an overview on the typical robustness of market sampled USB connected devices. The overview of the malfunction trend developed based on the general sensitivity levels will guide the IC designers to estimate the overall system susceptibility, and may help to anticipate the sensitivity of coming USB standards. A methodology is introduced for how to systematically and customly perform the soft-failure characterization on the commercial USB connected devices. Because ESD-induced noise pulse shape and other characteristics will vary based on the coupling path from the ESD discharge point to the affected net, different pulse widths and rise times are considered in this study to take this variation into account. Also several new designs and techniques to customize and generalize the measurement will be briefly

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introduced. Section II introduces the methodology of the USB IC sensitivity characterization, whereas section III discusses the testing results overview and parameter factors, followed by the conclusion in section IV

II. Methodology

A. Soft-failure Testing Overall Structure

To provide an overview on the robustness of commercial USB interfaces under ESD stress multiple ICs have been characterized. Similar to IEC 61000-4-2 testing, only the user observable errors have been considered. Deep error analysis into the protocol involving monitoring the USB registry, using a USB protocol analyzer, or other methods into the system [3] is not within the scope of this study. As the user-observed failures are more related to the general practice of IEC 61000-4-2 testing, an overview on the USB IC sensitivity in the current market was investigated instead of root cause analysis [4] of a much smaller number of devices.

The overall soft-failure analysis test setup is illustrated in Fig. 1. The test consists of ESD stress injection, isolation of the USB client device from the stress, measurement technique to characterize the current flowing into the I/O pin of the IC, and monitoring and determining when a soft-failure is observed by the user. During an ESD injection, current was directly injected onto the USB data trace, and the USB client device was protected by the isolation structure to ensure that the disturbance happened inside the device under test (DUT) USB IC. Meanwhile the operation continuity and soft-failure error message occurrence was monitored on the PC screen, and the current injected into the DUT IC pin was measured whenever a soft-failure occurred.

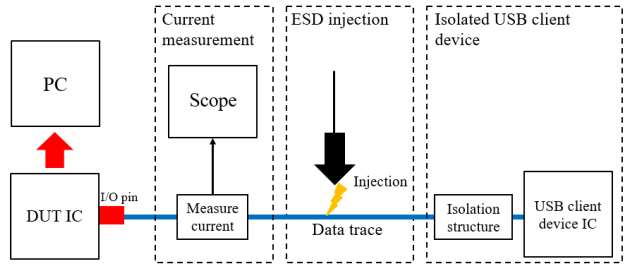

Fig. 1. Test setup overview.

B. ESD Stress Injection

A discharge to a USB connected device can couple noise onto the data lines. The amount of noise coupled depends on the shield quality. In [1] it was pointed out that a large portion of market sampled USB 2.0 cables had no shield. The actual noise waveform in the data lines will depend on the discharge point, discharging object, cable shield and connector mounting. To reduce the complexity, the IC characterization was performed by injecting directly into the data lines. To take the variability of the coupled noise pulses into account, pulses of three pulse widths (2 ns wide, 4 ns wide and 5 ns wide) have been used.

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The injection was performed directly on the USB data traces via a resistor, a capacitor or a transient voltage suppressor (TVS) during the data communication process using a transmission line pulser (TLP) as source. Over an ESD generator, the TLP offers the advantage of providing a well-defined pulse and it avoids additional transient field coupling.

C. Isolation Method

A USB link involves an IC at the either end. The USB client device needs to be isolated from the injected ESD stress in order to characterize the behavior of the DUT IC. An isolation structure was used on the data trace to reduce the current flowing to the USB client IC.

For links with unidirectional data stream during device communication such as for USB 3.0 standard and above, the isolation structure shown in Fig. 2 was used to greatly reduce the current flowing into the protected side (USB client IC). The isolation structure consists of two attenuations and an amplifier in between to reach 0 dB gain in one direction and over 30 dB attenuation in the other direction. More specifically, in the direction of the data traffic, the signal was normally transmitted without amplification or attenuation, while the in the opposite direction in which the noise current was injected, the injected current was significantly suppressed to protect the USB client device.

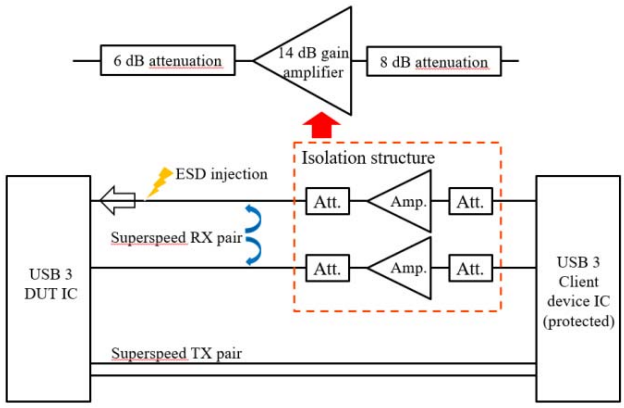

Fig. 2. Isolation structure outline.

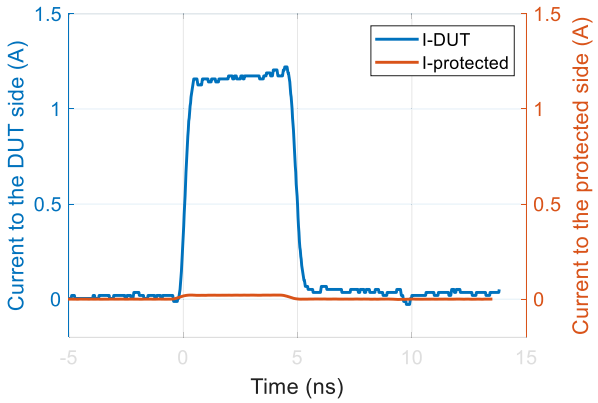

Fig. 3. Current waveform measured at both sides of the isolation structure.

For traces with bidirectional data stream such as those used in USB 1.1 and USB 2.0 standards, the isolation structure discussed above cannot be used, because the structure blocks signal transmission in one direction and thus disturbs normal data communication of these devices. In such cases a 25 Ω isolation resistor was mounted on the trace to offer some suppression of the current flowing into the USB client IC, while maintaining normal device recognition and operation.

D. *Current Measurement Technique*

The injected current level seen at the I/O pin of the IC can be used as a metric to see how much current the IC can tolerate before going under a soft-failure. The higher current level the IC can endure, the higher robustness is expected of the IC. Thus a method to measure the current flowing on the data trace to the IC pin is required to characterize the susceptibility of the IC.

However, measuring this current very close to the IC without disturbing the data traffic is challenging. The conventional methods of using an H-field probe to pick up the magnetic field above the trace or using a current probe to measure the current have the following disadvantages:

- The H-field probe sensitivity increases with frequency. To obtain the original current waveform shape and level, a deconvolution process is required.
- The H-field coupling is dependent on the probe-to-trace geometry. The width of the trace under test and how the probe is rotated or tilted can have nonnegligible effects on the measured results.
- Using a current probe such as a CT-1 or CT-6 probe introduces unwanted inductances which will influence the data traffic, especially in USB 3.0 links.

To overcome such disadvantages, a probe was designed that could be placed onto a trace at a location where a zero ohm chip resistor could be used. For that reason the probe was named "zero-ohm substitution probe". The probe also utilizes the concept of H-field coupling, but has a fixed coupling structure to eliminate influences from the probe-to-trace geometry. To use the probe for current measurement, the trace needs to be cut and the probe was mounted across the cut. The trace current was diverted into the probe and its magnetic field coupling structure provides an output to the oscilloscope, as illustrated in Fig. 4. The output from the probe is not dependent on the probe-to-trace geometry, as its internal coupling structure is fixed by design. The probe trace has almost 0 Ω impedance up to 10 GHz and does not affect signal quality or the eye diagram.

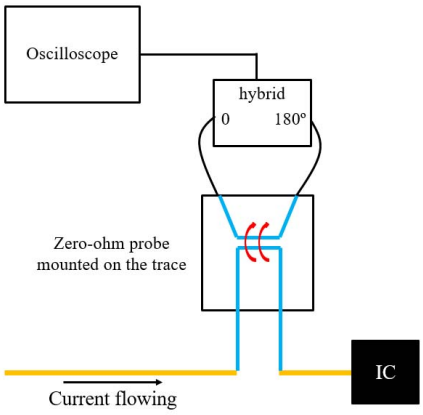

Fig. 4. Sketch describing the use of the zero-ohm substitution probe to measure the current flow.

E. *Soft-failure Testing*

The testing to characterize soft-failures for the commercial USB devices was systematically performed. The DUTs were selected to be common USB connected devices found on the market which allowed simple data communication operations such as file copying. As suitable candidates, commercial USB hubs under USB standard 1.1, 2.0 and 3.0 containing USB ICs were used as DUTs in this study. The DUTs were connected to the PC, and a USB 3.0 flash drive was used as the client device to transfer data through the DUT and to the PC. The soft-failure characterization was performed on the USB link between the DUT and the client device, while the client device was protected by the isolation structure such that the DUT IC was the primary target of failures.

The test method followed the following protocol: the TLP source voltage was started at 50 V, and was increased in increments of 10 V at each step. At every injected current level, 3 groups of ESD injections were performed and each group contained approximately 100 injections. The failure condition such as whether a failure occurred and the error type was recorded at each current level.

The injected pulse parameters were varied to investigate the factors in the IC sensitivity. Considered parameters in this study include pulse width and rise time.

F. *Extraction of Soft-failure Thresholds*

The failure condition of each DUT with different parameters was summarized into a table for the failure threshold extraction. TABLE II shows an example of the summarized failure condition of one DUT. The varied parameters were the injected pulse width and the rise time of the pulse. Under each test condition, the number of failures out of the 3 rounds and the error type were recorded at each injection level. If more than 2 failures out of 3 rounds occurred at an injection level, the DUT was determined to have a high probability to endure a soft-failure at this injection level or higher, and the failure threshold was found under such test condition. The current waveform at the IC I/O pin was captured when the failure occurred and the

peak current level was recorded as the failure threshold indicator.

When a soft-failure occurred, the error message was noted down and the failures with the same message were categorized as one "failure type". The number of occurrence of each failure type, for example "Failure type 1 (F1)", was recorded out of the 3 rounds of testing at each level.

TABLE II. OBSERVED ERRORS DURING TESTING

VTLP (V)	*300 ps rise time*			*900 ps rise time*		
	2 ns PW	***4 ns PW***	***5 ns PW***	***2 ns PW***	***4 ns PW***	***5 ns PW***
80~150	0 Fail	0 Fail	0 Fail	0 Fail	0 Fail	0 Fail
160	0 Fail	0 Fail	F4 (3/3)	0 Fail	0 Fail	F4 (3/3)
170	0 Fail	0 Fail	F4 (3/3)	0 Fail	0 Fail	F4 (3/3)
180	0 Fail	F4 (1/3)		0 Fail	0 Fail	
190	0 Fail	F2 (3/3)		0 Fail	0 Fail	
200	0 Fail	F2 (3/3)		0 Fail	F4 (3/3)	
210	F2 (2/3) F4 (1/3)			0 Fail		
220	F2 (3/3)			0 Fail		
230				0 Fail		
240				F2 (2/3)		
250				F2 (3/3)		

If the failure occurred at a lower current/voltage level, the susceptibility of the IC was considered higher.

III. SOFT-FAILURE SENSITIVITY OVERVIEW

The susceptibility of the USB ICs under test against soft-failure was investigated of the dependence of USB standard generations of the DUT, injected pulse width and injected pulse rise time. The soft-failure thresholds of the devices under test were extracted to summarize and characterize the IC susceptibility with regard to the USB standard information.

A. Soft-failure Susceptivility among USB Generations

14 commercial USB devices of USB 1.1, USB 2.0 and USB 3.0 standard were investigated for soft-failure susceptibility under injected ESD stress. Fig.5 shows the IC pin peak current during failures as soft-failure thresholds of the DUTs versus the USB standard generations that the DUTs belong to.

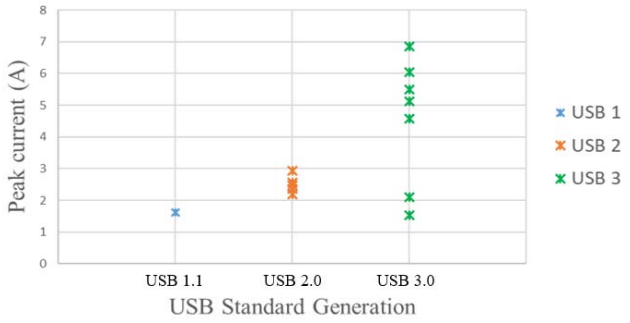

Fig. 5. Failure threshold VS. USB standards of the DUTs.

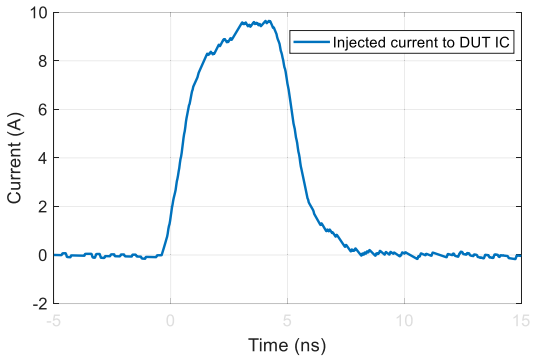

Fig. 6. Injected current waveform measured by the probe.

The devices under test showed a trend of increasing robustness of USB 3.0 ICs than USB 1.1 and USB 2.0, and it appeared that the USB 3.0 DUTs can endure higher peak current at the IC pin before reaching the soft-failure threshold. The I/O structure between USB 3.0 and USB 1,2 may be fundamentally different as to work for unidirectional and bidirectional data streams.

B. Soft-failure Susceptibility Dependence on Pulse Width and Rise Time

As the injected pulse width increased, the DUT IC was expected to have a higher susceptibility to the injected stress. Since more energy associated with the wider pulse was injected into the I/O structure and the IC substrate, the transistor characteristics are more likely changed to cause soft-failures besides bit misinterpretation of the data or the clock. The injected pulse width was varied at 2 ns, 4 ns and 5 ns as the common disturbance stress type that a consumer IC encounters. From the failure conditions summarized for a single DUT as shown in TABLE II and as shown in Fig. 7, the soft-failure sensitivity of the USB IC is dependent on the injected pulse width. A wider pulse has a higher possibility to cause soft-failures at lower injected current levels.

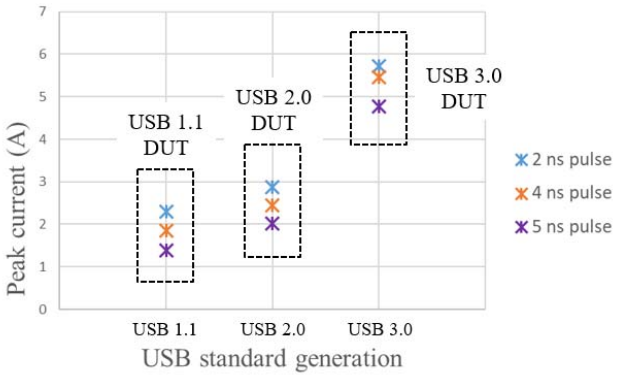

Fig. 7. Pulse width dependence on the soft-failure thresholds.

The IC sensitivity was also expected to have a dependence on the rise time of the injected pulse. The on-chip ESD protection of the IC and the off-chip protections, if any, usually have a turn-on time associated with the transient voltage

suppressor (TVS) diode, which determines how fast the protection can clamp down the transient voltage. A shorter rise time of the injected pulse may result in more current injected into the DUT IC before the TVS diode turns on, and thus lead to a higher possibility of soft-failures. The rise time of the injected pulse was varied at 300 ps and 900 ps to relate to the practical application. However from the testing results, pulse rise time showed an insignificant dependence on the IC susceptibility to ESD stress. The failure threshold did not have much change when the pulse rise time was varied. The failures happened at around similar injected peak currents.

IV. Conclusion

An overview on the commercial USB IC sensitivity of ESD-induced soft-failures is discussed and a new analysis method to measure and characterize the failures under different test conditions is proposed. USB 3.0 products appear to have a higher robustness on injected current against ESD-induced soft-failure, compared to USB 1.1 and USB 2.0. The pulse width of the injected ESD pulse has an effect over the soft-failure threshold of the IC under test, such that a wider pulse containing higher energy can cause a soft-failure to occur more easily. The IC susceptibility, on the other hand, does not have a high dependence on the rise time of the injected ESD pulse.

Acknowledgment

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