Thermoelectric Properties of Holey Silicon at Elevated Temperatures

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Abstract:

Compatibility to the semiconductor industry makes silicon thin film devices attractive for thermoelectric applications. Silicon has a competitive thermoelectric power factor but a large thermal conductivity, which results in an overall small thermoelectric figure of merit, ZT. By patterning arrays of nano-sized holes with spacing less than the average phonon mean free path into the Si thin films, their thermal conductivity can be greatly suppressed while their electronic properties are less affected. We fabricated and measured the electronic and thermal transport properties of such holey Si devices from 300 K to 650 K. Heat diffusion imaging, a hybrid approach that combines thermoreflectance imaging and the heat spreader method was used for the in-plane thermal conductivity measurement and gives a value of 6.00 ± 1.83 W/mK at room temperature. The power factor times temperature is about 0.52 ± 0.04 W/mK at 300 K and 1.10 ± 0.09 W/mK at 650 K. Therefore, ZT of the holey Si device is approximately 0.09 at room temperature and is at least 0.29 at 650 K. Further improvement is possible by optimizing the feature sizes and using surface doping.

1. Introduction:

Silicon-based thermoelectric thin-film materials are compatible with well-established semiconductor process technology, and therefore are promising in a broad range of device

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applications, including thermoelectric sensors integrated into Micro-Electro-Mechanical Systems (MEMS) [1], human energy harvesting [2] and complementary metal-oxide semiconductor (CMOS) MEMS-based thermoelectric power generators [3]. If a favorable efficiency can be achieved, Si thermoelectric devices can be used for many emerging but pressing application scenarios, such as on-chip thermal management [4] and power generation for wearable electronics as well as the Internet of Things (IoT) nodes [5].

Heavily p-doped bulk silicon possesses relatively large thermoelectric power factor times temperature (PFT) of ~ 2.24 W/mK at room temperature [6], suggesting its potential as an excellent thermoelectric material. Silicon has a large lattice thermal conductivity which is up to ~150 W/mK at 300 K for pristine bulk Si [7] and ~ 100 W/mK for heavily-doped bulk Si [6]. A combination of large power factor and large thermal conductivity makes silicon an ideal candidate for active cooling applications. [8,9] However, the large thermal conductivity of silicon is not desired for traditional thermoelectric applications and results in a small thermoelectric figure of merit ZT.

Thermal conductivity suppression can be realized by introducing various scattering processes to increase the scattering rates, hence lowering the phonon mean free path ($l = v\tau$), and/or by modifying phonon dispersion relations to lower the speed of sound and the density of states of phonons. Various techniques are used in literature to alter the thermal conductivity of silicon, including alloying, adding embedded nanoparticles for effective phonon scattering, and using low dimensional structures, such as Si/(Si)Ge superlattice [10][11][12][13] and quantum dot (QD) crystals [14][15], in which the periodicities of the superlattice spacing or QD spacing modify the phonon band structures.

Making superstructures oftentimes requires sophisticated epitaxial growths. The top-down fabrication process on monolithic Si, on the other hand, is closer to device-level applications.

Thermal conductivity can be suppressed by introducing boundary/surface scattering according to the Casimir limit [16]. The confinement length scale acts as a cutoff limit for phonon mean free paths (MFPs). Near 100-fold suppression in lattice thermal conductivity was found in Si nanowires (SiNWs), resulting in a great enhancement in the thermoelectric figure of merit, ZT, reaching 0.4 - 0.6 at room temperature [17][18]. In addition, the quantized electronic density of states in 1D SiNWs possesses a large asymmetry, which is expected to increase the Seebeck coefficient if the chemical potential is carefully manipulated. However, the synthesis of uniform, high-density arrays of SiNWs is non-trivial and is not currently feasible for the scalable production of thermoelectric modules.

The other alternative is to morphologically modify Si thin films to obtain nanopatterned holey Si [19][20] or sometimes referred to as Si nanomesh [21]. The structure is more robust compared to SiNWs and can be fabricated by scalable processes using top-down lithography patterning and etching methods. These films are patterned with periodic holes with spacing that is comparable to, or shorter than, the average phonon MFP of silicon. Such structure gives rise to the so-called "necking effect": the phonons with MFPs longer than the neck size are suppressed. The ballistic phonons scatter off holes and cause a negative local temperature gradient behind the holes, resulting in a significantly reduced thermal conductivity [21][22].

Yu *et al.*[21] found that the thermal conductivity of the Si nanomesh was even smaller than that of the Si nanowires array with the same periodicity (pitch distance), despite the fact that Si nanomesh had a lower surface-to-volume ratio. This indicates that a phononic modification was involved based on the superstructure, where the phonon group velocity decreased due to the flattening of phonon bands. Meanwhile, the electrical properties for the monolithic Si thin film were only slightly reduced in the Si nanomesh with a doping level on the order of 10^{19} $cm^2/V{\cdot}s$ [21]. Tang *et*

al. [19] performed a complete thermoelectric characterization on a similar holey Si membrane device fabricated via nanosphere lithography and block copolymer lithography. The thermal conductivity was dramatically reduced down to 1.73 – 2.03 W/mK in the holey Si device with the neck/pitch size of adjacent holes = 23/55 nm and a membrane thickness of 100 nm. In addition, the power factor reduced only by a factor of ~1.5 compared with the non-holey reference sample, leading to a final ZT of 0.4 at room temperature. However, a more recent work reported a much lower ZT ~ 0.05 in similar samples due to degradation in electrical conductivity as well as a slightly higher measured thermal conductivity [20]. It can be seen that both the transport mechanisms and measurements for holey silicon are quite complex. The properties are rather sensitive to the fine-grained sample specifications, e.g. surface roughness, doping efficiency, and impurities, which are all subject to the fabrication processes.

The works reviewed above are all on *suspended* holey Si films and the thermoelectric transport are characterized at low temperature to room temperature range. A more detailed review of the thermal transport of these nanostructured Si thin films can be found in [23]. In this work, we fabricate and measure a boron-doped holey Si device directly on a silicon on insulator (SOI) wafer, and extend the in-plane thermoelectric transport study to elevated temperature range, which, to the best of our knowledge, has not been reported. Heat diffusion imaing, a hybrid method to measure the in-plane thermal conductivity of thin-film materials using thermoreflectance imaging is used and will be discussed.

2. Device and Methods

2.1. Device Fabrication

A 4" SOI wafer with a 100 nm active Si layer on a 1 μm buried oxide was first sent to Leonard Kroko Inc. for the blanket boron implantation, which would eventually yield a 3×10^{19} – 1×10^{20}

cm^{-3} p-type doping level (boron 5 keV, 3×10^{14} atoms/cm^2 followed by boron, 25 keV, 3×10^{14} atoms/cm^2 with 7 degrees off-axis tilt). Rapid thermal annealing was then conducted at 1100 °C for 30 seconds to repair the implant damage and activate the boron dopants. Electron beam lithography (EBL) was used to write a square lattice of dot array to an area size of 30 μm × 200 μm for each device, with a dot (hole) pitch spacing of 100 nm. Resist development was conducted to transfer the pattern onto the Si surface, and reactive ion etching (RIE) was then used to etch the exposed areas to generate an array of holes, with a diameter of ~55 nm (neck size ~45 nm). Subsequently, the active device areas were covered with resist, and the rest of the Si layer was etched down to the buried oxide (BOX) to form arrays of 30 μm × 200 μm Si mesas for the following metallization. A 1 μm Al layer with 50 nm Au capping layer (Al can form Ohmic contact with p-type Si, and the Au cap helps to prevent Al from oxidation) was deposited as contacts for the transport measurements. The holey Si device and the contact configuration are shown in Fig. 1, where the contacts, heater, and thermometers are annotated. The fabricated wafer was then diced into 9 mm × 9 mm chips to be placed in dual in-line packages and wire bonded for the following thermoelectric transport measurements.

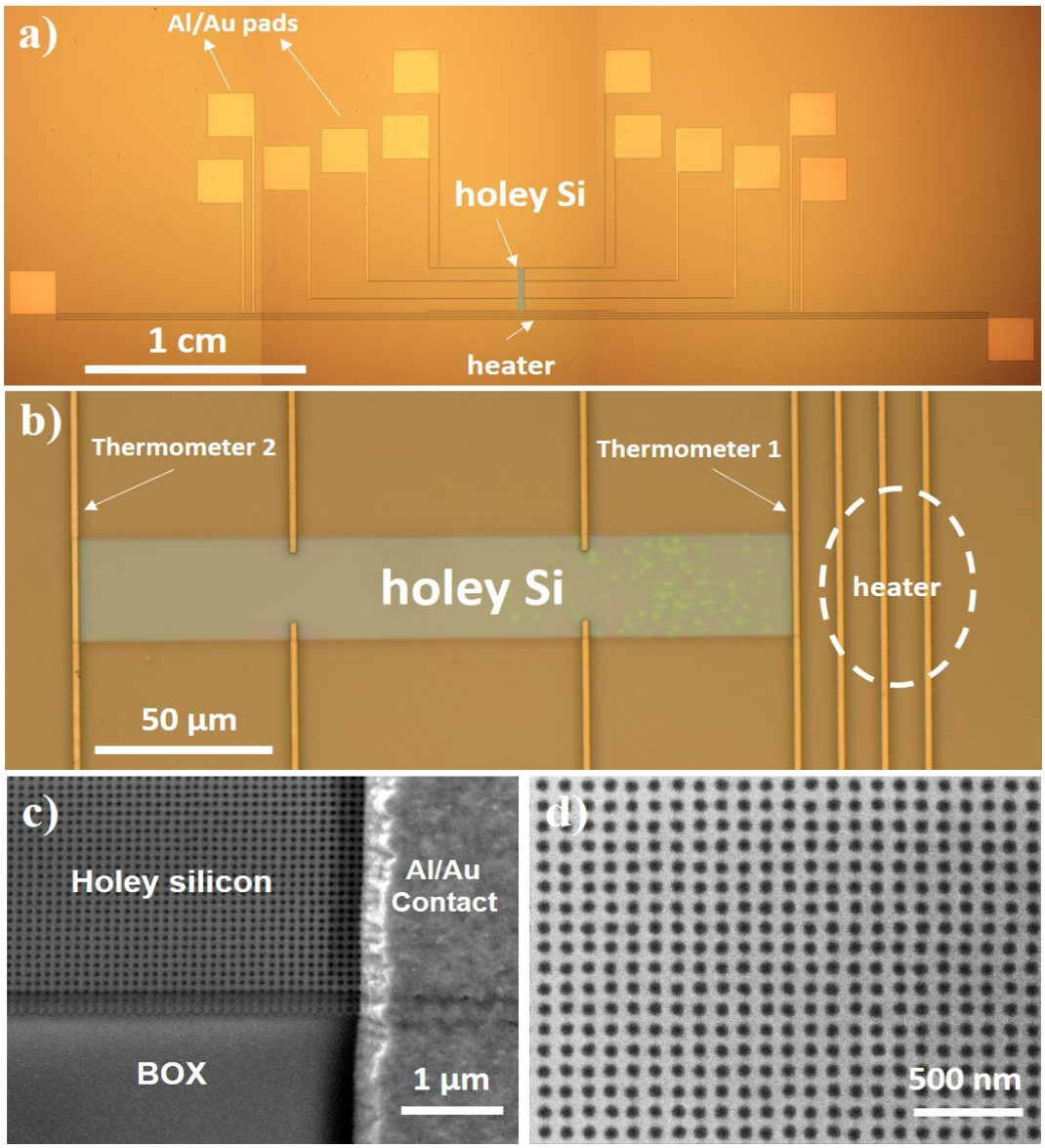

Fig. 1. a) Holey Si device configuration for transport measurements. b) Close-up of the holey Si thin film, rotated 90° from a). c) SEM image showing the holey Si film on the buried oxide (BOX) layer, as well as the Al/Au metal contact. d) Enlarged view of the holey Si device.

2.2.Electrical Transport

The packaged devices were mounted in a JANIS cryostat for electrical transport measurements in the 300 K to 650 K temperature range under vacuum (~ 10^{-6} torr). The Seebeck coefficient was measured using a resistive micro-heater and two calibrated thermometers, as annotated in Fig. 1 a) and b). The current was applied to the heater to generate a temperature difference across the two ends of the holey Si mesa as a result of Joule heating. This temperature difference and the produced Seebeck voltage were measured using the two thermometers at the two ends of the sample. Fig. 2 a) displays the Seebeck voltage response of the holey Si device when a 30 mA current was applied to the heater at 350 K. When the heater was turned on, the absolute voltage instantly changed and quickly saturated at ~ 225 μV, indicating that a steady-state temperature difference was built up across the two ends of the sample. The resistance versus time curves of the two thermometers was simultaneously measured using two separate lock-in amplifiers as shown in Fig. 2 b) and d). By raising the ambient temperature up about 10 K while keeping the heater OFF, the resistance of the thermometers was calibrated to the corresponding temperature in a separate run, as shown in Fig. 2 c) and e). The thermometer temperatures were extracted accordingly, assuming a constant temperature coefficient of resistance in this case. The temperature difference was determined to be 0.98 ± 0.06 K, giving a Seebeck coefficient of 239.5 ± 5.1 μV/K at 350 K. The positive sign of the Seebeck coefficient confirms the p-type conduction mechanism in the boron-doped holey Si device. Using the same method, the temperature dependence of the Seebeck coefficient was obtained and will be discussed in the next section.

The electrical conductivity was measured using the standard four-point probe method. A

small current of 0.1 μA was used for the measurement and a lock-in amplifier was used to improve

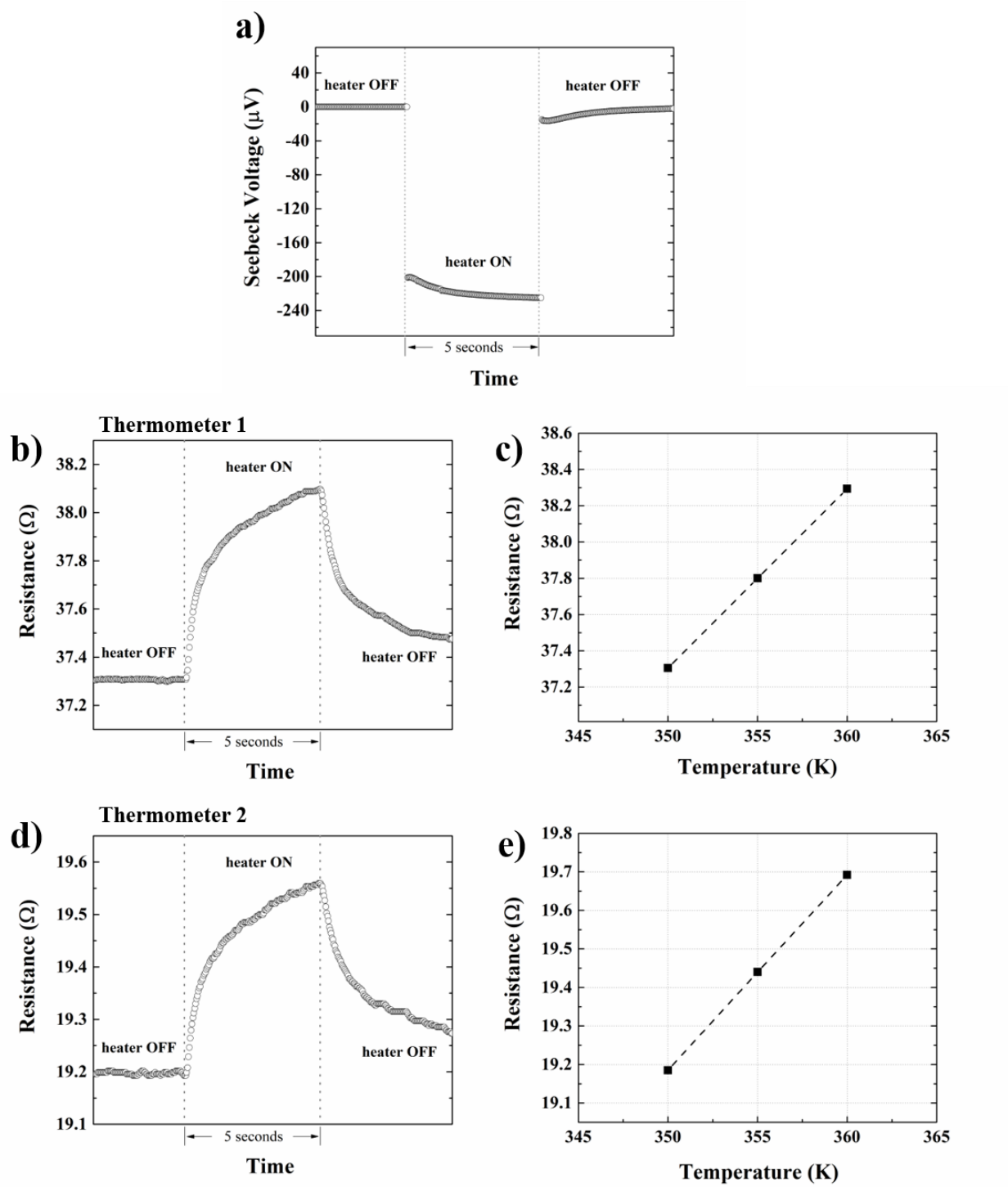

Fig. 2. a) Seebeck voltage response of the doped holey Si device when the heater is ON/OFF; and the corresponding resistance change of b) thermometer 1 and d) thermometer 2 as a function of time at 350 K. c) and e) are temperature calibration for thermometers in b) and d) respectively.

the signal to noise ratio.

2.3.Thermal Transport

In-plane thermal conductivity measurement for thin-film materials still remains challenging in practice. For thin films on a substrate, there are only very few methods available. The two main methods are namely the variable-linewidth 3ω method [24] and the heat spreader method [25]. Both methods are difficult to implement and require a highly sophisticated device structure for measurement. Cross-plane thermal conductivity is usually measured instead, using the 3ω method [26] or time-domain thermoreflectance (TDTR) method [27][28], granted that the material is isotropic. Due to its morphology and geometry, thermal transport in holey Si is highly anisotropic. . The thermoreflectance measurement combined with finite element modeling has been used in the past to extract the in-plane thermal conductivity of Si thin films [29]. Here, we use a modified heat spreader method [25] combined with thermoreflectance imaging to extract the in-plane thermal conductivity of the holey Si device. We refer to this method as heat diffusion imaging. This method is more direct and does not require extensive combined modeling. .

The refractive index of the sample surface changes according to the temperature variation (ΔT) and the changes in the reflected light intensity ($\Delta R/R$) are collected by the thermoreflectance imaging system. Their relation can be expressed as [30][31]

$$\frac{\Delta R}{R} = \chi \Delta T, \qquad (1)$$

where χ is the thermoreflectance coefficient, and it mainly depends on the studied material and the wavelength of the light source. By mapping the spatial changes in the reflectivity, a relative temperature variation profile of the area of interest can be plotted. Except for some well-documented elemental materials, such as Au and Pt, the thermoreflectance coefficient for each material needs to be calibrated to obtain the absolute temperature values.

The thermoreflectance imaging system [32] from MicroSanj in our laboratory and its schematic diagram are shown in Fig. 3. A control unit generates and synchronizes a LED light source (530 nm green light was used in this study) for illumination and a pulsed electrical voltage is applied to the gold line fabricated on the silicon device. The temperature change due to the applied voltage pulse modifies the surface reflection intensity, which is captured by a charge-coupled device (CCD) camera and sent back to the control unit for analysis. The synchronization diagram for a typical transient thermoreflectance measurement can be found in Ref. [31]. A precise lock-in of the light and electrical signals allows the system to capture the transient temperature mapping under bias. Since the thermoreflectance coefficient is usually very small (on the order of 10^{-4} [31]), signals measured by the CCD camera are averaged over many device thermal excitation cycles to improve the signal-to-noise ratio.

The in-plane thermal conductivity of the holey Si active layer can be derived by examining how heat propagates along the film according to the classical fin equation [33]. In our case, the thin

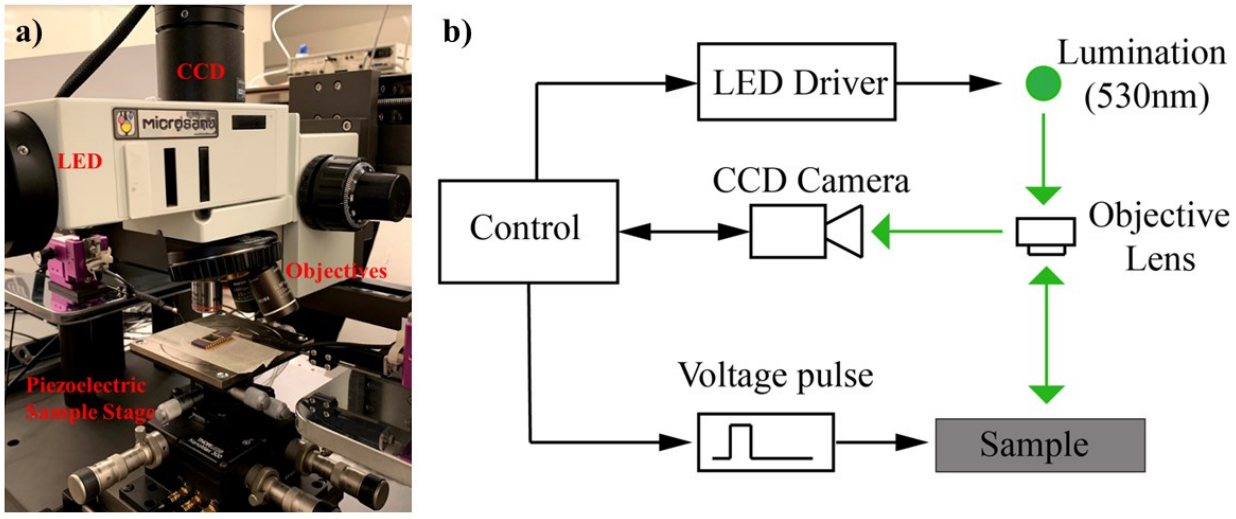

Fig. 3. a) MicroSanj thermoreflectance imaging system in our laboratory and b) its working schematic diagram.

film of interest (holey Si) sits on an insulation layer (buried oxide) and the metal line deposited at the end of the film serve as the heater. When a pulsed voltage is applied to the heater, Joule heating

spreads along the film, building up a temperature decay profile away from the heater. This temperature profile obeys the classical fin equation and decays exponentially in the lateral direction [33]. The temperature-position relation can be written as

$$T(x) - T(\infty) \propto e^{-\beta x}, \quad (2)$$

$$\beta = \sqrt{\frac{h_i}{k_x d}}, \quad (3)$$

where x is the position along the x axis, k_x is the in-plane thermal conductivity of the film and d is the thickness of the film. $h_i = k_{i,z}/d_i$ accounts for the cross-plane conduction into the insulation layer underneath, where $k_{i,z}$ and d_i are the cross-plane thermal conductivity and the thickness of the insulation layer, respectively. With the substrate properties and the geometry known and the temperature profile measured, we can extract the in-plane thermal conductivity of the holey silicon. This approach is identical to the heat spreader method and has been discussed extensively in the past. [25] The heat spreader method has been verified for Si thin films on SiO_2/Si substrate [34] and for few layer graphene on SiO_2 [35]. Here the main difference is the use of thermal imaging instead of thermometers to measure the temperature profile. There are several advantages. First, we do not need to fabricate extra thermometers. Second, we can measure the temperature directly on the sample. We note that the thermometers in traditional heat spreader method are spaced slightly away from the sample as an electrical insulating layer is needed underneath the metallic thermometers. Finally and most importantly, we are not limited to only few data points. Instead, we can take hundreds of temperature data points along the sample making our fitting more reliable and more accurate.

3. Results and Discussion

The measured temperature dependence of the electrical conductivity and the Seebeck coefficient is shown in Fig. 4. The trend indicates a metallic behavior due to the heavy boron doping (3×10^{19} – 1×10^{20} cm^{-3}). The electrical conductivity gradually decreases with increasing temperature, due to higher electron-phonon scattering rates. As the temperature increases, the chemical potential shifts closer to the middle of the bandgap, resulting in a rising Seebeck coefficient.

The corresponding power factor times temperature (PFT) curve is shown in Fig. 4 c), in which a PFT of 0.52 ± 0.04 W/mK at room temperature and a PFT of 1.10 ± 0.09 W/mK at 650 K are obtained. The room-temperature PFT is slightly lower than that of the suspended holey Si film (~ 0.69 W/mK) reported in Ref. [19], but significantly exceeds the reported value of ~ 0.15 W/mK in Ref. [20], with a similar device configuration and doping level. This discrepancy, besides measurement methodology, should come from the distinct fabrication processes, which have direct impacts on surface roughness, doping efficiency, impurity level, etc. Our values are plotted with other Si samples (holey thin films [19,20], non-holey thin films [19,20], polycrystalline thin film [36,37], nanostructured bulk Si [38] and single-crystal bulk [6,39]) of similar doping concentrations for comparison.

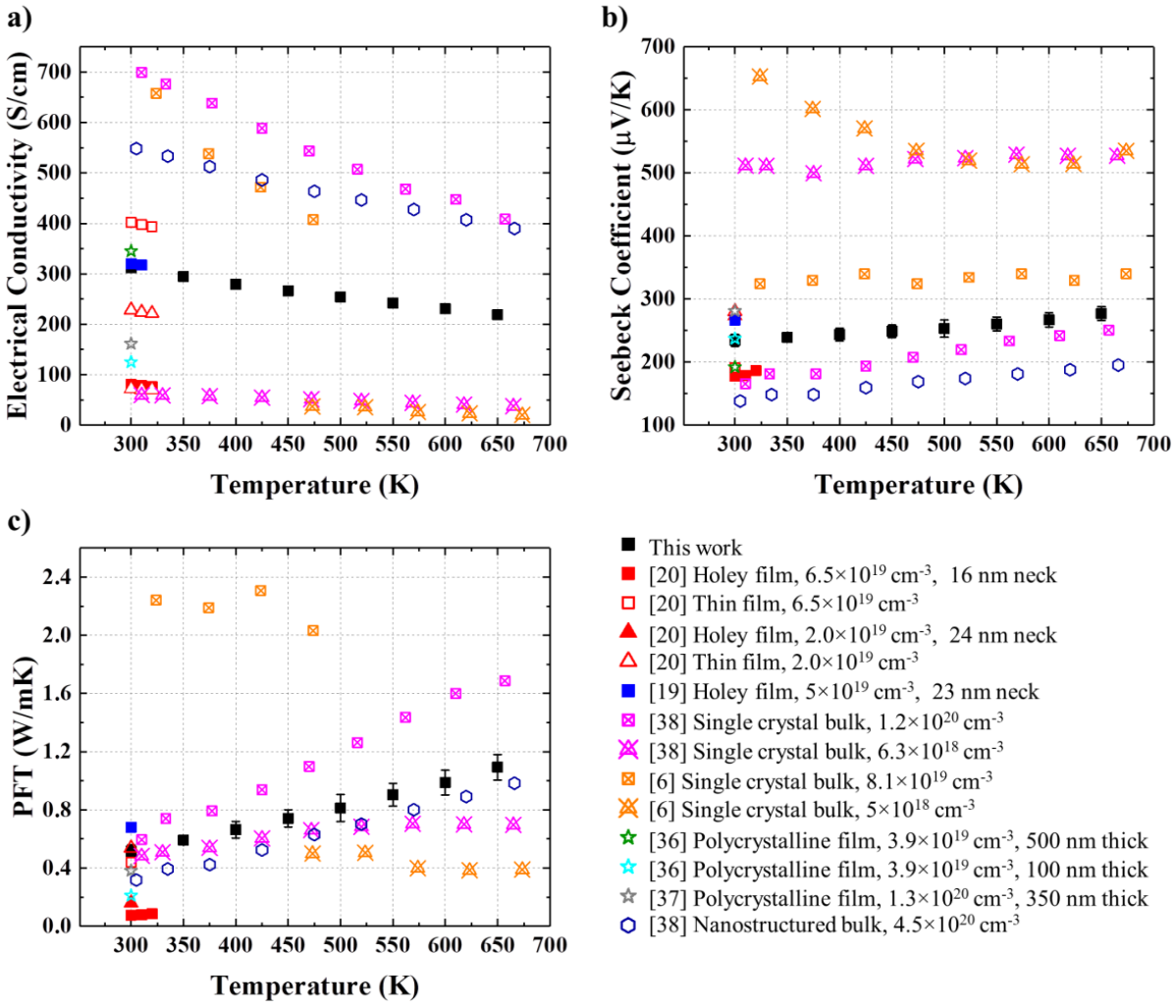

Fig. 4. Temperature dependence of a) electrical conductivity, b) Seebeck coefficient and c) power factor times temperature (PFT) of the doped holey Si device in comparison with doped Si samples from literature [6,20,36–40]. The closed symbols are for holey Si thin films including this work, the open symbols are for plain Si thin films, the crossed symbols are for single crystal bulk Si, the star symbols are for polycrystalline thin films and the hexagonal symbols are for nanostructured bulk. All samples are boron doped with carrier concentrations noted in the legend. The thin films are 100 nm thick unless otherwise noted.

In order to measure thermal conductivity, a pulsed voltage of up to 5 V, with 5 to 10 ms pulse width and 30% duty cycle, was applied to the heater deposited at one end of the thin-film and the resulting temperature drop was measured using the thermoreflectance method. Fig. 5 shows the temperature

gradient map over the thin film in steady-state averaged over a few hundred thermal cycles. As shown in Fig. 5, we also repeated the measurement on a non-holey silicon thin film as a reference and a base for comparison. The reference silicon thin-film is lightly doped (~10^{16} cm^{-3}) and has the same dimension (100 nm thick). It can be observed that the resultant temperature rise from the heater extends over longer distance on the non-holey Si thin film than on the holey Si one, due to a much larger thermal conductivity.

Since β is derived from the exponential fitting factor of the temperature profile, calibration for the exact thermoreflectance coefficient to get the absolute temperature map is not necessary and an arbitrary unit is adopted for the temperature. The same constant thermoreflectance coefficient is assumed for all the temperature maps. Multiple temperature gradient line profiles along the length of the Si thin films, which start from just outside the edge of the perpendicular heater line and point away from the heater, have been taken on each device to reduce the uncertainty in the results. The representative temperature profiles of both films are shown in Fig.5 c) and d). The distance/pixel of these temperature maps obtained with 100 x magnification objective is about 60 nm so we do not have the resolution to detect the temperature change across a hole of 55 nm diameter.

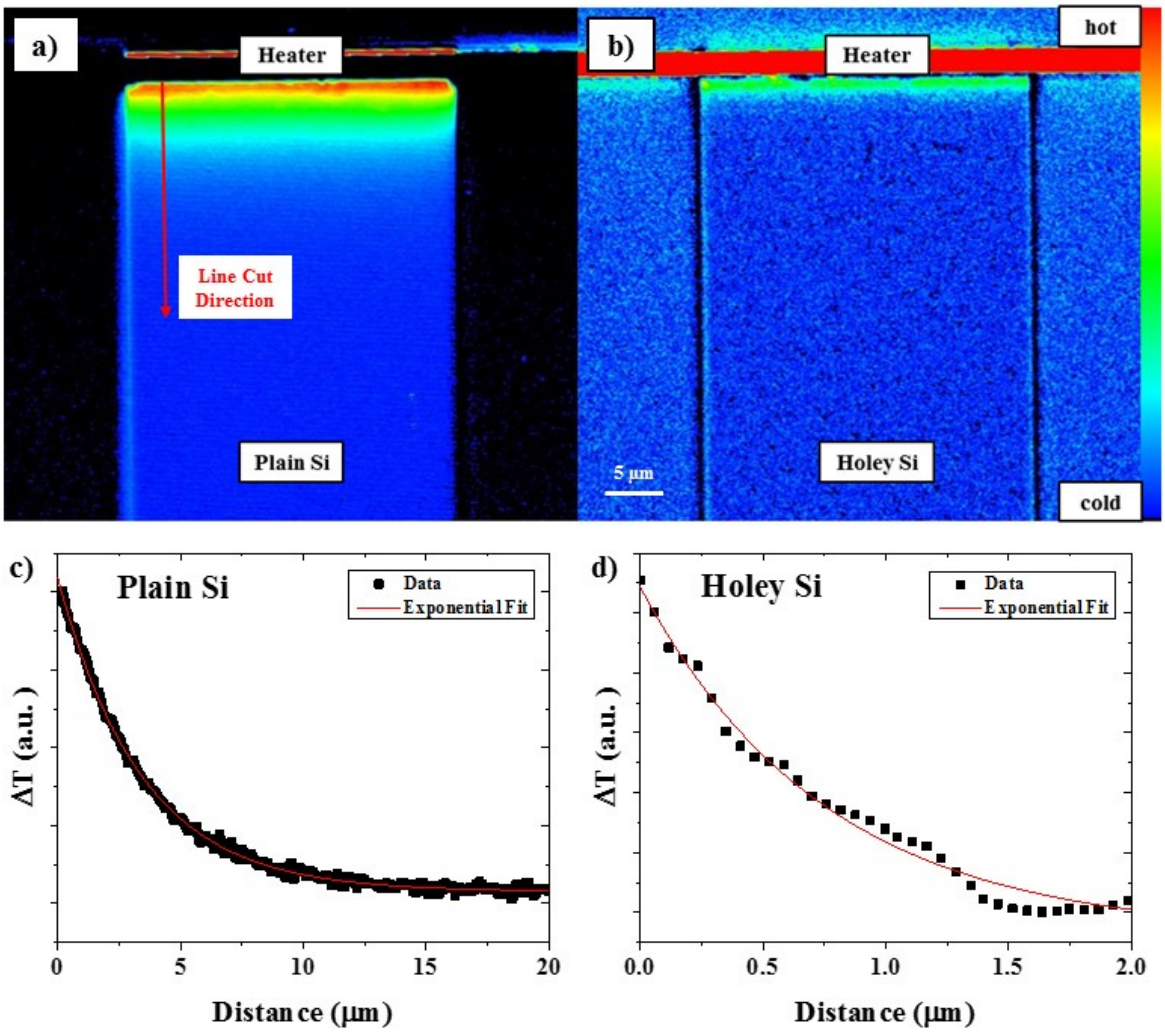

Fig. 5. Temperature variation maps of a) plain, non-holey Si and b) holey Si sample produced by the thermal imaging system with 4 V applied to the heater at one end of the sample, and 530 nm LED illumination. Note that the heater in a) is shown in dark color because its thermoreflectance coefficient has an opposite sign to the coefficient assumed. c) and d) are representative temperature decay profiles on a) the non-holey and b) the holey Si devices. Arbitrary unit for temperature, relative to the thermoreflectance coefficient used, is adopted here.

The parameter β and thus the in-plane thermal conductivity can be extracted by performing an exponential fit to the temperature line profiles according to Eq. (3). The thickness of the holey silicon film for our sample is 100 nm and that of the insulating SiO_2 layer is 2 µm. The thermal conductivity of the thermally grown SiO_2 is ~ 1.35 W/m K [41]. The heat conductance of the

substrate is $h_i = 6.75 \times 10^5$ W/(m^{2}K). The convection to the surroundings is in parallel with h_i and is on the order of 10 W/(m^{2}K) [33], which is negligible compared to the heat leak to the substrate. The thermal contact conductance between the holey silicon layer and the SiO_2 layer is in series with h_i and is much larger (about 2 G W/m^{2}K [42–44]), which makes it also negligible. Rearranging Eq. 1, the in-plane thermal conductivity is $k_x = \frac{h_i}{d\beta^2} = \frac{6.75\times10^{12}}{\beta^2}$ W/mK. Using the values of β obtained from the exponential fitting curves, the average k_x for the plain Si sample is ~ 73.21 ± 1.54 W/mK, while that for holey Si is ~ 6.0 ±0.2 W/mK at room temperature. For plain Si thin films with doping concentrations smaller than 10^{17} cm^{-3}, the phonon-boundary scattering dominates over the phonon-impurity scattering [45] and thus it is possible to compare our value with thermal conductivity of pure silicon thin films. The value obtained for plain Si thin film is consistent with previous experimental studies on nearly intrinsic Si samples of similar thickness [46–48] within reasonable errors, which validates our measurement.

Our thermoreflectance imaging setup was then moved to a cryostat with an optical window for measurements up to 391 K. The thermal conductivity of the underlying SiO_2 at those temperatures has been taken from the recommended values for fused bulk SiO_2 [7]. As shown in Fig. 6 a), the in-plane thermal conductivity of holey Si decreases with rising temperatures due to increased phonon scattering. At 391 K, the thermal conductivity is about 3.8 ± 0.3 W/mK.

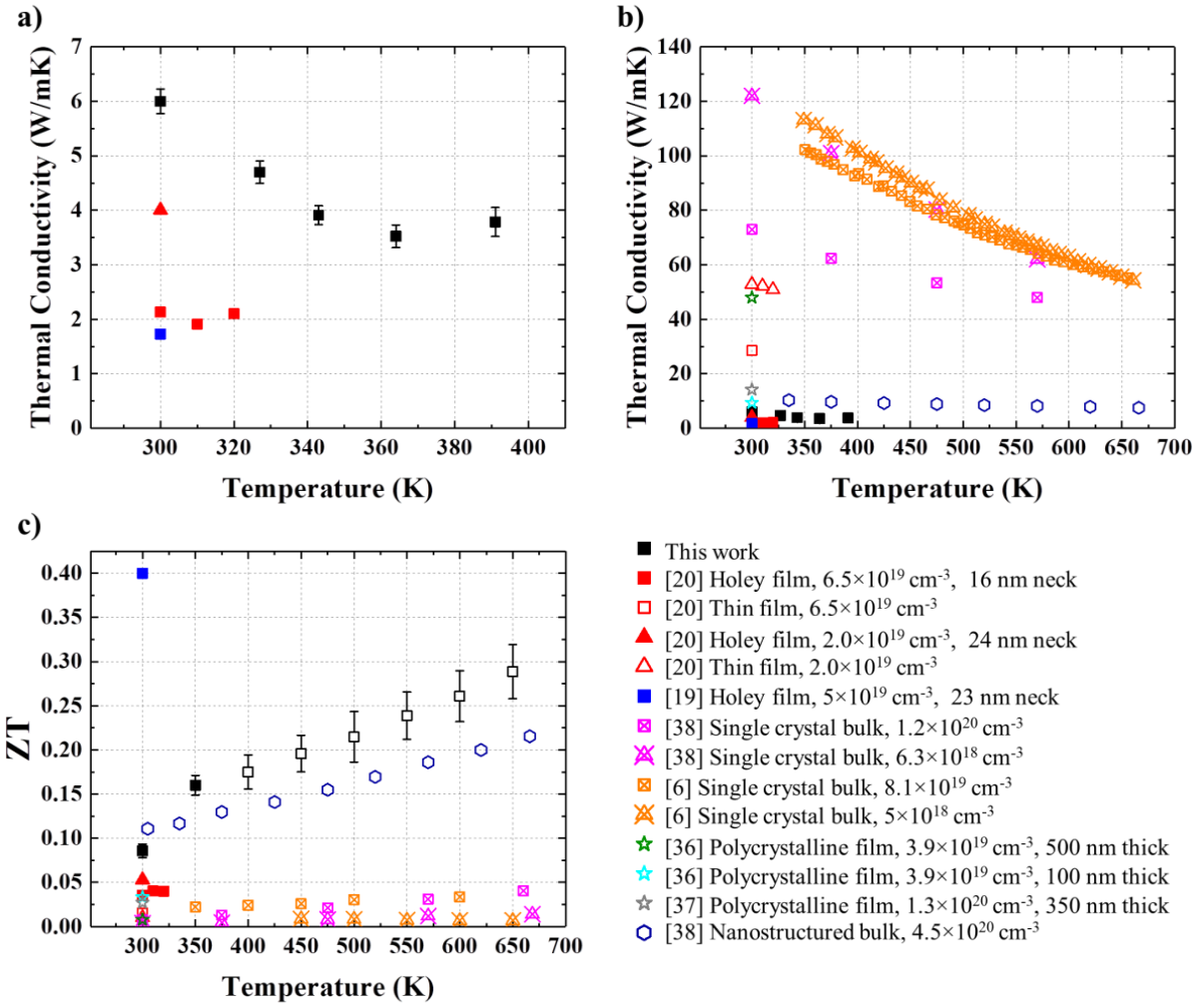

Fig. 6. Temperature dependence of a) thermal conductivity of our holey Si device compared with other holey Si devices from literature, b) the thermal conductivity of Si samples with similar carrier concentrations and c) the figure of merit, ZT. The closed black symbol represents our experimental data and the open black symbols give our projected ZT by assuming a constant thermal conductivity against temperature higher than 391 K. The results are compared with data from literature [6,20,36–40]. All samples are boron doped with carrier concentrations noted in the legend. The thin films are 100 nm thick unless otherwise noted.

The thermoelectric figure of merit, ZT, can then be calculated for the holey Si device. At room temperature, ZT is approximately 0.09. As the temperature increases, the rate of change in its thermal conductivity gradually decreases. We expect minor changes in the thermal conductivity of holey Si above 400 K and we can estimate the lower limit of its ZT at higher temperatures by

assuming a constant thermal conductivity 3.8 ± 0.3 W/mK. The projected temperature dependence of ZT is provided in Fig. 6 b). The holey Si device becomes more efficient at elevated temperatures, with its ZT exceeding 0.29at 650 K.

A comparison of the room temperature thermoelectric properties between our holey Si device and other Si samples reported in literature is provided in Table 1. Our room temperature ZT shows more than 4 times improvement over the highly-doped bulk Si sample [6], due to the 16-fold reduction in thermal conductivity. For holey Si thin films, the phonon MFP, and thus the thermal conductivity, is reduced with reduction in the neck size, i.e. the distance between neighboring holes [23]. Due to a larger neck size compared to the other two reports on holey Si devices [19,20], the thermal conductivity is slightly higher. Nevertheless, the room temperature ZT is still higher than that in Ref. [20] due to a superior electrical transport performance.

Sample	Carrier Concentration (cm^{-3})	Electrical Conductivity (S/cm)	Seebeck Coefficient (μV/K)	Thermal Conductivity (W/mK)	ZT
Highly doped bulk Si	8.1×10^{19}	~ 588.2	328	102	0.022
Holey Si with 23 nm neck size	5×10^{19}	~ 320	~ 265	1.73 ± 0.06	0.4
Holey Si with 24 nm neck size	2.0×10^{19}	~ 80	270 ± 22	~ 4	0.05
Our device with 45 nm neck size	$3 – 10\times10^{19}$	312 ± 1	235 ± 10	6.00 ± 1.83	0.09

Table 1. Measured thermoelectric properties of our holey Si device compared with other Si samples reported in literature [6,19,20] at 300 K. All samples are p-type.

4. Conclusions

A nanopatterned holey silicon device was fabricated and its thermoelectric properties were studied for the first time at elevated temperatures (up to 650K). The heat diffusion imaging was developed for the in-plane thermal conductivity measurement. A greatly suppressed thermal conductivity of 6.0 ± 0.2 W/mK was obtained at room temperature due to enhanced phonon scattering by the nanopatterned holey morphology. The PFT is 0.52 ± 0.04 W/mK, leading to a ZT of ~ 0.09 at room temperature. An improved thermoelectric performance was observed at elevated temperatures, with a doubled PFT of 1.10 ± 0.09 W/mK at 650 K. Thus, a lower limit on ZT of ~ 0.29 at 650 K can be estimated, assuming a constant thermal conductivity with temperature. Both the nanofabricated material and the transport measurement methodology are of great interest in thermoelectric device applications.

Acknowledgment

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