Decoupling Capacitor Placement Optimization With Lagrange Multiplier Method

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***Abstract*—This paper proposes a decoupling capacitor placement optimization method based on the cavity model and Lagrange multiplier. The variable conditions associating with coordinates (x,y) of input impedance expression based on the cavity model are combined with the Lagrange multiplier method. The decoupling capacitor optimum placement within a defined area of the board can be found through the proposed analytical method. The example of finding an optimum location of the decoupling capacitor within a defined area of the power delivery network is exposed, the results are compared to the brute-force method to prove the effectiveness of the proposed method.**

***Index Terms*—Cavity model, Decoupling capacitors, Lagrange multiplier method, PDN**

I. Introduction

With rapid technology development, the integrated circuit (IC) is yielding faster transition. As the switching speeds of processor clocks rates rise and more functions are embedded onto the IC, the power consumption is increased dramatically. The current load can reach over 100 A on a printed circuit board (PCB) [1]. Therefore, the power noise poses a challenge for the power delivery network (PDN) design. The impedance of the PDN with effects of the high transient current can generate significant noise affecting the functional devices on the same power rail.

To reduce the PDN noise, a well-designed PDN network with decoupling capacitors is needed. However, due to the limits of the geometry, the cost and the performance of the PCB, the decoupling capacitors need to be placed carefully to reduce the number of decoupling capacitors and the PDN noise. Lots of researches have been done to investigate the placement of decoupling capacitors [2]–[5].

Previous works have developed the input expressions related to the coordinate of the placement based on the resonant cavity model [6]. With the multi-port parameters expressed cavity model, the input impedance expression can be easily obtained. The semi-analytical method to optimize the placement of the decoupling capacitor based on the input impedance expression with respect to the angle and radial distance have been developed in [4].

However, optimizing the placement in a limited region on the board is very rare in previous works. Therefore, we propose a method based on the Lagrange multiplier method with VRM effect to optimize the placement of the decoupling capacitor within a dedicated area on the PCB board. The Lagrange multiplier method is suitable to optimize multiple variables system with linear and nonlinear, equality and inequality conditions [7]. The details and results are discussed in this paper.

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II. Proposed Semi-analytical Method Development

The details of the analytical expression of cavity model of PDN and Lagrange multiplier methods are expressed. The mathematical expressions of the proposed method for decoupling capacitor placement are developed.

A. Input impedance expression with respect to coordinate of placement

To formulate the problem, a parallel plane with dimension a, b, and dielectric thickness d is applied. The multi-port impedance parameters Z_{ij} of a parallel plane can be formulated by representing the standing waves inside the gap of the planes as an infinite set of trigonometric functions [6].

$$Z_{ij} = \frac{j\omega\mu d}{ab}\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\cdot \frac{c_m^2 c_n^2 f_p \cos k_m x_i \cdot \cos k_n y_i \cdot \cos k_m x_j \cdot \cos k_n y_j}{k_m^2 + k_n^2 - k^2} \tag{1}$$

Where c_m and c_n equal to 1 for $m, n = 0$, and $\sqrt{2}$ for $m, n \neq 0$; $k_m = m\pi/a$; $k_n = n\pi/a$; (x_i, y_i) and (x_j, y_j) are the coordinates of ports i and j; the f_p and the waveguide number k are shown as follows:

$$f_p = \operatorname{sinc}\left(\frac{k_m W_{xi}}{2}\right)\cdot \operatorname{sinc}\left(\frac{k_n W_{yi}}{2}\right)\cdot \operatorname{sinc}\left(\frac{k_m W_{xj}}{2}\right)\cdot \operatorname{sinc}\left(\frac{k_n W_{yj}}{2}\right) \tag{2}$$

$$k = \omega\sqrt{\mu_d \varepsilon_d}\cdot\left(1 - j\left(\frac{\tan\delta + \sqrt{2/\omega\mu_c\sigma_c}/d}{2}\right)\right) \tag{3}$$

Where (W_{xi}, W_{yi}) and (W_{xj}, W_{yj}) are the dimensions of ports i and j, respectively.

The impedance matrix of the parallel planes with decoupling capacitors and VRM can be expressed as in (4) [8], [9]:

$$\mathbf{Z_{n\times n}} = \left(\mathbf{E_{n\times n}} + \mathbf{Z_{pp}} * \mathbf{Y_C}\right)^{-1} * \mathbf{Z_{pp}} \tag{4}$$

where $\mathbf{E_{n\times n}}$ is an identity matrix with size n which is the number of the ports; $\mathbf{Z_{pp}}$ is the all the multi-port impedance

parameters Z_{ij} of a bare parallel plane; $\mathbf{Y_C}$ is a diagonal matrix contain the admittance elements of the VRM and decoupling capacitors. Equation (5) shows an example with only one decoupling capacitor of $\mathbf{Y_C}$.

$$\mathbf{Y_C} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1/Z_{vrm} & 0 \\ 0 & 0 & 1/Z_C \end{bmatrix} \tag{5}$$

The input impedance $Z_{in} = \mathbf{Z_{11}}$ at the port can be obtained through (4).

B. Optimization of decoupling capacitor placement with Lagrange multiplier method

Lagrange multipliers method can transform the optimization question with m variables and n conditions to the optimization question of $m+n$ variables without conditions. When applied to inequality and equality conditions, the following general forms can be expressed [7]:

$$\begin{aligned} &minf(x) \\ s.t \quad &h_j(x)) = 0,\ j = 1, 2, 3...n' \\ &g_i(x) \leq 0,\ i = 1, 2, 3...n \end{aligned} \tag{6}$$

The minimum solution of the optimization of the question can be found by adding the Lagrange multipliers and making its gradient to zero. The optimum location of the decoupling capacitor can be found by integrating the input impedance expression and Lagrange multiplier method when the locations of the VRM and port have been defined. The inequality conditions of the optimization are defined based on the selected region from point $\mathbf{P(x_1, y_1)}$ to $\mathbf{O(x_2, y_2)}$ on the board as shown in following equations:

$$\begin{aligned} x_1 \leqslant x \leqslant x_2 \\ y_1 \leqslant y \leqslant y_2 \end{aligned} \tag{7}$$

Therefore, the functions of the inequality condition for the locations can be written as shown in (8):

$$\begin{aligned} g_1(x) &= x - x_1 - {s_1}^2 \\ g_2(x) &= x_2 - x - {s_2}^2 \\ g_3(y) &= y - y_1 - {s_3}^2 \\ g_4(y) &= y_2 - y - {s_4}^2 \end{aligned} \tag{8}$$

where $s_{1,2,3,4}$ are called the slack variables because they make up the slack in the inequalities. The revised problem is: minimize $f(x, y) = Z_{in}$ subject to functions in (8). The Lagrange multiplier formulation is:

$$\begin{aligned} L(x, y, s_{1,2,3,4}, \lambda_{1,2,3,4}) = f(x, y) + \lambda_1 g_1(x) + \\ \lambda_2 g_2(x) + \lambda_3 g_3(y) + \lambda_4 g_4(y) \end{aligned} \tag{9}$$

where $\lambda_{1,2,3,4}$ are the multipliers of inequality $g(x)$ function.

The gradient operation can be performed to have the minimum solution of Z_{in} with the inequality constraint of the coordinates (x, y) as shown in (10):

$$\nabla L(x, y, s_{1,2,3,4}, \lambda_{1,2,3,4}) = 0 \tag{10}$$

The optimization for this multiple variables with inequality conditions can be transformed to find the minimum solution within the Karush-Kuhn-Tucker (KTT) conditions. Since the solutions of $\nabla L(x, y, s_{1,2,3,4}, \lambda_{1,2,3,4}) = 0$ will have multiple results, the KTT can help us to define which result satisfy the conditions. The gradient of (9) will generate ten equations shown in (11). (x_1, y_1) and (x_2, y_2) are known as the selected area to place the decoupling capacitor. In addition, these equations can be manually reduced to six equations. By solving these equations with ten variables $x, y, s_{1,2,3,4}, \lambda_{1,2,3,4}$, the solutions can be obtained. Then, the KTT conditions can be applied to find the optimum solution among them. Normally, equation (9) is nonlinear system equations which is difficult to have the analytical solutions. However, there are researches have been done to investigate the numerical solutions with equality conditions based on Newton's method [10].

$$\begin{cases} \frac{\partial L}{\partial x} = \frac{\partial f(x,y)}{\partial x} = \frac{\partial Z_{in}}{\partial x} = 0 \\ \frac{\partial L}{\partial y} = \frac{\partial f(x,y)}{\partial y} = \frac{\partial Z_{in}}{\partial y} = 0 \\ \frac{\partial L}{\partial \lambda_1} = \frac{\partial (\lambda_1 g_1)}{\partial \lambda_1} = x - x_1 - s_1^2 = 0 \\ \frac{\partial L}{\partial \lambda_2} = \frac{\partial (\lambda_2 g_2)}{\partial \lambda_2} = x_2 - x - s_2^2 = 0 \\ \frac{\partial L}{\partial \lambda_3} = \frac{\partial (\lambda_3 g_3)}{\partial \lambda_3} = y - y_1 - s_3^2 = 0 \\ \frac{\partial L}{\partial \lambda_4} = \frac{\partial (\lambda_4 g_4)}{\partial \lambda_4} = y_2 - y - s_4^2 = 0 \\ \frac{\partial L}{\partial s_1} = \frac{\partial (\lambda_1 g_1)}{\partial s_1} = -2\lambda_1 s_1 = 0 \\ \frac{\partial L}{\partial s_2} = \frac{\partial (\lambda_2 g_2)}{\partial s_2} = -2\lambda_2 s_2 = 0 \\ \frac{\partial L}{\partial s_3} = \frac{\partial (\lambda_3 g_3)}{\partial s_3} = -2\lambda_3 s_3 = 0 \\ \frac{\partial L}{\partial s_4} = \frac{\partial (\lambda_4 g_4)}{\partial s_4} = -2\lambda_4 s_4 = 0 \end{cases} \tag{11}$$

III. Results Analysis

The proof of concept (POC) is defined as Fig. 1 with the dimension a, b, d are 130 mm, 100 mm and 0.1 mm respectively. The dielectric constant and loss are 4.4 and 0.02 respectively. The Port 1 is located at (45 mm,10 mm) by taking the dimension (a, b) as the (x, y) coordinate system. The VRM with $R = 0.1\ \Omega$, $L = 1\ nH$ is located at (5 mm, 7 mm) on the plane. To formulate the problem, suppose that a 1 nF decoupling capacitor with ESR = 0.06 Ω, ESL = 0.04 nH needs to be placed within the highlighted blue region from point $\mathbf{P}$(52.5 mm, 6 mm) to $\mathbf{O}$(73 mm 26.5 mm) in Fig. 1, we need to find the optimum location of the decoupling capacitor in this region. The input impedance Z_{in} of the parallel plate

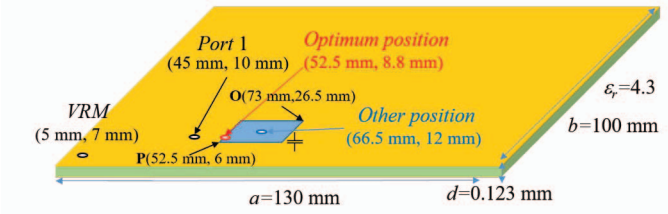

Fig. 1. Parallel planes with decoupling capacitor placement

with only VRM can be obtained as the solid curve shown in Fig. 2 through the computation. The input impedance of the decoupling capacitor is shown as the dashed line in Fig. 2. We can observe that the decoupling capacitor can pull down the resonance at 718 MHz. The optimum location (52.8 mm, 8.8

mm) computed by solving (11) is located on the edge of the highlight red region close to the Port 1. The simulation time for a single decoupling capacitor location optimization is around 1 second. Fig. 3 shows the Z_{in} comparison of different cases of

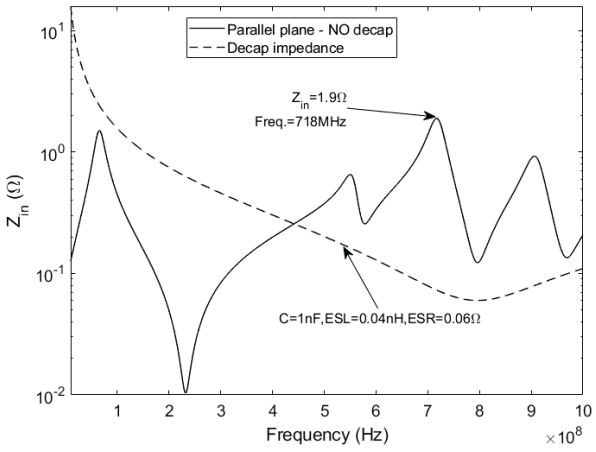

Fig. 2. Z_{in} of the parallel plate without decoupling capacitors

the parallel planes. The dashed black curve in Fig. 3 indicates the parallel planes without decoupling capacitor, a resonance at 718 MHz with impedance 1.9 Ohm is marked. The blue curve indicates when the decoupling capacitor is placed at the middle (66.5 mm, 12 mm) of the selected blue region in Fig. 1. We can observe that the decoupling capacitor at this location can pull down the resonance to 0.5 Ω. However, when the decoupling capacitor is located at the optimum location, the resonant impedance can be pull down to 0.277 Ω, shown as the solid red curve in Fig.3. The optimized position shows the best results at the resonant frequency 718 MHz compare to the others. The Z_{in} distribution is computed as shown in Fig. 4

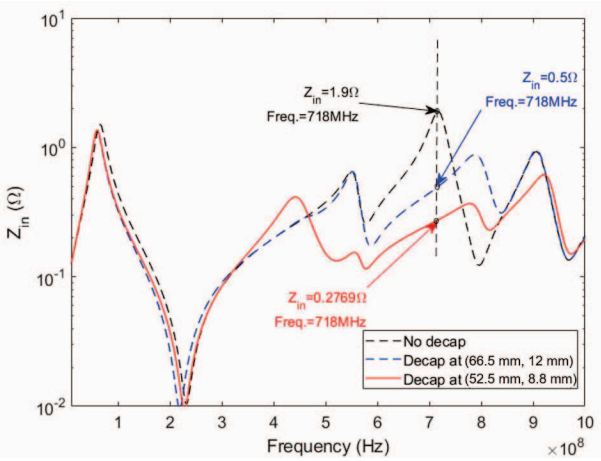

Fig. 3. Z_{in} comparison of different cases of the parallel planes

through the brute-force method for the different positions of the decoupling capacitor. We can observe that the optimum position computed by the proposed method is the same as that computed by the brute-force method, which validates the accuracy of the proposed method in this paper. We can also observe that in the highlighted area, the optimum position is the nearest position to the Port 1.

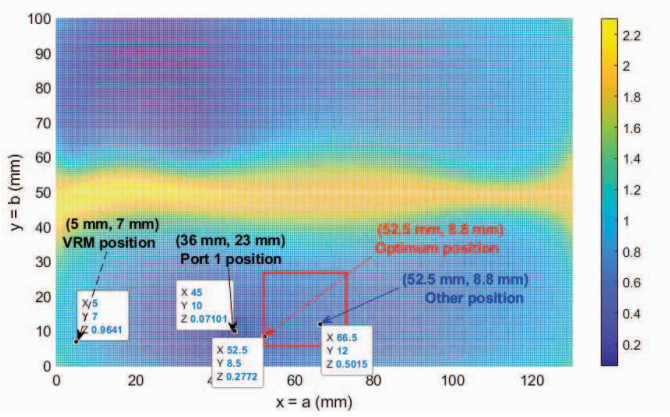

Fig. 4. Z_{in} distribution at 718 MHz with respect to the location of the 1nF decoupling capacitor

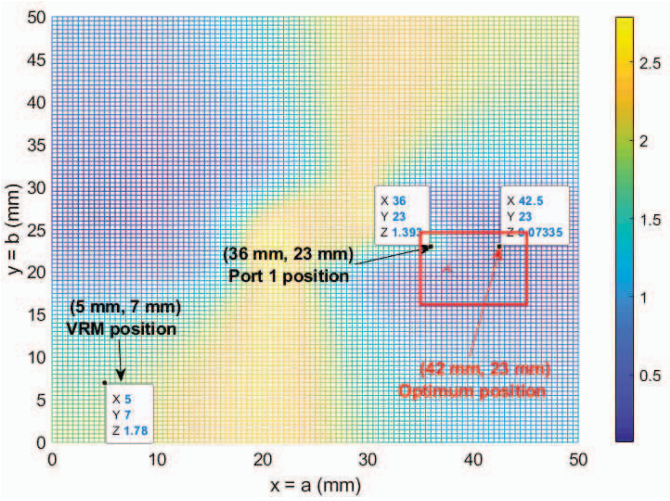

Fig. 5. Z_{in} distribution at 1.42 GHz with respect to the location of the 30 pF decoupling capacitor

However, in another case, it shows that the nearest position to the port is not the best case. The board size a, b, and d are 50 mm, 50 mm and 0.1 mm, respectively. A 30 pF decoupling capacitor with 6 $m\Omega$ ESR and 0.289 nH ESL is used to pull down the impedance of the power/ground plane pair at 1.42 GHz. The Port 1 and VRM are located at (36 mm, 23 mm) and (5 mm, 7 mm), respectively. The rest parameters are the same as the first POC we studied.

The optimum location of this decoupling capacitor, computed by the proposed method, is (42 mm, 23 mm), which is the same as that computed by the brute-force method, as shown in Fig. 5. This optimum position is located in the middle of the highlighted red region, which pulls down the resonant impedance at 1.42 GHz to 0.073 Ω. In addition, points most close to Port 1 in the highlighted red region in Fig. 5 have

a much higher impedance than that when the capacitor is located at the optimum location. It shows that the opinion that capacitors should be placed as close as to the reservation port is not always correct.

IV. Conclusion

We proposed an analytical method for the PDN optimization by combining the cavity model with multi-ports parameters and the Lagrange multiplier method. The mathematical process of the input impedance expression based on cavity model related to coordinates is developed through the Lagrange multiplier method. Two optimization examples are computed with the proposed method, the results compared to the brute-force method proved the efficiency of the method. The opinion of placing the decoupling capacitor as close as possible is proved not always correct. Since we are targeting one decoupling capacitor placement in this paper, the future work will focus on the placement of multi-decoupling capacitors with more complex scenario by covering the PDN cascading, among VRM, PCB, PKG.

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