Signal Integrity and Power Integrity

En-Xiao Liu, Guest Editor

Welcome to the Signal Integrity and Power Integrity Column!

In this issue, I am pleased to recommend the work reported by Biyao Zhao and co-authors on the topic of modeling, analysis, and design of decoupling capacitors (decaps) in multi-layered PCBs.

Designers and researchers in the area of high-speed digital design are not unfamiliar with the I3 phenomena, i.e., Signal Integrity (SI), Power Integrity (PI), and Electromagnetic Interference (EMI). The current paper is about PI by specifically focusing on tackling the issue of the layout design of decaps in advanced PCBs.

The contributions and practical values of this paper are multi-fold. First, an efficient modeling methodology is proposed and demonstrated to quantify the decap interconnect (pin) inductance. In high-speed designs, any component deserves attention, if its physical size is comparable to a significant fraction of the operating wavelength, because it enables the high-speed signal to behave in a dynamic wave nature. The proposed methodology is built on solid formulas, design curves, and circuit models, which facilitates quick and accurate design and what-if studies. An additional benefit is that it offers an intuitive tool for designers to decipher the physics behind the PI phenomenon. Second, leveraging the methodology, the authors propose an approach to guide the layout design of decaps, so as to enhance decap efficacy by tapping on the effect of partial current cancellation. Third, a special scheme of doublet layout of decaps is proposed to dramatically reduce the number of decaps as compared to the conventional layout. Three design cases are provided together with a recommendation of the best scenarios to use for the layout scheme. Last, but not least, the authors present the study of the layout of the power and ground vias for a 3-terminal capacitor. Different layout designs as well as their impact on power integrity are finally demonstrated by using a commercial product.

Enjoy reading!

Decoupling Capacitor Power and Ground Via Layout Analysis for Multi-Layered PCB PDNs[1]

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Abstract—A modeling methodology to calculate the decoupling capacitor interconnect inductance in a multi-layer PCB is proposed herein. The methodology is based on the resonant cavity model of parallel planes. The self-inductance and mutual inductance are extracted to understand the via configuration influence on the effectiveness of decoupling capacitors. A special layout of decoupling capacitor is proposed to increase the effectiveness of the decoupling capacitors by taking maximum advantage of the mutual inductance between interconnect vias with two decoupling capacitors placed in a pair, and two pairs of power and ground vias placed in alternating directions as close as possible. The number of decoupling capacitors needed can be reduced dramatically. Three PCB PDN designs are used to present the effectiveness of doublet layout in different design scenarios. Similar analysis is extended to 3-terminal decoupling capacitor layout design. The decoupling capacitor interconnect inductance of the five via layouts for 3-terminal capacitors is analyzed. The number of decoupling capacitors needed for a commercial product using the doublet layout and 3-terminal capacitor layout is compared to the design with an alternating decoupling capacitor layout to reflect the impact of the decap layout design on the PCB PDN performance.

Keywords— Power distribution network design, PDN impedance, decoupling capacitor layout.

I. Introduction

The power distribution network (PDN) in a printed circuit board (PCB) is a critical part of high-speed digital design. A well-designed PDN is necessary to limit the voltage ripple generated by switching currents to ensure the functionality of the integrated circuit (IC). Failing to meet the charge requirements causes voltage ripple on the power nets [1],[2], which can propagate through the traces, vias and planes, leading to the electromagnetic interfer-

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ence problems, or couple to the nearby signal nets resulting in signal integrity issues [3]-[7].

The maximum tolerable power voltage ripple on a logic power net has reduced significantly with faster communication speeds and lower power voltage levels in new generations of IC technology. Also, the current draw from the IC is increasing due to the higher density and increasing complexity of the circuits on the chip. Designing a good PCB PDN in high-speed digital systems is increasingly more challenging.

The objective of the PCB PDN design is to lower the PDN input impedance below the target impedance to ensure the maximum voltage noise generated is within limits. Surface mounted decoupling capacitors (referred to as "decaps" in this paper) are used to lower the PDN input impedance in a middle frequency range that is typically from a few hundred kilohertz to one- or two-hundred megahertz [8]-[10]. However, there is always a series inductance along the current path to connect the decaps to the IC through vias, pads, and planes, which limits the effectiveness of the capacitors. The decap interconnect inductance is a part of the inductance contribution of the current path from the IC to the decaps in the mid-frequency range. It has a large impact on the input impedance and the effectiveness of decaps when the decap interconnect inductance is a large portion in the equivalent inductance from the IC to the decaps through vias and the power cavity

Decap is generally placed based on the leftover space after routing, together with engineering experience to estimate the number and the placement of decaps for high-layer count PCB PDNs. Many decisions need to be made with regard to the placement of decaps for a high-layer count PCB PDN geometry, such as the side of the PCB to place the decaps, the capacitance value and package size of the decaps, the distance to the IC region, the decap layout, and the number of decaps needed. Every decision contributes to the inductance associated with the current path from the IC to the decaps, and influences the PDN input impedance.

There are several methods that used different optimization methods are used to guide the decoupling capacitance placements [11], [12]. These methods is bounded by the limitation of the mathematical optimization methods. The connection to the physic understanding of the geometry is limited. Here, a physics-based approach is proposed to illustrate the connections between the design details and the PDN input impedance. The current path from the IC to the decaps can be divided into different blocks, and every block can be considered individually from the standpoint of inductance with various decap layouts [8]-[10]. In this paper, extracting the decap interconnect inductance for the impedance equivalent circuit is illustrated. Formulations and a design space are proposed for a quick and accurate estimation of the decap interconnect inductance, for several decap placement patterns and sizes. The design formulas for decap interconnect inductance account for the geometry details to understand and design the decap placement to meet the specifications of the system. Based on the formulas, the mutual inductance between the vias in the decap layout is analyzed. Guidelines for increasing the effectiveness of decaps and reducing the number of decaps needed are detailed based on the extraction and quantification of mutual inductance between the decap interconnect-vias.

A low-inductance decoupling capacitor layout, denoted as doublet, is proposed herein as well. Two decaps are placed in a pair. Two pairs of power and ground vias are added as close as possible in alternating directions in the center of the two decaps to take the advantage of the mutual inductance of the vias carrying opposite directions of current. Three design cases are used to analyze the middle frequency inductance reduction by using the doublet layout to illustrate the effectiveness of the doublet layout in reducing the number of decaps needed to achieve a specified impedance in the PDN design.

The layouts of power and ground vias for a 3-terminal capacitor package are studied following the design insights from the doublet layout. A commercial PCB PDN geometry is used to compare the number of decaps needed to meet a target impedance by using a 3-terminal capacitor, a doublet layout, and an alternating layout. Through the analysis of the inductance components, the influence of the decap layout on the PCB PDN impedance is presented.

The modeling methodology used to calculate the decap interconnect inductance is detailed in Section II. Three design cases are reported in Section III to present the reduction of the middle frequency inductance using the doublet layout in PCB PDNs. In Section IV, 3-terminal decap layouts are analyzed. The doublet, 3-terminal capacitor, and alternating layout are compared using the impedance equivalent circuit model to identify the number of decaps needed to meet the target impedance.

II. L_{PCB_Decap} Modeling & Formulation

A generic multi-layered PCB PDN stack-up with many decaps placed on the top layer of the PCB, the bottom layer away from the IC and the bottom layer under the IC is shown in Fig 1(a). The input impedance looking into the PCB from the IC is often used in PDN analysis, which follows a generic trend as shown in Fig. 1(b) [8]. The decoupling capacitance C_{Decap} is effective in the middle frequency range, and the current comes from the IC port, reaches the power net area fill, spreads across the power net area fill, reaches the decaps and comes back to the power-return using ground vias and planes. The equivalent inductance of this current path is defined as the equivalent inductance L_{PCB_EQ}. At higher frequencies, the plane capacitance C_{Plane} between the power cavity becomes effective and the current only reaches the power cavity and comes back to the port without passing through the decaps. Based on the two current paths, L_{PCB_EQ} can be divided into four blocks, the decap interconnect inductance L_{PCB_Decap}, the inductance above the topmost or bottommost power-return plane L_{above}, the IC interconnect L_{PCB_IC}, and the inductance of current crossing the power net area fill L_{PCB_Plane}.

Adding decaps can reduce L_{PCB_EQ}, L_{PCB_Decap}, and L_{PCB_Plane}. The reduction of the L_{PCB_Decap} depends on the decap via placement patterns, the package size of the decaps, and the thickness

from the decaps to the power cavity (thickness from GND1 to GND3, from GND6 to GND4). The reduction rate of L_{PCB_Decap} to the increase number of decaps is related to the mutual inductance between the vias in the decap layout. An approach to quantifying L_{PCB_Decap} by identifying the influence of the mutual inductance between power and ground vias on the L_{PCB_Decap} reduction of several decap layouts is proposed herein. A special decap layout with power and ground vias placed as close as possible in an alternating directions is emphasized to observe the impact of the mutual inductance between the decap interconnect vias on reducing L_{PCB_Decap}. A reference case is used herein by adding decaps in parallel without considering the mutual inductance, referred to as 1/n. Analytical expressions and design values for four decap placement patterns with four decap sizes are presented to provide references to estimate L_{PCB_Decap} for general designs.

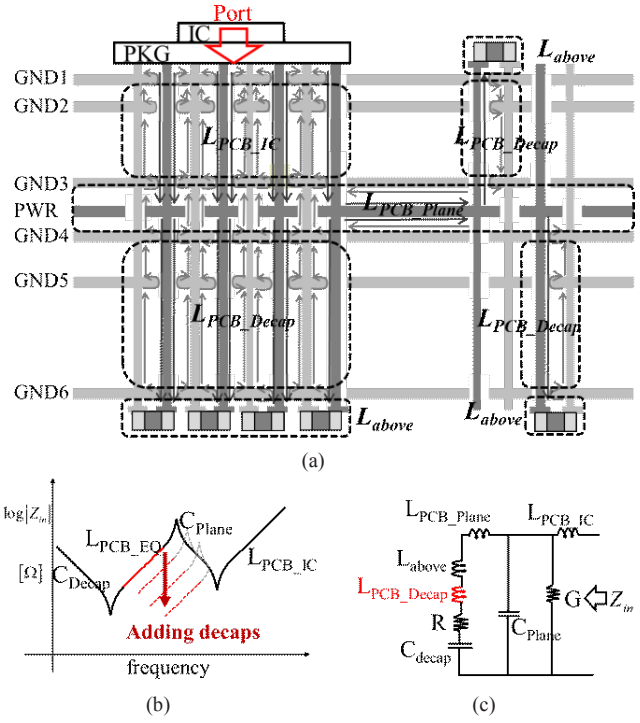


Fig. 1. PDN geometry, input impedance and impedance equivalent circuit model. (a). A stack-up of a high-layer count PCB PDN geometry with a power net fill and inductance definition [13]. (b). The middle frequency range PDN input impedance reduces by adding more decaps. Here, C_{Decap} is the decoupling capacitance from all decaps. C_{Plane} is the plane capacitance from the power cavity. (c). The impedance equivalent circuit model which follows the current paths.

A. L_{PCB_Decap} Formulation

The decap interconnect inductance can be extracted based on the cavity model [14]-[18], as

$$L_{ij} = \frac{\mu h}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{(2-\delta_m)(2-\delta_n)}{k_{mn}^2-k^2} \times\cos\left(\frac{m\pi x_i}{a}\right)\cos\left(\frac{m\pi y_i}{b}\right)\mathrm{sinc}\left(\frac{m\pi W_{xi}}{2a}\right)\mathrm{sinc}\left(\frac{m\pi W_{yi}}{2b}\right) \times\cos\left(\frac{m\pi x_j}{a}\right)\cos\left(\frac{m\pi y_j}{b}\right)\mathrm{sinc}\left(\frac{m\pi W_{xj}}{2a}\right)\mathrm{sinc}\left(\frac{m\pi W_{yj}}{2b}\right) \quad (1)$$

Where, a, b, and h are the dimensions of the cavity along the x, y, and z directions, respectively. The coordinate (x_i,y_i) is the location of the i^{th} port. W_{xi}, and W_{yi} are i^{th} port dimensions along the x and y directions, respectively. The indices m, and n are TM wave mode numbers in the x and y directions, respectively. The permeability and permittivity of the dielectric layer are μ and ε, respectively. The symbols δ_m, and δ_n are the Kronecker delta. The decap interconnect inductance L_{PCB_Decap} is found by placing the ports at the corresponding via locations of the decaps in the power net area fill and shorts at the decap locations, as shown in Fig. 2 (a). The PDN input impedance from cavity model for different PDN applications are compared to simulations and measurements in [9], [10], [17]-[19].

L_{PCB_Decap} is related to the dielectric thickness from the topmost ground to the nearest ground layer in the power cavity. An example is shown in Fig. 2 to explain the circuit model reduction with two decaps placed on the top layer from the physics-based circuit model based on the cavity model. From (1), the inductance is proportional to the height of the cavity. To combine the inductors in the top and bottom cavities, the inductance is scaled to the summation of the cavity heights. The circuit shown in Fig. 2 (b) is then changed to the circuit shown in Fig. 2 (d). Further, the inductors in parallel for power vias and ground vias can be reduced to a single power via and a ground via respectively, as shown from Fig. 2 (d) to Fig. 2 (e). From KVL and KCL, the equivalent inductance for the inductors in parallel is

$$L_{Group} = \left(\sum_{columns}\sum_{rows}[\mathbf{L}]^{-1}\right)^{-1}. \quad (2)$$

After series and parallel reduction, the L_{ij} matrix for the circuit shown in Fig. 2 (e) is written as

$$\mathbf{L}_{Pair} = \begin{bmatrix} L_{PWR} & L_{PWR\_GND} \\ L_{GND\_PWR} & L_{GND} \end{bmatrix}. \quad (3)$$

Here L_{PWR} is the self-inductance of the single power via reduced from all power vias, L_{GND} is the self-inductance of the single ground via reduced from all ground vias, and L_{PWR_GND} is the mutual inductance between the grouped power via and the power-return via. The rigorous calculation for L_{PCB_Decap} is

$$L_{PCB\_Decap} = L_{PWR} + L_{GND} - 2L_{PWR\_GND}. \quad (4)$$

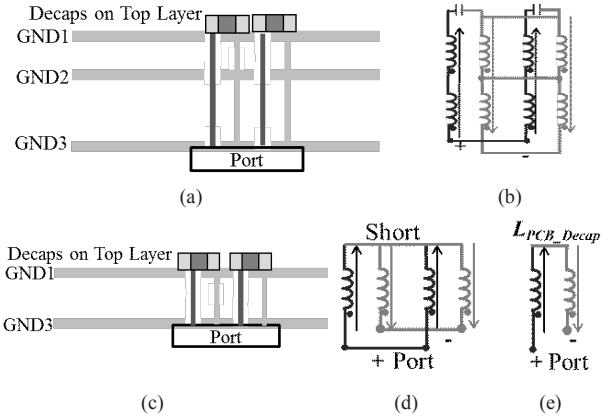


Fig. 2. Physics-based circuit model reduction for the L_{PCB_Decap} calculation based on the cavity model, (a) L_{PCB_Decap} stack-up extracted from a high layer stack-up shown in Fig 2, (b) one-to-one corresponding circuit model for (a), (c) the stack-up after the series reduction applied to the geometry in (a), (d) one-to-one corresponding circuit model for (c), and (e) final reduced equivalent circuit model for L_{PCB_Decap}.

B. L_{PCB_Decap} Modeling Results

Decaps are added around the IC region symmetrically at a distance D, as shown in Fig. 3 (a). Four decap layouts –alternating, aligned, doublet, and shared are used herein, as shown in Fig. 3. The doublet layout includes two decaps placed in pairs and two pairs of power and ground vias. The vias are placed as close as possible in alternating directions in the middle of the two decaps. This configuration maximizes the mutual inductance of the vias carrying opposite directional currents to reduce L_{PCB_Decap}. The case of adding decaps with no mutual inductance (1/n) is used here as a reference. The distance between power and ground vias remains the same as that in alternating and aligned layouts, as shown in Fig. 3(f).

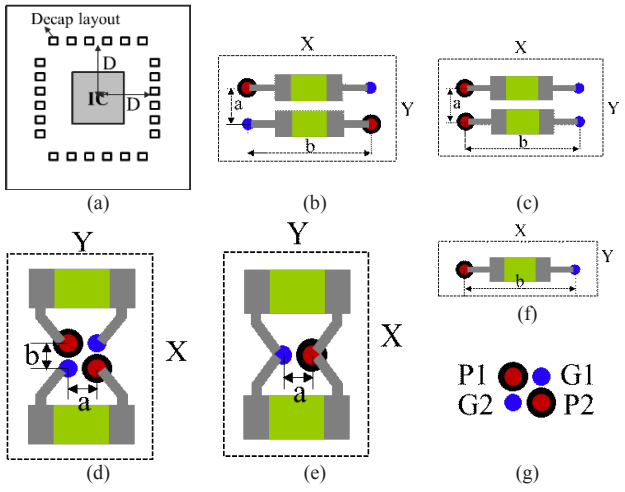


Fig. 3. (a) The decap pairs are added in a line around the IC with the distance D. (b) Alternating layout. (c) Aligned layout. (d). Double layout. (e) Shared layout. (f) Single decap layout. (g). Via definition for the four vias used in one pair of decaps.

The relative position of the power and ground vias in the three decoupling capacitor layouts is different, which influences the current distribution. The details of the relative via locations for different decap layouts and sizes based on the dimensions from Advanced Circuits 4PCB [20] and Electronic Components KEMET [21] are shown in TABLE II with parameters defined in Fig. 3. The drill diameter used in this section is 8 mils. The pad and anti-pad diameters are 16 mils and 25.5 mils, respectively. The minimum distance between the copper shapes from manufacture limitations is 5 mils to calculate the minimum distance for two vias. The board size is 8000 mils by 8000 mils to have enough space to add 32 pairs of decaps.

TABLE I
RELATIVE VIA LOCATIONS AND PACKAGE SIZE ([MILS]) OF THE THREE DECOUPLING CAPACITOR PLACEMENT PATTERNS

Placement pattern	Size	a	b	X	Y
Alternating/ Aligned	0201	45	106.5	132	85
	0402	53	122.5	148	101
	0603	88	193.5	219	171
	0805	108	209.5	235	211
Doublet/ Shared	0201	25.75	25.75	136.5	71
	0402			152.5	87
	0603			222.5	158
	0805			262.5	174

The L_{PCB_Decap} modeling results with the number of pairs of decaps are shown in Fig. 4. The decap to the ground layer above the power layer is 49mils to represent the case with many layers between the decap and the power cavity. The decrease of L_{PCB_Decap} with the number of decap pairs follows a straight line on a log-log plot, for all decap layouts, and the doublet layout has the lowest L_{PCB_Decap}, which is associated with the largest mutual inductance. In Fig. 4(b), only 10 pairs of decaps placed using a doublet layout are needed to reach 34 pH for the L_{PCB_Decap}, while 32 pairs and 16 pairs are required using the aligned layout and alternating layout, respectively.

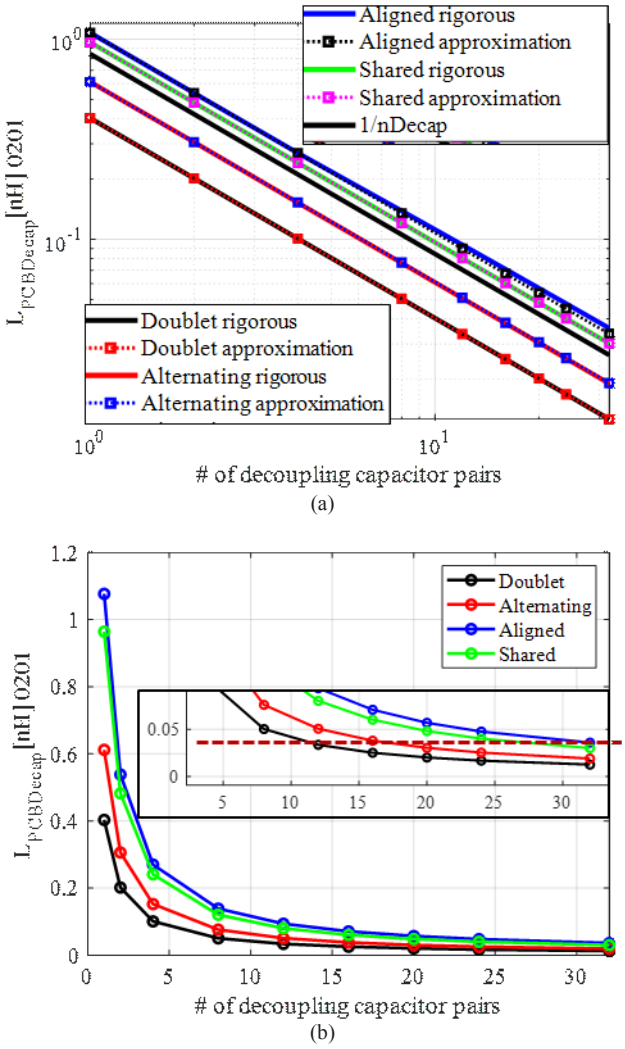


Fig. 4. L_{PCB_Decap} change vs the number of decap pairs. (a) The decrease of L_{PCB_Decap} is a straight line on a log-log plot, (b) The decrease of L_{PCB_Decap} for decaps for 0201 package size.

C. L_{PCB_Decap} Calculation

A quick calculation of L_{PCB_Decap} can be proposed based on the fact that the mutual inductance between the vias in different pairs of decaps is negligible, since the distance between them is much larger than the power and ground vias inside the layout. The mutual inductance between the four vias within one pair dominates the L_{PCB_Decap} calculation. Adding decap pairs can be treated as adding the pairs in parallel without considering the mutual inductances between differ-

ent pairs. The L_{PCB_Decap} can be calculated as the L_{PCB_Decap} of the first pair of the doublet layout divided by the number of pairs as

$$L_{PCB\_Decap} = \frac{L_{PCB\_Decap\_PUL}\,|_{npair=1}}{n_{(decap\ pair)}} \times h\,. \tag{5}$$

Here, $L_{PCB\_Decap\_PUL}$ is the L_{PCB_Decap} when the thickness from the decap to the power cavity is 1 unit. h is the thickness from the decap to the power net area fill, such as the total thickness of different cavities between GND1 and GND3, and between GND4 and GND6 in Fig. 1. The per unit inductance of the first decap pair is calculate from (1) for different decap sizes so that the application of the formula is convenient for general use.

The inductance matrix for the four vias is calculated using (1), and then KCL and KVL are applied to the four vias to calculate the L_{PCB_Decap} for the first pair. The voltages and currents for the two power/ground vias are assumed to be the same. The definition of the via names is shown in Fig. 3 (g). The voltage and current relationship can be expressed as

$$\begin{bmatrix} L_{P1} & M_{P1G1} & M_{P1P2} & M_{P1G2} \\ M_{P1G1} & L_{G1} & M_{P2G1} & M_{G1G2} \\ M_{P1P2} & M_{P2G1} & L_{P2} & M_{P2G2} \\ M_{P1G2} & M_{G1G2} & M_{P2G2} & L_{G2} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_1 \\ V_2 \end{bmatrix}, \tag{6}$$

where, I_2=-I_1, and I_1 and I_2 are the currents of the one power via and one power-return via, respectively. Here, V_{Decap}=V_1-V_2, V_{Decap} is the voltage across the unit cell, and V_1 and V_2 are the voltages of power and power-return vias, respectively. L_{Pi} is the self-inductance of the i^{th} power via, i=1,2. L_{Gi} is the self-inductance of the i^{th} power-return via, i=1,2. M_{PiPj} is the mutual inductance of the i^{th} power via and j^{th} power via, i=1,2, j=1,2. M_{PiGj} is the mutual inductance of the i^{th} power via and jth power-return via, i=1,2, j=1,2. L_{PCB_Decap} is calculated as

$L_{PCB\_Decap} = V_{Decap}/(2I_1)$. Solving the matrix, L_{PCB_Decap} for one pair of decaps is calculated as

$$L_{PCB\_Decap\_PUL}\,|_{n_{(decap\ pair)}=1} = \frac{1}{2}(L_P + L_G - 2M_{PG} + M_{P1P2} + M_{G1G2} - M_{P1G2} - M_{P2G1}) \tag{7}$$

Each inductance shown in (7) is calculated from (1). The validation of the quick calculation is shown in Fig. 4(a). L_{PCB_Decap} has a good match with rigorous calculations using (1)-(4) with all mutual inductances included, which indicates that the mutual inductances between the decap pairs can be neglected.

A table of the L_{PCB_Decap} per unit length for the three layouts using the dimensions shown in TABLE I is given in TABLE II. From (7), only the L_{PCB_Decap} for the first pair of decaps is needed for a quick calculation of total L_{PCB_Decap}.

TABLE II.
THE LPCB_DECAP [PH] PER MIL OF ONE DECAP PAIR FOR THE THREE DECAP LAYOUTS OF DIFFERENT PACKAGE SIZES

$L_{PCB\_Decap\_PUL}\|_{npair=1}$	Aligned	Alternating	Doublet	Shared
0201	20.8	11.3	6.8	17.3
0402	21.4	11.8	6.8	17.3
0603	23.4	14.6	6.8	17.3
0805	23.4	15.5	6.8	17.3

D. Mutual Inductance Influence in L_{PCB_Decap}

The decrease rate of L_{PCB_Decap} regarding to the increase of decaps is related to the mutual inductance between vias. The mutual inductance influence can be explained using (7). For the Shared layout, L_P+L_G-2M_{PG} is the calculation for the L_{PCB_Decap} for the first pair. The term M_{P1P2}+M_{G1G2}-M_{P1G2}-M_{P2G1} is the total mutual inductance contribution between four vias of two decaps in a pair. In alternating and doublet layouts, the mutual inductances M_{P1G2} and M_{P2G1} are larger than M_{P1P2} and M_{G1G2}. The mutual term M_{P1P2}+M_{G1G2}-M_{P1G2}-M_{P2G1} is negative. Similarly, for the aligned layout, the mutual inductance term is positive. The mutual inductances in the three layouts and the effect on L_{PCB_Decap} are shown in TABLE III.

TABLE III.
THE SELF AND MUTUAL INDUCTANCES IN THE ONE DECAP PAIR FOR THE THREE DECAP PACKAGES IN SIZE 0201 [PH]

	Aligned	Alternating	Doublet	Shared
L_P+L_G	3277.9	3265.5	3274.9	3274.9
M_{P1P2}+M_{G1G2}	2138.2	1672.6	2248.0	0
M_{P1G2}+M_{P2G1}	1672.6	1709.5	2428.9	0
M_{PG}	854.8	1063.0	1213.0	1213.0
M_{P1P2}+M_{G1G2}-M_{P1G2}-M_{P2G1}	465.6	-36.9	-181	0
L_{PCB_Decap}	1017.0	551.3	334	848.9

There are two design changes that lead to the inductance reduction using the doublet layout. From (7), the doublet layout adds a second loop by adding another pair of power and ground vias. The other change is from the mutual inductance. The mutual inductance is related to the distance between two vias. Since the distance between the power vias to the ground vias is closer than that between the power vias or the ground vias in the doublet layout, M_{P1P2} and M_{G1G2} are smaller than M_{P1G2} and M_{P2G1}. Then, M_{P1P2}+M_{G1G2}-M_{P1G2}-M_{P2G1} is a negative value. Due to these two reasons, the L_{PCB_Decap} is reduced by more than a half by using the doublet layout as compared to the aligned and shared via layouts.

E. L_{PCB_Decap} Measurement

A test vehicle was developed and two-port VNA measurements were performed to validate the formulation. The test vehicle contains two stack-ups, as shown in Fig. 5. The inductance difference in the mid-frequency range between the two fixtures is L_{PCB_Decap}. The use of the two fixtures enables the inductance to be in the measurable range of the VNA with high accuracy. The large thickness of 40 mils is used to increase the difference between the inductance of the two fixtures to improve accuracy. The accuracy of two-port measurement for PCB PDN is included in [19]. Due to manufacturing limitations, the dimensions b and a in Fig. 3 are 120 mils and 60 mils for the alternating and aligned layout. For the doublet layout, a=b=39 mils. The drill diameter used is 15 mils. The board size is 1000 mils by 750 mils to reduce the layout area. The L_{PCB_Decap} per mil is shown in TABLE IV. L_{PCB_Decap} is calculated from Z-parameters. The thickness h is 40 mils. The simulation and measurement results compare favourably with the rigorous formulation results from (1)-(4).

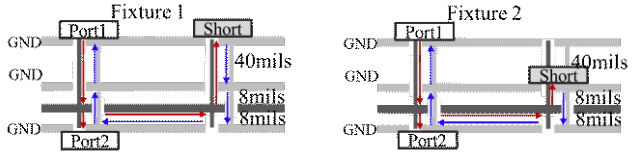


Fig. 5. Stack up details of the test vehicle cases. The current paths for the two cases are labeled. (a). The short is placed on the top GND layer. (b). The short is placed on the second GND layer.

TABLE IV
THE SIMULATION AND MEASUREMENT RESULTS FOR ONE AND TWO PAIRS OF DECAPS IN THREE LAYOUTS. [pH/mil]

	# of pairs	Formulas	CST	Measurement
Alternating	1	10.6	10.8	10.7
	2	5.3	4.9	4.6
Aligned	1	18.7	18.3	18.4
	2	9.3	8.7	9.2
Doublet	1	7.2	7.0	7.0
	2	3.6	3.6	3.2
Shared	1	17.8	17.6	17.1
	2	8.9	8.7	8.2

III. L_{PCB_DECAP} Design

The effectiveness of adding decaps varies in different PCB designs. Three design cases are used in this section to analyze the effectiveness of using the doublet layout.

A. Design Cases

The L_{PCB_EQ} reduction by replacing the decap layout using the doublet layout can be analytically expressed. The L_{PCB_EQ} of the original design can be written as the summation of the inductances from different blocks, as

$$L_{PCB\_EQ} = L_{PCB\_IC} + L_{PCB\_Plane} + L_{PCB\_Decap} \quad (8)$$

Here, L_{above} is not considered since the decaps are treated as shorts. By changing the decap layout to the doublet layout, L_{PCB_Decap} and L_{PCB_Plane} are reduced by β and γ. Then the L_{PCB_EQ} using the doublet layout is

$$L'_{PCB\_EQ} = L_{PCB\_IC} + (1-\beta)L_{PCB\_Decap} + (1-\gamma)L_{PCB\_Plane} \quad (9)$$

Define the L_{PCB_Decap} percentage in the original design as

$$\alpha = \frac{L_{PCB\_Decap}}{L_{PCB\_EQ}} = \frac{L_{PCB\_Decap}}{L_{PCB\_IC} + L_{PCB\_Plane} + L_{PCB\_Decap}} \quad (10)$$

Then L_{PCB_IC} can be expressed as

$$L_{PCB\_IC} = \frac{(1-\alpha)L_{PCB\_Decap} - \alpha L_{PCB\_Plane}}{\alpha} \quad (11)$$

The L_{PCB_EQ} reduction percentage is

$$\frac{L_{PCB\_EQ}\ \text{reduction}}{\text{percentage}} = \frac{L_{PCB\_EQ} - L'_{PCB\_EQ}}{L_{PCB\_EQ}} = \alpha\beta + \alpha\gamma\frac{L_{PCB\_Plane}}{L_{PCB\_Decap}} \quad (12)$$

From (12), the L_{PCB_EQ} reduction percentage is related to L_{PCB_Decap} percentage in L_{PCB_EQ}, L_{PCB_Decap} to L_{PCB_Plane} ratio, and the reduction of L_{PCB_Decap} and L_{PCB_Plane}. The L_{PCB_EQ} reduction percentage can reflect the effectiveness of using doublet layout in a PCB PDN design.

Three cases are designed to generate different L_{PCB_Decap} percentage α in L_{PCB_EQ} using two stack-ups as shown in Fig 6, and two different numbers of IC vias. One stack up (Stack-up 1) is shown in Fig. 6(a) with the power layer in the middle of the stackup and decaps on the top layer. The current comes from the IC, directly passes across the power-net area fill to reach the decaps and comes back to the IC through the nearby ground planes. The equivalent inductance L_{PCB_EQ} comes from L_{PCB_Plane} and L_{above}, according to the definition shown in Fig. 1(a). In Stack-up 2 shown in Fig 6 (b), the power net area fill is buried deeper in the stackup and is far away from the decaps on the top layer. The current comes from the IC, goes through the vias in the IC region to reach the power cavity, then passes across the power plane and the vias in the decap region, and comes back to the IC through ground vias and planes, as shown in Fig. 6(b). When the plane is far away from the decaps, the inductance contribution from L_{PCB_IC} and L_{PCB_Decap} is significant. Two IC pin numbers are used in the design cases, with one pair of power and ground vias, as shown in Fig. 7 (a) and Fig. 7 (b), and 256 pairs of power and ground vias, as shown in Fig. 7 (c). Multiple power and ground vias add multiple parallel current paths in the IC region, which can reduce the L_{PCB_IC} significantly.

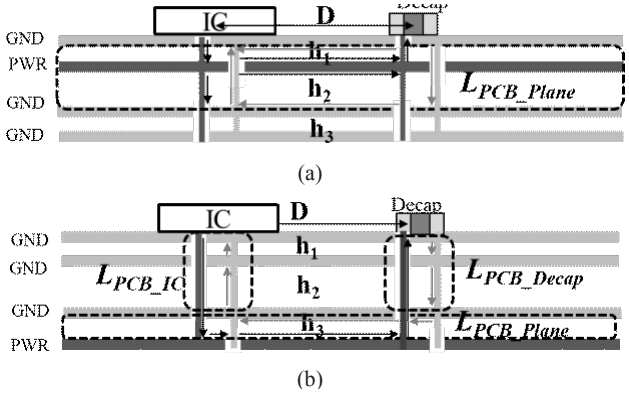


Fig. 6. Two different stack-ups extracted from the complete PCB stack-ups so that the dominant component is clear to enlarge the difference of various types of PCB PDNs. The two stack-ups are only the commonly used portions in PCB PDN stackups. (a) Stack-up 1, with the power plane close to the decoupling capacitors placed on the top layer, (b) Stack-up 2, with power plane at the bottom layer far away from the decoupling capacitors.

The effectiveness of using the doublet layout is analyzed for the three cases. Here, the shared layout is selected as the original design. Other layouts can be analyzed in a similar way. Case 1 uses Stack-up 1 with one pair of power and ground vias for the IC. Here, L_{PCB_Plane} is the dominant component in L_{PCB_EQ}. Case 2 uses Stack-up 2 with one pair of power and ground vias for the IC. L_{PCB_Decap} and L_{PCB_IC} has a larger portion in L_{PCB_EQ} due to the large thickness from the decap and IC to the power cavity. Case 3 uses Stack-up 2 with 256 pairs of power and ground vias for the

IC. The large number of IC vias reduces L_{PCB_IC} so that it is a negligible contribution to L_{PCB_EQ}, and L_{PCB_Decap} is the dominant component in L_{PCB_EQ}. In all design cases, decoupling capacitors are added gradually around the IC at a distance D symmetrically as a square, as shown in Fig. 7 (b).

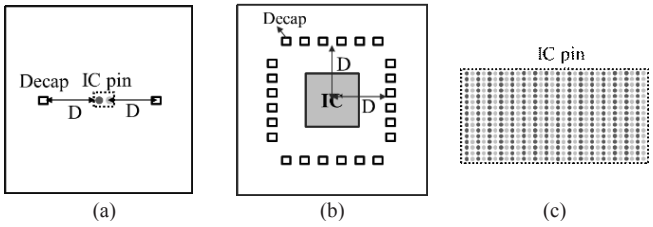


Fig. 7. Adding the decoupling capacitors (decap) gradually at distance D symmetrically around the IC (port) with (a) Case 1 with two pairs of decaps, with one pair of power and ground vias, (b) Case 2 with 8 pairs of decaps, with one pair of power and ground vias, and, (c) Case 3 with 256 pairs of power and ground vias. The square shown in the figures represents the doublet layout footprint or the shared-via footprint.

B. L_{PCB_EQ} Results

The circuit model extracted from the first-principles cavity model is used to calculate L_{PCB_EQ}. The default dimensions for the stackup used in this section are h_1=9 mils, h_2=40mils, and h_3=9mils. The decoupling capacitors are assumed to be in size 0402. The board size is 6 inches by 6 inches and the center-to-center distance of the decap layout to the IC region is 1.5 inches. The L_{above} is ignored with the capacitors shorted in the circuit model, since it is detailed in [22]. The decap via locations follow TABLE I. The center-to-center distances between nearby decap pairs are 300 mils along the x and y directions.

The L_{PCB_EQ} extracted from the PDN input impedance for the three cases shown with different numbers of capacitor pairs are shown in Table V, Table VI and Table VII. The reduction percentage of L_{PCB_EQ} using the doublet layout is defined as the ratio of the inductance reduction by using the doublet layout to the L_{PCB_EQ} of the shared layout. CST simulation is applied to validate the inductance extraction from the cavity model. From TABLE V and Table VI, the L_{PCB_EQ} using the cavity model has less than 8% difference to that from CST simulation.

Using the doublet layout can lower the equivalent inductance in all cases. And in some cases, only half of the decoupling capacitors are needed to reach a similar L_{PCB_EQ} by using the doublet layout. For example, in Case 2, only four pairs of capacitors are needed for the doublet layout with L_{PCB_EQ} to be approximately 1nH. While, eight pairs of capacitors are need in the shared-via layout. Comparing L_{PCB_EQ} reduction of the three cases, the reduction of L_{PCB_EQ} using doublet layout is the largest in Case 3, and the smallest in Case 1. Also, in Case 1 and Case 2, the inductance reduction is larger when the number of capacitor pairs is smaller. While, the reduction is consistent in Case 3 with different number of decaps.

TABLE V.
L_{PCB_EQ} [pH] FOR CASE 1

# of pairs	Cavity Model Shared	Cavity Model Doublet	Cavity Model Reduction	CST Shared	CST Doublet
1	480.1	439.9	8.4%	503.5	462.8
2	339	312.6	7.8%	356.4	334.6
4	273.3	261.8	4.2%	294.3	280.7
8	258	253.2	1.9%	277.2	271.9
16	246.5	242.1	1.8%	266.1	262.8
32	237.1	235.2	0.8%	258.5	256.6

The difference of L_{PCB_EQ} reduction percentage with the increase of decaps can be analyzed following the dominant inductance component in L_{PCB_EQ} and (12). In Case 1, the L_{PCB_EQ} all comes from L_{PCB_Plane} since L_{above} is not considered here. There is no L_{PCB_Decap} and the reduction percentage by using doublet layout is the lowest. In Case 2 and Case 3, the decap to the power cavity thickness is large, and L_{PCB_Decap} is significant. The difference between Case 2 and Case 3 is the number of IC vias used. When the number of IC vias is 256, L_{PCB_IC} is reduced to the level that it is negligible in L_{PCB_EQ}, which increases the L_{PCB_Decap} percentage in Case 3 as compared to that in Case 2. Thus, the reduction percentage in Case 3 is larger than that in Case 2.

TABLE VI.
L_{PCB_EQ} [pH] FOR CASE 2

Pair #	Shared L_{PCB_EQ}	Shared L_{PCB_Plane}	Shared L_{PCB_IC}	Shared L_{PCB_Decap}(%L_{PCB_EQ})	Shared CST	Doublet L_{PCB_EQ}	Doublet L_{PCB_Plane}	Doublet L_{PCB_IC}	Doublet L_{PCB_Decap}	Doublet CST	Reduction
1	1877.1	249	862.8	731.9 (39%)	1819.2	1466.9	183.9	862.8	294.6	1475.4	21.9%
2	1395.9	186.8	862.8	365.9 (26.2%)	1359.2	1193.5	157.9	862.8	147.3	1188.1	14.5%
4	1171.4	159.1	862.8	183 (15.6%)	1141.4	1070.8	145.7	862.8	73.7	1049.2	8.6%
8	1078.4	145.3	862.8	91.8 (8.5%)	1063.6	1032.4	139.5	862.8	36.56	1019.6	4.3%
16	1031	138.4	862.8	46.1 (4.5%)	1007.8	1006.9	136.2	862.8	18.2	992.7	2.3%
32	1003.6	138.4	862.8	23.15 (2.3%)	982.9	991.6	134.6	862.8	9.1	980.4	1.2%

TABLE VII.
L_{PCB_EQ} [pH] FOR CASE 3

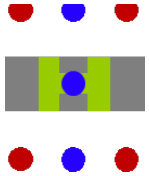
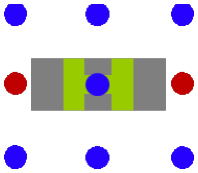
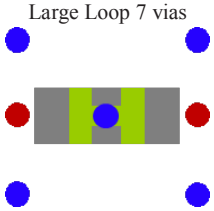
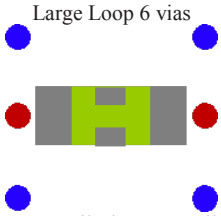
Pair #	Shared L_{PCB_EQ}	Shared L_{PCB_Plane}	Shared L_{PCB_IC}	Shared L_{PCB_Decap}	Doublet L_{PCB_EQ}	Doublet L_{PCB_Plane}	Doublet L_{PCB_IC}	Doublet L_{PCB_Decap}	Reduction
1	841.8	117.9	2.7	731.9	332.1	52	2.7	294.6	60.5%
2	397.8	57.8	2.7	365.9	166	26	2.7	147.3	58.3%
4	197.8	29.5	2.7	182.98	83.3	13.9	2.7	73.7	57.9%
8	104.1	15.9	2.7	91.8	46	7.3	2.7	36.56	55.8%
16	53.8	8.3	2.7	46.1	24.6	3.9	2.7	18.2	54.3%
32	29.5	4.8	2.7	23.16	13.8	2.1	2.7	9.1	53.2%

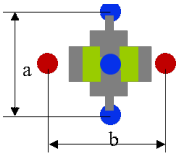
IV. Multi-terminal Decoupling Capacitors

Multi-terminal decoupling capacitors are used in PDN designs to reduce the number of decaps needed. From previous analysis, changing the decap via placement and number of vias is effective when L_{PCB_Decap} is a large fraction of L_{PCB_EQ}. The idea for using multiple vias in the layout design from doublet to maximize mutual inductance can be used to design the footprints for multi-terminal decaps. In this section, different via placements for decaps are analyzed and L_{PCB_Decap} is calculated.

A typical footprint for a 3-terminal capacitor is shown in Fig. 8, and is referred to as Large Loop normal layout. The dimensions for 0805 sized 3-terminal decap are a=90.6mils, and b=102.4 mils. The L_{PCB_Decap} is 110.3 pH when the decap to power cavity thickness is 10 mils. The drill diameter is 8 mils. The antipad diameter is 25.5 mils. Several other via layouts are proposed by adding more parallel current paths and minimizing the distance between power and ground vias, as shown in Table VIII. The Small Loop design adds two extra power vias. The power vias are moved closer to the ground vias to maximize the mutual inductance between the power and ground vias. The Large Loop 9 vias layout adds extra ground vias to reduce the distance between the power and ground vias. The distance between the extra ground vias to the original ground vias is set to be large to decrease the mutual inductance between ground vias. The Large Loop 7 vias layout removes the top and bottom original ground vias to further enlarge the distance between the ground vias. The Large Loop 6 vias removed all original ground vias to check the need of ground vias in the center. The L_{PCB_Decap} for the four 3-terminal in 0805 size when the thickness from the decap to the power cavity is 10 mils is included in TABLE VIII. The L_{PCB_Decap} of Small Loop layout is the smallest, and it increases with larger distance between power and ground vias, and the reduction of vias used in the layout. The comparison of the different cases for L_{PCB_Decap} with the doublet layout, and 1/n is shown in Fig. 9. The L_{PCB_Decap} of doublet layout is smaller than that of 3-terminal decap using Large Loop 7 vias and Large Loop 6 vias layouts.

TABLE VIII
THE L_{PCB_DECAP} FOR 3-TERMINAL CAPACITOR STUDY WITH DIFFERENT LAYOUTS

Name	Small Loop	Large Loop 9 vias
Layout		
Dimension 1 decap	a=90.6 mils, b=78.8 mils $L_{PCB\_Decap\_10mils}$ = 69.2 pH	a=90.6 mils, b=102.4 mils $L_{PCB\_Decap\_10mils}$ = 77.9 pH
Name	Large Loop 7 vias	Large Loop 6 vias
Layout		
Dimension 1 decap	a=90.6 mils, b=102.4 mils $L_{PCB\_Decap\_10mils}$ = 81.0 pH	a=90.6 mils, b=102.4 mils $L_{PCB\_Decap\_10mils}$ = 89.1 pH



a=90.6 mils, b=102.4 mils
$L_{PCB\_Decap\_10mils}$ = 110.3 pH

Fig. 8. Footprint of a 3-terminal capacitor [23], Large Loop normal layout.

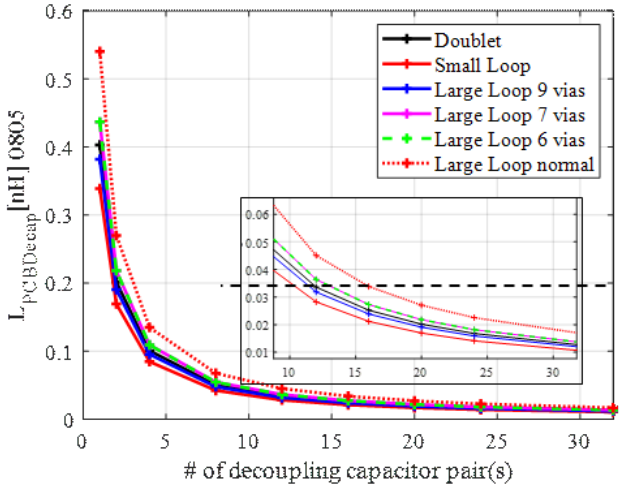
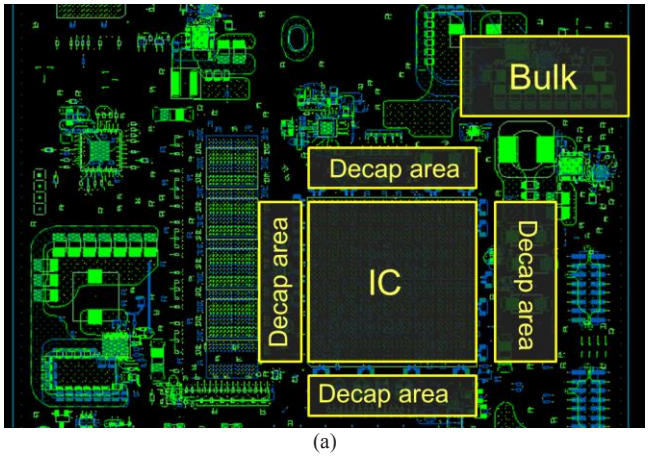
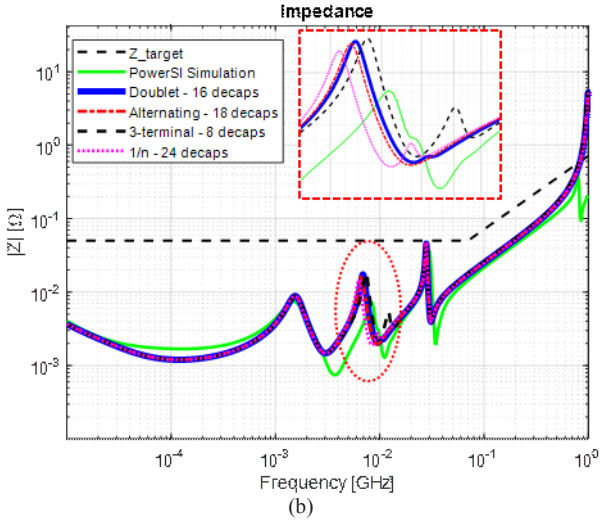


Fig. 9. L_{PCB_Decap} change with the number of decaps using five 3-terminal decap layouts and doublet layout.

The number of decaps needed for PDN designs can be analyzed based on the impedance equivalent circuit model in Fig. 1(c). A IC in a commercial product with power plane in the middle of a 12-layer stackup is used to analyze the number of decaps needed to meet the target impedance. The top view of the product used for the calculations is shown in Fig. 10(a). The IC is placed on the top layer of the PCB. There are 123 power vias and 236 ground vias used for this IC, and L_{PCB_IC} is 7.6 pH. There are 24 bulk capacitors added on the top layout and bottom layer. And 60 decaps are added under the IC. To meet the target impedance, additional decaps need to be added around the IC in the decap area shown in Fig. 10(a). Here, the alternating layout, doublet layout and 3-terminal in Large Loop normal layout are used to assess how many additional decaps are needed for this design. The target impedance is set to be 50 mΩ below 70 MHz. L_{above} for the three layouts is modelled using CST with the decap to ground layer height to be 10 mils. The L_{PCB_Decap} PUL value for this PCB and L_{above} is shown in TABLE IX. The doublet layout has the smallest L_{PCB_Decap} PUL value and the 3-terminal capacitor layout has the smallest L_{above} value. The number of decaps needed to meet the target impedance using the alternating layout, doublet layout and 3-terminal decap is 18, 16 and 8. The PDN input impedance from cavity model and impedance equivalent circuit model [24] looking in to the PCB at the IC terminals for the 3 layouts with decaps around the IC is shown Fig. 10(b). The PDN input impedance for all the designs meets the target impedance.



(a)



(b)

Fig. 10. (a) Top view of the commercial PCB PDN geometry. The decap area blocks is the area that can be used to add decaps around the IC. (b). PDN input impedance that meets the target impedance using different decap layouts.

TABLE IX
L_{PCB_DECAP} AND L_{ABOVE} FOR THE THREE DECAP LAYOUTS USED IN THE COMMERCIAL PCB PDN

	L_{PCB_Decap} PUL	L_{above}	# of decaps needed
Alternating	16.8 pH	577.7 pH	18
Doublet	8.3 pH	748.9 pH	16
3-Terminal	11.1 pH	134.1 pH	8
1/n	19.9 pH	891.4 pH	24

V. Discussions and Conclusions

A modeling methodology to quantify the decap interconnect inductance is proposed in this paper. Based on the methodology, an approach to guide the design the decap layout to increase the effectiveness of using decaps is proposed. Mutual inductance with opposite current directions can be used to increase the effectiveness of decaps and reduce the number of decaps needed. The advantage of this method is that the geometry details can be pre-designed quickly and accurately based on formulas, design curves, and circuit models.

A special decoupling capacitor layout is proposed to increase the effectiveness of decaps. The advantage of this layout comes from adding extra parallel current loops and maximizing the mutual inductance between the vias carrying current in opposite directions. The number of decoupling capacitors needed can be dramatically reduced using the doublet layout. Three design cases are used to illustrate the effectiveness of using doublet layout in different design scenarios. A recommendation is to use the doublet layout to reduce the number of decoupling capacitors needed when the power net area fill is in the middle of the stack-up and L_{PCB_Decap} is the dominant inductance contribution in L_{PCB_EQ}. The analysis of effectiveness of using doublet layout can be extended to other decap layouts.

The layout for the power and ground vias for a 3-terminal capacitor is also studied, and the inductance L_{PCB_Decap} was calculated for this via layout and compare to the alternating and doublet layouts. Reducing the current loop dimensions and increasing the number of parallel current loops can reduce the L_{PCB_Decap}. The PCB PDN of a commercial product is included to reflect how the decap layout design influences the PCB PDN design. Doublet layout and 3-terminal capacitor layout are compared to alternating layout to identify the number of decaps needed to meet the target impedance, and can be used to lower the number of decaps needed.

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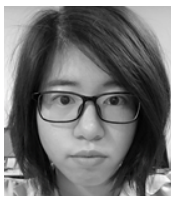
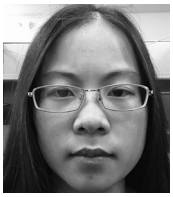
Biographies



Biyao Zhao *(S'14) received the BSEE from Huazhong University of Science and Technology, Wuhan China, in 2014, and the MSEE and PhD from the Missouri University of Science and Technology (MST), Rolla, USA, in 2016 and 2020, respectively. Her current research interests include system-level power distribution network modeling and design, signal integrity analysis, and power integrity analysis for 3-D integrated circuits. Ms. Zhao was a recipient of the 2017 IEEE EMC Society President's Memorial Award, the Best SI/PI Student Paper Award at the IEEE EMC Symposium, Raleigh, NC, USA, 2014, and the Best SI/PI Paper Award at the IEEE EMC Symposium, Washington, DC, USA, 2017.*



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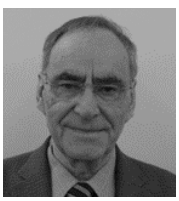
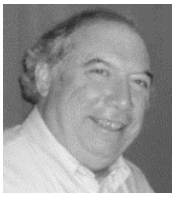
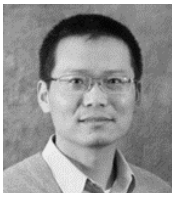


Albert Ruehli *(M'94–LF'05) received his Ph.D. degree in Electrical Engineering in 1972 from the University of Vermont, Burlington, and an honorary doctorate in 2007 from the Lulea University in Sweden. He is a Life Fellow of the IEEE and a member of SIAM. He is now an Emeritus of IBM Research and an adjunct professor in the EMC area at the Missouri University of Science and Technology. He is the editor of two books, Circuit Analysis, Simulation and Design (New York, North Holland 1986, 1987), and coauthor of a book, Circuit Oriented Electromagnetic Modeling using the PEEC Techniques. He is author or coauthor of over 250 technical papers.*



Bruce Archambeault *(M'85–SM'99–F'05) received the B.S.E.E. degree from the University of New Hampshire, Durham, NH, USA, in 1977, the M.S.E.E. degree from Northeastern University, Boston, MA, USA, in 1981, and the Ph.D. degree from the University of New Hampshire, in 1997, all in electrical engineering. Previously he was an IBM Distinguished Engineer with IBM, Research Triangle Park, NC, USA. Dr. Archambeault is a member of the Board of Directors for the IEEE EMC Society and a past Board of Directors member for the Applied Computational Electromagnetics Society. Currently he is the immediate past President of the IEEE EMC Society and an adjunct professor in the EMC area at the Missouri University of Science and Technology.*



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James L. Drewniak *(F'07) is a Curator's Professor of Electrical and Computer Engineering at the Missouri University of Science and Technology. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign. His research is in electromagnetic compatibility, signal and power integrity, and electronic packaging.* **EMC**

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