Differential Via Designs for Crosstalk Reduction in High-Speed PCBs

Junda Wang[#1], Chaohui Xu[#2], Shuai Zhong[#3], Siqi Bai[#4], JongJoo Lee[#5] and DongHyun Kim[#6]
[#]Missouri University of Science and Technology
Rolla, MO, USA.
[1]jwb9d@mst.edu, [2]cxfdc@mst.edu, [3]szyc7@mst.edu, [4]sb2pc@mst.edu,
[5]jlcbf@mst.edu, [6]dkim@mst.edu

***Abstract*—With an increased data rate of high-speed PCBs, an increase in crosstalk degrades the signal integrity of the high-speed system. In most PCB designs, via-to-via coupling has the largest impact on crosstalk. Until now, multiple PCB design methods for crosstalk mitigation are proposed under the IC pin field area, such as increasing the distance between signal pairs, adding more ground vias in between the signal vias and placing signal pairs orthogonal to each other. However, such methods sacrifice the signal to ground (S:G) ratio and require a change in the IC package ball map. In this paper, two different via designs are proposed to reduce crosstalk without sacrificing the S:G ratio, while maintaining the package ball maps. In the first proposed design, crosstalk is mitigated through tilted drilling, where the vias are drilled with 45 degrees angle on the PCB. Differential via pairs located in different rows achieves orthogonality for crosstalk cancellation when viewed from the horizontal cross-section. In the second proposed design, additional intermediate vias are designed to achieve orthogonality between differential via pairs without changing the IC package ball map or the drilling direction. Using a 3D full-wave simulation tool, the two prosed designs are simulated. Simulation results demonstrate that both designs decrease in crosstalk with negligible change in insertion loss and return loss compared to the conventional via design up to 30 GHz range. The proposed methods can be directly applied to lower the crosstalk in the existing high-speed PCBs with minor adjustments in the PCB design while maintaining the same IC packages.**

***Keywords*—Crosstalk, ICN, differential pair, tilted drill, orthogonality, pin map.**

I. Introduction

With the rapid increase of data rate in modern electronic devices and systems, signal integrity (SI) and electromagnetic compatibility (EMC) issues are also becoming more problematic[1]-[9]. Crosstalk is one of the major concerns in high-speed channels. In the PCB trace region, crosstalk can be shielded by placing stitching vias along traces. For the crosstalk mitigation in the ball grid array (BGA) pin field region, adding more ground vias between signal vias or increasing the spacing between signal vias can reduce crosstalk[10]. Even though such methods effectively lower the crosstalk, due to limited space in the BGA pin field region, pacing more vias or spacing out the vias may be costly or physically impossible with current PCB manufacturing techniques. Previously, the orthogonal layouts have been proposed to lower the crosstalk, without increasing the S:G ratio [11], [12]. However, for the practical implementation of such layouts, chip vendors must change the package to adopt the new orthogonal BGA.

In this paper, new via designs are proposed to decrease the crosstalk in PCB without sacrificing any S:G ratio or changing the chip package. The first method is the crosstalk reduction by tilted orthogonal via and the second method is the intermediate orthogonal via layout. For the first method, differential vias are tilt drilled. Differential pairs in different rows are drilled with 45 degrees with opposite drilling direction. Therefore, two pairs form orthogonality, which theoretically, mitigates crosstalk. The second applies the orthogonal layout in the inner layer of PCB away from the crowded BGA pin field region, the top layer is identical to the conventional pin pattern. Both of the proposed methods allow existing chip package design to be used while reducing the crosstalk in the PCB.

ICN is firstly introduced in IEEE 802.3ba standard [13] to evaluate the crosstalk in the high-speed PCB as a substitute for insertion loss to crosstalk ratio (ICR) [11]. ICN is the weighted summation of crosstalk noise in the frequency domain concerning the power spectrum of the signal being transferred [14] and it's been used as the crosstalk assessment index in this paper. Section II introduces the principle and 3D modeling of the tilted via. The intermediate orthogonal layout is discussed and analyzed in section III . Both of the proposed methods are compared to the conventional layouts and the crosstalk cancellation effectiveness is verified in section IV.

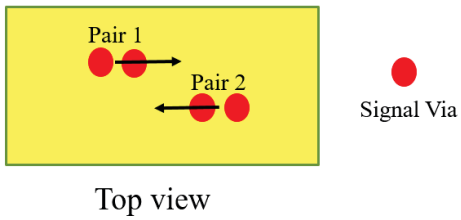
II. Differential Crosstalk Cancellation by Tilted Orthagonal Via

Crosstalk in the pin field area of PCB is dominated by parallel vias. Mutual inductance exists between parallel differential via pairs, resulting in noise coupling between one pair to another. To mitigate such crosstalk, the drilling direction of differential vias can be set to 45 degrees, so that the vias are no longer parallel to each other. With the crossing angle of 90 degrees between two differential pairs, crosstalk between the orthogonally crossing vias will achieve crosstalk cancellation.

Fig. 1 depicted the principle of crosstalk cancellation of the tilted orthogonal via. Pair 1 and pair 2 are two pairs of differential vias, pair 1 drilling rightwards and 2 drilling leftwards with 45 degrees from the top view. The cross-section shows that orthogonality formed between two pairs.

Based on the proposed crosstalk cancellation principle, 3D modeling of the full pin map is designed. The full pin map is shown in Fig. 2, there are 9 differential pairs in the model as marked, blue arrows in the figure indicate the drill direction, pairs 1, 2, 4, 5, 7 and 8 drilling leftwards and pairs 3, 6 and 9 drilling leftwards with 45 degrees, differential pairs

in one row are always orthogonal to pairs in another adjacent row, crosstalk between adjacent rows can be mitigated.



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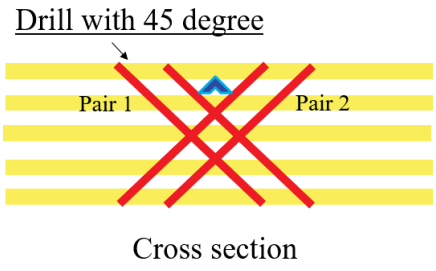


(b)

Fig. 1. Illustration of tilted orthogonal via: (a) top view; (b) cross-sectional view.

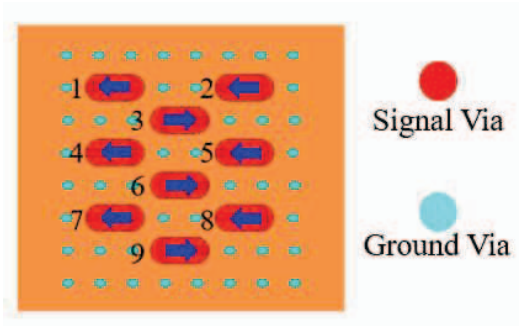
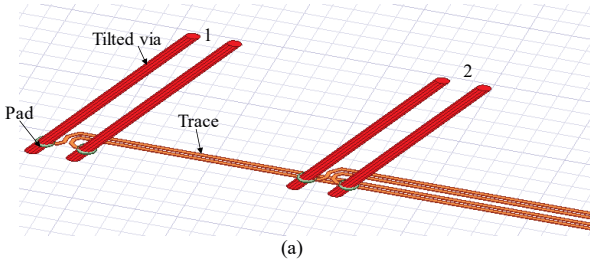
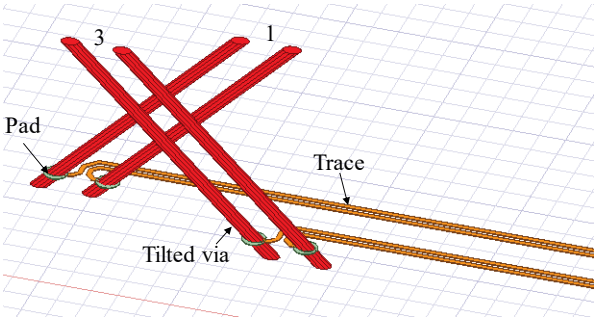


Fig. 2. Top view of the 3D model with tilted orthogonal via.

Stripline traces are added to the 3D model for the evaluation of the crosstalk level. Fig. 3 (a) shows the via-pad-trace interconnection of the differential pair 1 and 2 in Fig. 2. Both pairs are drilled with 45 degrees towards the left side, pair 1 and pair 2 route in two different layers to avoid overlap of traces and both of them route in a deep layer to make sure the crosstalk cancellation can be magnified. Fig. 3 (b) shows two pairs drilling in different direction, which corresponding to pair 1 and 3 in Fig. 2. The vias have the radius of 5 mils and traces are 3.75 mils. The edge-to-edge separation of the traces are 3 mils. The vias are backdrilled as the industry usually do for high-speed signals.



(a)

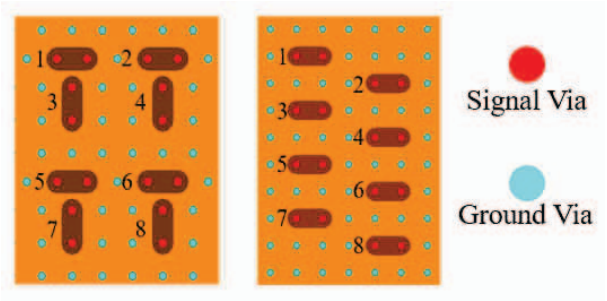


(b)

Fig. 3. (a) Tilted via with trace routing; (b) cross-sectional view of trace added model.

III. Differential Crosstalk Cancellation by Intermediate Orthogonal Layout

Fig. 4. shows a comparison between the orthogonal PCB layout and the conventional PCB layout. The conventional chip package matches the only pin array of the conventional PCB layout. To make use of the orthogonal layout, different chip package design is required.



(a) (b)

Fig. 4. (a) Orthogonal layout; (b) Conventional layout.

In the newly proposed design, the orthogonal layout is utilized by the additional intermediate via. Fig. 5 shows using an additional intermediate via layout. In the BGA/pin region, the pin pattern keeps the same as the conventional design, vias are rerouted in the inner layer of PCB through the intermediate trace and the conventional pin map is converted to the orthogonal pin map. The short via under the BGA pin field must be kept as short as possible to reduce crosstalk. Build-up vias can be utilized for the short vias.

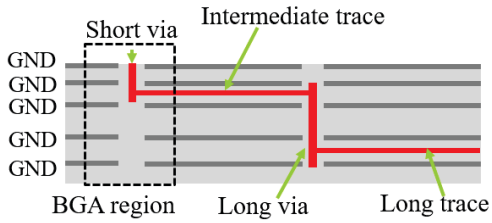


Fig. 5. Crosstalk Cancellation by Intermediate Orthogonal Layout.

The 3D model of the additional intermediate orthogonal layout is shown in Fig. 6. Four differential pairs are shown in the figure, including short vias in the BGA region, long orthogonal intermediate via, and short trace in between. The board thickness is 135 mils, the via radius is 5mil, and the trace width and spacing are 3.75 mils and 3 mils, which are

the same as the previous section. To reduce discontinuity, 2 mils advanced backdrill is applied on the bottom of the BGA region, and the top and bottom of the intermediate via. Trapezoidal dumps in the trace are for the skew compensation.

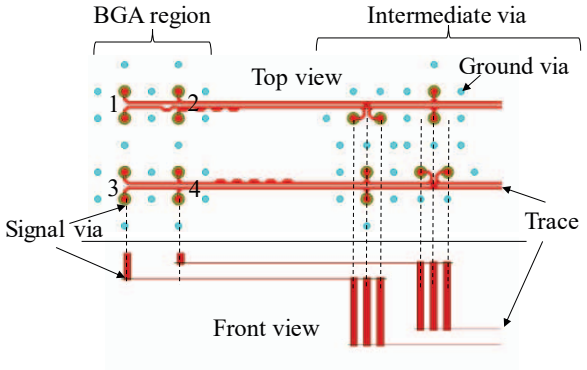


Fig. 6. Intermediate orthogonal layout modeling, top view and front view.

IV. Analysis of Advanced Via Designs for Crosstalk Reduction

A. Analysis on Differential Crosstalk Reduction in Tilted Orthogonal Via

To analyze the crosstalk cancellation of the tilted orthogonal via, the proposed full-wave model of the tilted orthogonal via with trace routing in Fig. 3 needs to be compared with the conventional via with trace routing which has the same S:G ratio. Fig. 7 shows the modeling of the conventional via with trace routing. The conventional via design drill vias directly from the top to the bottom. The modeled conventional via with trace routing has the same pin pattern and board thickness as the tilted orthogonal via with trace routing, both of the two models are routed in the same layer and vias are backdrilled equally, board width in two models are identical which means both two models have the same trace length and models simulated under the same configuration.

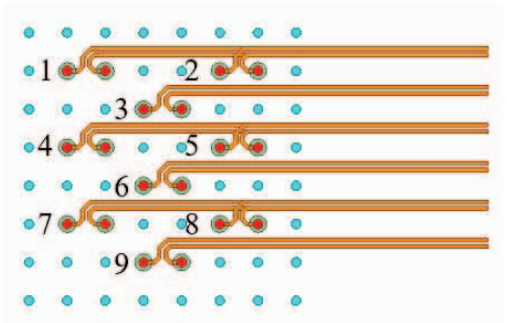
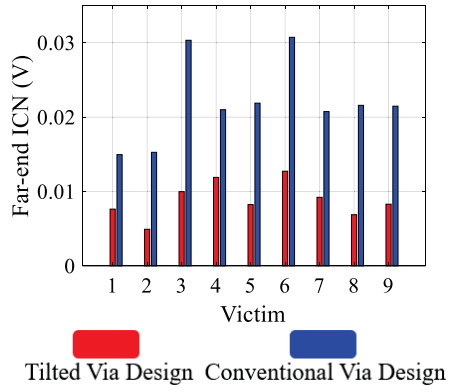


Fig. 7. Conventional via with trace routing.

ICN comparisons up to 30Gbps between two different designs are shown in Fig. 8. It can be seen clearly that for both the far-end and near-end ICNs, tilted orthogonal via design reduces crosstalk at every single pair and it results in approximately 50% ICN reduction compared to conventional via design. Tilted orthogonal via design efficiently reduces crosstalk.



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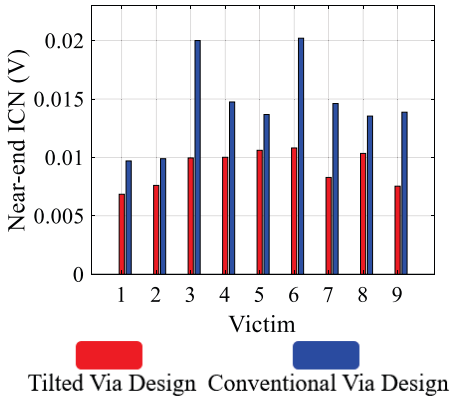
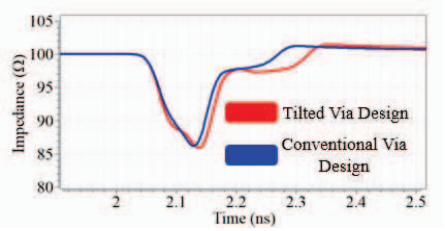


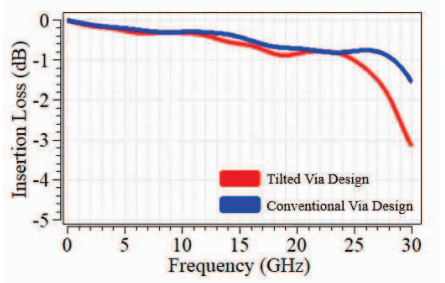
(b)

Fig. 8. ICN comparisons up to 30Gbps: (a) Far-end; (b) Near-end.

The characteristic impedance, insertion loss and return loss of pairs in two different designs also compared to make sure the only variable in the comparison is the drill methodology and reduction of crosstalk will not affect other signal integrity performances. Fig. 9 demonstrates that characteristic impedance, insertion loss and return loss of two models are comparable. The tilted orthogonal via design will reduce the crosstalk without sacrificing signal integrity performances.



(a)



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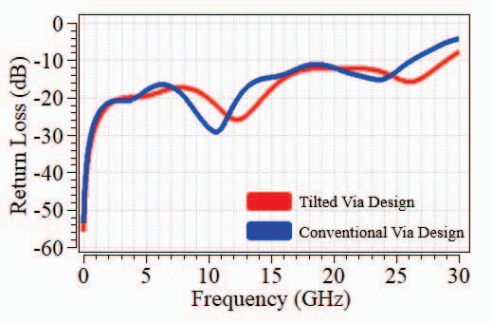


(c)

Fig. 9. Tilted via design vs. Conventional via design: (a) Characteristic impedance; (b) Insertion loss; (c) Return loss.

B. *Crosstalk Mitigation by Intermediate Orthogonal Layout Verification*

To verify the intermediate orthogonal layout for crosstalk cancellation, the intermediate orthogonal layout is compared to the conventional layout which the differential vias drills directly from the top to the bottom in the PCB. Fig. 10 shows the conventional layout modeling. Differential pairs as marked in the plot. The trace routing layer of differential pairs in the models is the same as it routed in the intermediate orthogonal layout model.

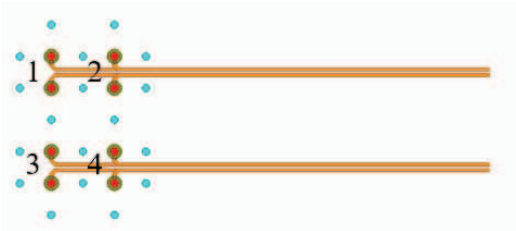
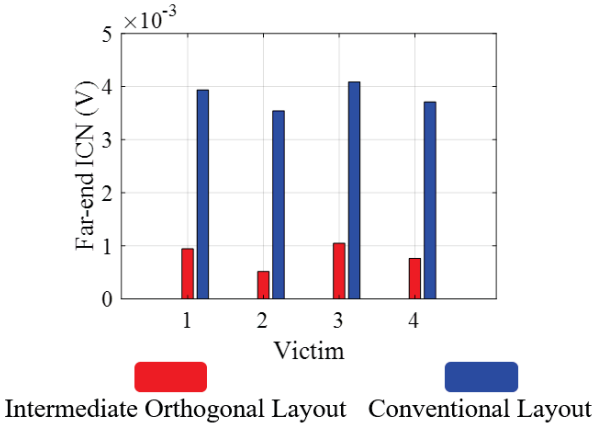
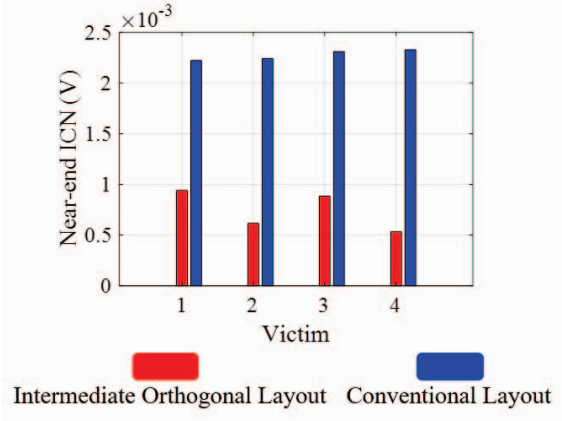


Fig. 10. Conventional layout.

Fig. 11 demonstrated the ICN comparison between two designs up to 30Gbps. As expected, the intermediate orthogonal layout has reduced ICN for both far-end and near-end. The intermediate orthogonal layout canceling crosstalk through via placement orthogonality in the inner layer of PCB, in the top of PCB, the conventional pin pattern is still maintained. The intermediate orthogonal layout mitigates crosstalk without changing the chip package.



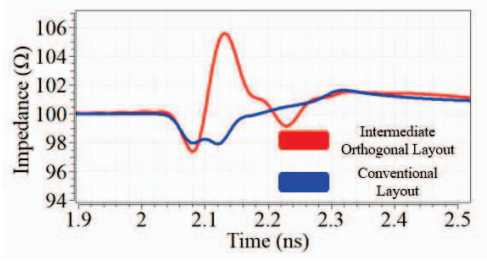
(a)



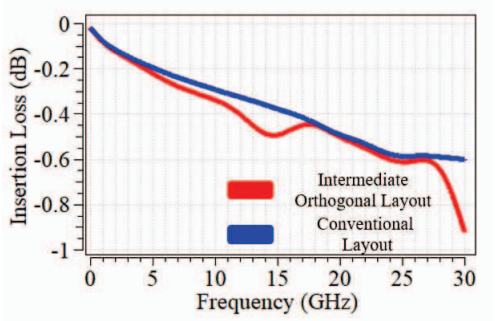
(b)

Fig. 11. ICN comparisons up to 30Gbps: (a) Far-end; (b) Near-end.

Fig. 12 shown the characteristic impedance, insertion loss and return loss comparisons of differential pairs between the intermediate orthogonal layout and the conventional layout. The objective of comparing characteristic impedance, insertion loss and return loss between these two designs is to make sure the improvement of crosstalk in the intermediate orthogonal layout won't sacrificing any other signal integrity performances. The spike in the characteristic impedance of intermediate orthogonal layout pairs caused by the dumps in the trace routing. The impedance mismatch also caused the increase of the return loss at low frequency but the return loss level is still acceptable. Apart from the impedance mismatch of few ohms and the acceptable increase in return loss, pairs in the intermediate orthogonal layout have similar characteristic impedance, insertion loss and return loss as pairs in the conventional layout. Although the extra discontinuity of the intermediate orthogonal via introduces an insertion loss deviation, the amount is small, only 0.1 dB, which is acceptable. The proposed intermediate orthogonal layout method reduces crosstalk without sacrificing signal integrity performances.



(a)



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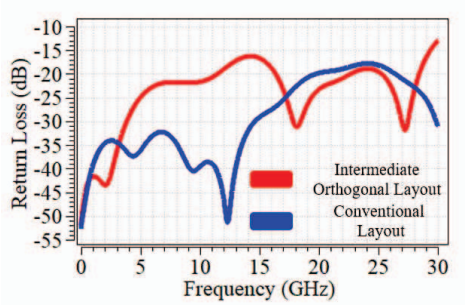

(c)

Fig. 12. Intermediate Orthogonal Layout vs. Conventional Layout: (a) TDR; (b) Insertion loss; (c) Return loss.

V. Conclusion

The tilted orthogonal via and intermediate orthogonal layout are proposed in this paper to mitigate the crosstalk without sacrificing any S:G ratio and changing the chip package design. Reduction in crosstalk in the two proposed designs are verified by the ICN comparison up to 30Gbps. In addition to ICN comparison, the characteristic impedance, insertion loss and return loss of the new designs have been verified that the improvement on the crosstalk will not degrade the signal integrity performances.

References

[1] L. Zhang *et al*., "Sparse Emission Source Microscopy for Rapid Emission Source Imaging," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 59, no. 2, pp. 729-738, April 2017.

[2] J. Xu, L. Zhang, M. Sapozhnikov and J. Fan, "Application of Deep Learning for High-speed Differential Via TDR Impedance Fast Prediction*," IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity*, 2018, pp.645-649.

[3] J. Li *et al*., "EMI coupling paths in silicon optical sub-assembly package," *2016 IEEE International Symposium on Electromagnetic Compatibility,* Ottawa, ON, 2016, pp. 890-895.

[4] Y. Guo, D. Kim, J. He, X. Ye, A. Sutono, V. Kunda, A. Luoh, Z. Kiguradze, L. Shen, and J. Fan., "Robust EUL crosstalk characterization techniques for high-speed interconnect," *Asia-Pacific Electromagnetic Compatibility Symposium 2020 (APEMC).* 19-22 May 2020, Sydney, Australia.

[5] J. He *et al.*, "Extracting characteristic impedance of a transmission line referenced to a meshed ground plane," in *2016 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2016, pp. 651-656: IEEE.

[6] J. He et al., "An Integer Programming Application for PCB Stack-up Arrangement," in *2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+ SIPI),* 2019, pp. 432-436: IEEE.

[7] Z. Xu, R. Blaise, and M. Olivier, "Multiphysics Tensorial Network Analysis Applied to PCB Interconnect Fatigue Under Thermal Cycle Aggression," *IEEE Transactions on Electromagnetic Compatibility* 61.4 (2019): 1253-1260.

[8] Q. Wang *et al.*, "Effectiveness analysis of de-embedding method for typical YSV pairs in a silicon interposer," in *Proc. IEEE 23rd conf. Elect. Perform. Electron. Packag. Syst.,* 2014, pp. 239-242.

[9] C. Wu, B. Chen, T.S. Mikheil, X. Ye, and J. Fan, "Error bounds analysis of de-embedded results in 2X Thru de-embedding methods," in *Proc. IEEE Int. Symp. Electromagn..Compat. Signal/Power Integrity*, 2017, pp.532-536.

[10] J. Lim *et al.*, "ASIC package design optimization for 10 Gbps and above backplane SerDes links," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 2012, pp. 199–204.

[11] B. Chen, S. Pan, J. Wang, S. Yong, M. Ouyang, Y. S. Cao, Y. Wang, H. Deng and J. Fan, 'Differential Far-end and Near-end Crosstalk Mitigation in the Pin Field Area of SerDes Channel with Trace Routing Guidance', *IEEE Transactions on Electromagnetic* Compatibility 61, no. 4(2019): 1385-1394.

[12] B. Chen, M. Ouyang, S. Yong, Y. Wang, Y. Bai, Y. Zhou and J. Fan, "Integrated Crosstalk Noise (ICN) Analysis among Multiple Differential BGA and Via Pairs by Using Design of Experiments (DoE) Method," in Proc. *IEEE Int. Symp. EMC*, Washington, DC, USA, Aug. 7-11, 2017, pp. 112-117.

[13] IEEE 802.3ba Std-2010, IEEE, 2010.

[14] B. Chen *et al*., 'Differential Integrated Crosstalk Noise (ICN) Mitigation in the Pin Field Area of SerDes Channel', in Proc. *IEEE Int. Symp. EMC 2018*, Long Beach, CA, USA, pp. 533-537.