IC Pin Modeling and Mitigation of ESD-Induced Soft Failures

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***Abstract*—In this article, electrostatic discharge (ESD) induced soft failures (SFs) of a USB3 Gen1 device are investigated by direct transmission line pulse injection with varying pulsewidth, amplitude, and polarity to characterize the failure behavior of the interface and to create a SPICE model of the voltage and current waveform dependent failure thresholds. ESD protection by transient-voltage-suppression diodes is numerically simulated in several configurations. The results show viability of using well-established hard failure mitigation techniques for improving SF robustness. A good agreement between numerical simulation for optimized board design and measurements are achieved. A novel concept of SF system efficient ESD design is proposed and demonstrated to be effective for making decisions during early product development, in board designing and prototyping phase.**

***Index Terms*—Circuit model, electrostatic discharge (ESD), SEED, soft failure (SF), SPICE, transmission line pulse (TLP).**

I. Introduction and Overview

ELECTROSTATIC discharge (ESD) induced soft failures (SFs) have been a subject of extensive investigations [1]–[10]. Many studies concentrate on empirically characterizing complex systems, some on studying simpler devices such as 16-bit microcontroller units or simpler flip-flop structures and modeling them in detail with full-wave and circuit solvers in order to understand the root cause of specific failures [1]–[3]. Sophisticated characterization techniques are required in order to study each interface of a complex interface, such as USB3 SuperSpeed [4]–[8]. Often, the root cause of such a failure lies in noise and glitches on power rails as a result of direct or indirect ESD [3]–[5]. In most practical situations, however, the system is very complex and it is either impractical or too time consuming to study and model each interface at a high level of detail (i.e., individual registers and voltages for every node) before being able to propose, test and release a more robust design for ESD-induced SF.

System-efficient ESD design (SEED) is a well-established concept in the industry [9], [10]. It stands for the design optimization methodology that maximizes robustness of signal lines to ESD-induced hard failures (damage) by simulating the high current behavior of PCB components. Typically, a measurement-based victim pin model is created, and then combined with other parts that affect ESD robustness: transmission lines, discrete components, interconnects, etc. Design changes are made in the model and evaluated in terms of stress at the victim pin, compared to the damage thresholds. Common protection schemes include adding discrete components (TVS diodes, CM chokes, etc.) that are placed at different locations within the interface under test. The damage thresholds of the victim are evaluated through measurement or provided by device vendors. The process continues until the maximized robustness levels are achieved in simulation, then implemented in practice.

To date, there has been discussion of SEED concept for SF, but no implementation or validation was presented [4], [6]. This work aims to demonstrate that such concept is viable and to validate it by testing and modeling a range of commonly used hard failure mitigation techniques.

The methodology is applied to SuperSpeed lanes of a USB3 Gen 1 interface. A directional injection concept is developed for the high-speed interface and used to characterize the RX pins of the device under test. An automated test system is used to characterize the victim pin and classify the failure modes related to the interface. The characterization results are presented as SF likelihood as a function of injected stress levels, polarity, and rise time. This is an extension of a characterization methodology developed previously [7], [8]. Eight failure modes across four severity levels are identified for the device under test (DUT). This information is, then, used to create a circuit model that outputs failure the likelihood for the applied stress.

The rest of this article is organized as follows. Section II of this article contains DUT pin characterization setup, procedure, and the results. Section III describes pin modeling methodology and SF modeling methodology. Section IV proposes a SEED-like simulation procedure for SFs. Section V provides evidence for viability of the proposed procedure and discusses the results. Section VI gives an outlook and a direction of further improvement of the methodology. Finally Section VII concludes this article.

Manuscript received February 13, 2020; revised April 28, 2020; accepted May 30, 2020. This work was supported by the National Science Foundation under Grant IIP-1916535. *(Corresponding author: Giorgi Maghlakelidze.)*

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Digital Object Identifier 10.1109/TEMC.2020.3011544

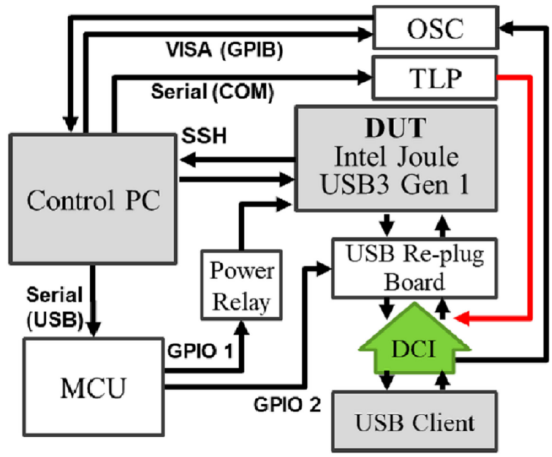

Fig. 1. System diagram of the characterization setup. The control PC communicates with the TLP measurement system over GPIB and COM, controls a MCU via serial, and interfaces with DUT by SSH over LAN.

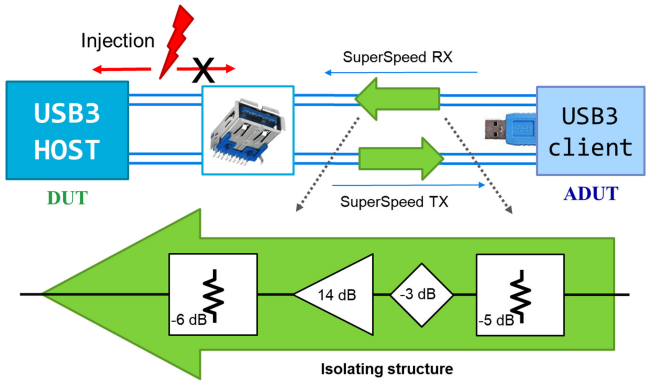

Fig. 2. Isolation concept for DCI. The reverse direction of the structure absorbs the stress and prevents it from propagating towards the USB3 client.

II. Characterization Methodology and Results

A. Automated Setup Description

The goal of this setup is to characterize an I/O pin of an active device in terms of SF modes and thresholds under direct stress injection. This is achieved by running a series of automated stress tests, varying stress parameters, and then statistically processing the resulting data.

Most devices of the setup are controlled by a computer via several common interfaces (general purpose interface bus IEEE-488 (GPIB), communication port (COM), local area network (LAN), and secure shell (SSH)). The system diagram is given in Fig. 1. A standard transmission line pulse (TLP) measurement system is used to apply repeatable stress to the DUT pin and measure voltage and current transient waveforms [16].

A detailed description of the process algorithm and the system is given in [7]. For cohesion, a summary is provided below. The DUT is an Intel Joule system. It consists of two parts: a "compute module" (SoC, WiFi module, and eMMC) and an "expansion board" (interface fanout, PDN, ESD protection, filters, etc.). The two boards plug in through a 100-pin HRS surface-mount SF40 interconnect.

The TLP pulses are injected into the active USB3 Gen1 interface SuperSpeed data lines of the DUT, without significant loading of the USB3 Gen 1 signal. This is achieved by using a low-capacitance TVS diode soldered at the point where TLP output connects to the data pin [11].

The injection point is located on the directional current injection (DCI) board. The structure allows to direct the current into the host (DUT in this case), while protecting the client on the other end.

B. Directional Current Injection Board

For purposes of SF characterization, it is important to determine whether the host or the client of the high-speed link fails, and the interface must be active.

When a stress pulse is injected into a DUT, the current spreads in both directions from the entry point. Due to the complexity of a typical system, it is difficult to determine whether the host or client failed. Moreover, if the host is the DUT, different clients may introduce unwanted vendor-to-vendor variation. Thus, directional current injection structures are developed. The passive circuit is effective and provides 60:1 directionality of the DUT current for serial links under 1 GHz bandwidth [12]. For USB3 Gen 1 and higher or other high-speed data protocols, a new concept is proposed.

The concept as applied to USB3 Gen 1 Type A is illustrated in Fig. 2. An isolation structure placed in series with the signal path. The directionality is facilitated by a flat-gain amplifier MMIC. Before and after the amplifier, resistive attenuators are placed. The system is designed to achieve the total gain of ~ 0 dB in the relevant frequency range for the target technology. For USB3 Gen1 the target channel data rate is above 5 Gb/S, for higher datarates an equalizer can be added. However, no equalizer was used in the fabricated isolation structure.

Under the frequency range of 2.5 GHz, the differential insertion loss in the isolation structure less than 5 dB. The stress current injected at the output side of the isolation structure is split: most of the current propagates towards the victim pin, while a small part is dissipated in the attenuator and the amplifier output terminal.

Fig. 3 shows the measurements performed on the test structure with a 100 ns TLP, in order to establish the effectiveness of the proposed design. The results show that DUT is subjected to 90% of the total current from the TLP. 10% is dissipated in the isolation structure, while only several mA of current arrives at the protected (ADUT) side.

The SF tests are only performed up to a few amperes to avoid hard fails. The amplifier must be selected appropriately and stress levels should be well-controlled to avoid damage.

C. Characterization Process and Outcome

Typical characterization process starts by powering the system, calibrating TLP test system, and establishing an active link. Then, a characterization loop proceeds to sweep injected stress

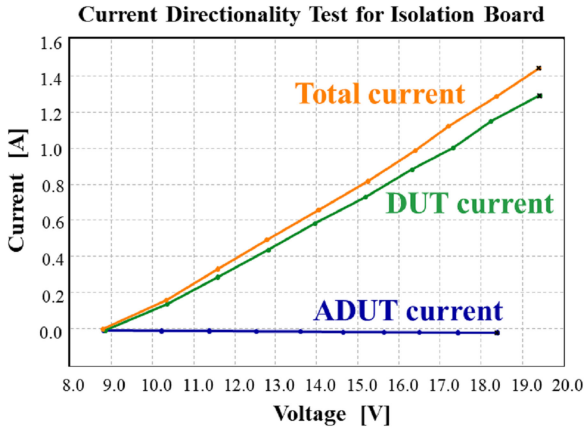

Fig. 3. Current directionality when injecting at the DCI board. 90% of the current propagates towards the DUT. The protected side is isolated by the reverse direction of the amplifier, so milliamps of currents are detected at the ADUT side of the link path.

TABLE I
SOFT FAILURE CATEGORIES

Cat.	Visible	Action Needed	Failure Examples for USB3
A	✗	✗	Bit errors; packets are resent
B	✓	✗	Drop in data throughput; re-enumerated by the host
C	✓	✓	Stop of data transfer; re-plugging of the cable or power cycling required
D	✗	✓	Device re-enumerates, but latch-up is unnoticed and power cycling is required

levels and polarity. For each injection, the following steps are taken as follows:

1) reset the DUT to nominal state;
2) inject stress into the target pin;
3) measure transient current and voltage waveforms;
4) diagnose the SF mode based on the kernel logs;
5) log the data and proceed to the next stress level.

More intricate details of the process are described in [7] and [8].

After the completion of pulse length and polarity sweep, the data are processed and grouped. The SFs are grouped and categorized by two traits: visibility and whether any action is needed by the user in order to resolve the error.

Table I contains the summary and examples of SFs and categories the different SF modes in the process of USB3 host characterization.

The failure likelihood depending on the injection level is illustrated in Fig. 4 for an USB3 SuperSpeed RX positive pin. The likelihood is calculated as a ratio between the number of failures and the total number of times the stress was injected. The characterization results show that both for positive and negative stress injections, there is a sharp threshold after which failure rate

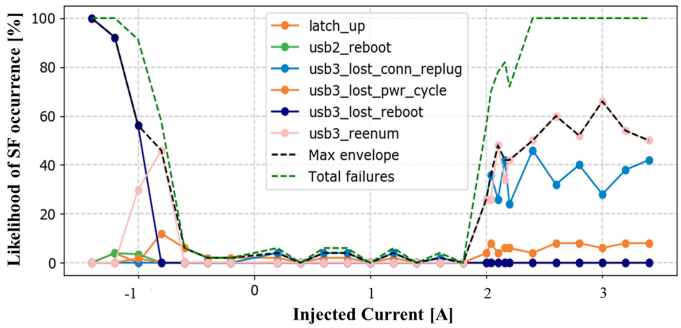

Fig. 4. SF characterization results for SSRX_P pin for 100 ns. The interface is more susceptible to negative stress, as indicated by the low 100% failure threshold, as compared to the positive half of the plot.

is total of 100%, as shown by the dashed green curve. The victim is more prone to failure for negative polarity stress, as compared to positive. Failure modes for positive stress injections are split into three types as follows:

1) USB3 client re-enumerates within the host operating system and continues functioning (failure category B);
2) USB3 client disappears from the host operating system and the failure is fixed by replugging the client (failure category C);
3) latch-up at one of the power domains that presents as persistent power drain, which requires a complete power cycle to fix (failure category D).

The latch-up is detected by using an on-die power monitor [8].

Negative polarity pulses cause similar SFs, but with higher severity. These include the following:

1) USB3 re-enumerations;
2) USB3 client disappears from the host, but requires a system software reboot to fix (bringing power down not required);
3) USB interface falls back to USB2 mode and requires software reboot;
4) USB3 client disappears from the host and requires a full power cycle in order to fix the SF.

The latter failure mode is one of the more severe ones, as it requires bringing the power of the whole system down. In embedded systems that means taking out the battery, or flipping a hardware switch, which is often either inconvenient or inaccessible in consumer electronics.

After device characterization and establishing SF modes and thresholds, this information is used to create a circuit model and optimize the design to improve device robustness to SF. The robustness improvement is quantified as increase in threshold values.

III. MODELING METHODOLOGY

A. *Victim Pin Quasi-Static I-V Model*

The model of the victim pin is a standard 3-parameter diode to VDD and a diode to VSS that is based on measured quasistatic I-V curve. The measurement consists of sweeping magnitude of

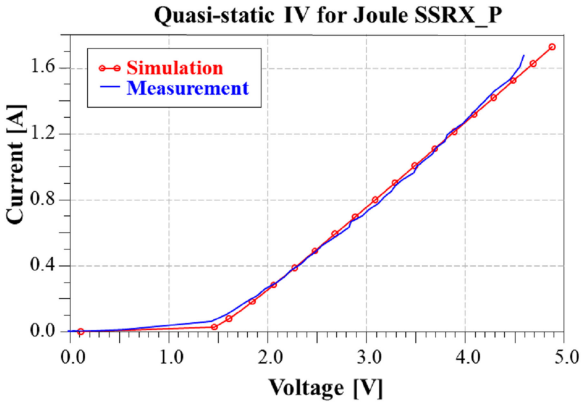

Fig. 5. Model of the victim pin SSRX_P compared to the measured quasi-static IV curve. The characteristic remains the same whether the DUT is powered or not.

100 ns TLP pulse with t_{rise} of 0.6 ns, then averaging window of 70–90% in transient voltage and current waveforms. This model describes pin behavior for long stress pulses. Fig. 5 shows good agreement between the model and the measurement above 0.3 A of the injected current. This is acceptable, because no failures occur at low levels of stress. When testing the DUT pin in order to create a diode model for SF analysis, one should limit the injection range to well below the levels of current and voltage that cause permanent damage (hard failure). A reasonably safe upper bound would be 70% of the hard failure threshold. Higher voltage or current can either introduce damage immediately, or cause latent damage of the DUT due to accumulated stress from multiple injections.

B. Pin SF Model

The SF characterization determines the stress current threshold of different SFs. To use this information in a SEED simulation two options are possible. The SEED simulation can calculate and output the victim current, then in a post processing step it can be determined whether a SF occurs. A circuit-based alternative allows to obtain relatively faster results, thereby removing the requirement of additional data post processing. For relatively faster results during the SEED simulation, a circuit is designed to describe the victim's reaction to the injected current.

The most critical parameter in the SF model is measuring the average current I_{avg} injected into the victim, then comparing it against the thresholds obtained in the process of pin characterization. Average current is obtained as follows:

$$I_{\text{avg}} = \frac{Q_{\text{total}}}{T_{\text{TLP}}} = \frac{1}{T_{\text{TLP}}} \int_{t0}^{t1} i_{\text{victim}}(t)\, dt \qquad (1)$$

where T_{TLP} is TLP pulse length, i_{victim} and Q_{total} are the current and total charge injected into the pin, respectively.

Fig. 7 describes the SF pin symbol and the circuit that combines the I-V diode model and the SF model for the USB3 re-enumeration SF mode.

Part 1) of Fig. 7 has the current controlled voltage source as an ideal current probe. The two ideal diodes determine the stress current path for different stress polarities.

Part 2) of Fig. 7 is a charge detector that measures total charge Q_{total} injected into the victim pin.

Part 3) of Fig. 7 contains the circuit that detects whether the I_{avg} current threshold (specified by the pin symbol parameter) has been exceeded and the probability value of the SF. The dc-voltage source outputs signal proportional to the failure likelihood as observed during the characterization process. The voltage-controlled switch isolates the output pin from the dc source.

The potential at the terminal of the charge detector's capacitor is used as control voltage V_{ctrl} of the switch. Fig. 8 illustrates how the potential tracks the integral of injected stress current. As the V_{ctrl} reaches the threshold value, the switch shorts, thus bringing the output pin potential to the value of SF likelihood.

The detector circuit and the SF output circuits are duplicated for each SF mode. All SF output pin fail levels are summed to provide the total probability P_{total} that any failure would occur. P_{total} is output as voltage at a pin of the symbol. This SF model provides the failure probability directly during the simulation run and a postprocessing is not required. This accelerated the process of design optimization, as described in Section IV.

IV. SF SEED Concept and Implementation

System-efficient ESD design has been discussed, but it has not yet been applied to SFs [4], [6]. The methodology consists of the following steps:

1) pin characterization with TLP;
2) pin-specific modeling;
3) simulation of stress waveforms.

First, the target interface is experimentally characterized on reference hardware, then a corresponding measurement-based physical and SF-pin models are developed. The viability of SEED methodology is explored in relation to SFs of USB3 Gen 1 SSRX_P pin. Several mitigation schemes are tested experimentally to evaluate their effectiveness.

Fig. 6 provides schematic overview of the interface model. TLP is modeled as pulse-voltage source. The interconnect discontinuity and PCB traces are modeled based on TDR measurements. The victim pin is represented as a diode, as described in Section III. Several external mitigation techniques are applied to the pin and the SF robustness is evaluated in terms of the SF threshold shift.

A. Mitigation Techniques: Resistors and TVS Diodes

Several external mitigation techniques are tested in this work, experimentally and within numerical models as follows:

1) an external current-limiting series resistor;
2) a current-diverting TVS diode to signal reference;
3) a combination of a series resistor and a TVS diode.

Several values of series resistors are tested and compared, but standalone resistors are never used as a mitigation technique. Often, they are combined with a TVS diode placed between the protection diode and the victim. In terms of the stress, this means that there is a higher impedance towards the victim and the current is diverted to the TVS diode instead. In terms of

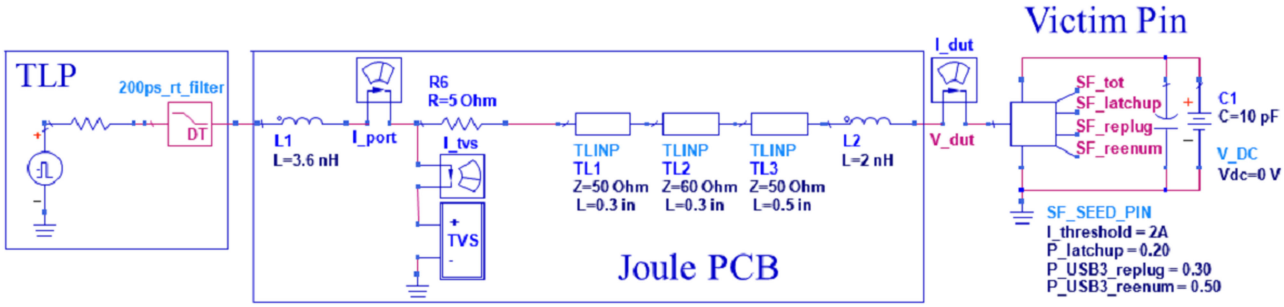

Fig. 6. System model for the SSRX_P pin including several elements of the PCB, the USB connector, and protection devices.

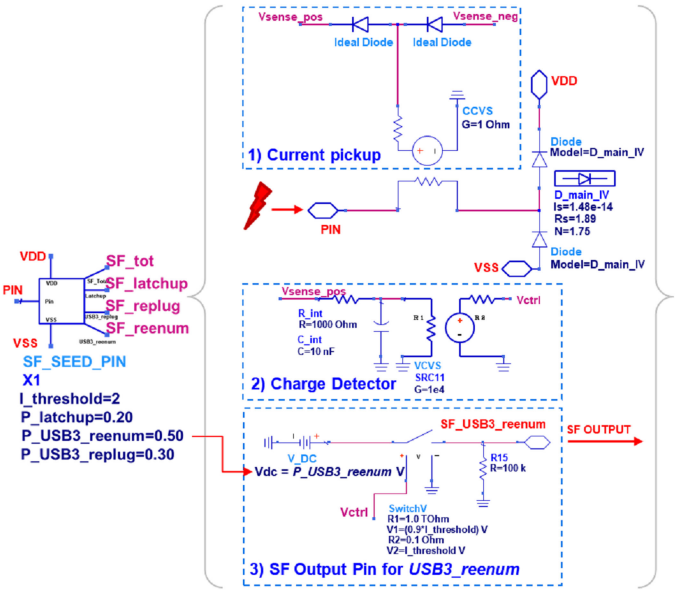

Fig. 7. Circuit model of the SF detector and output.

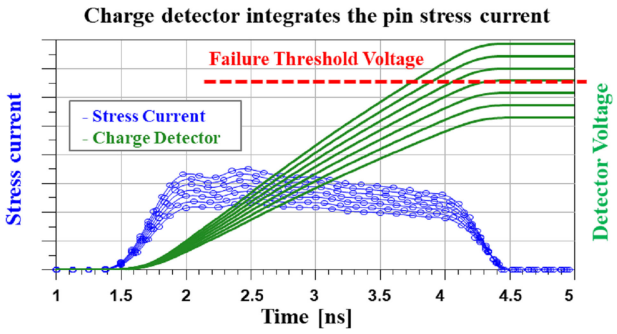

Fig. 8. Charge detector of the SF Pin model output. The current is integrated and then the obtained charge is compared to the threshold value established during the measurement phase.

voltage, it helps to raise the node potential at the diode terminal, which turns ON the diode at lower current stress levels.

As a part of this investigation, several TVS diodes were first evaluated in terms of their quasistatic I-V characteristics. In the next step, dynamic models were built to describe the turn ON behavior, and previously established modeling framework was used [13], [15]. The main idea is to divert the stress current away

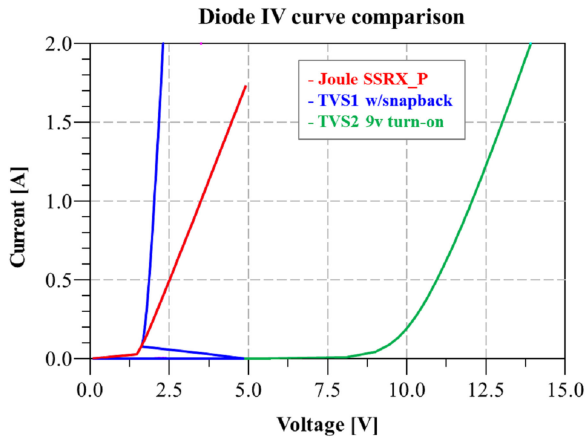

Fig. 9. TVS diode I-V curve compared to the victim pin SSRX_P.

from the victim. The diode static characteristics are compared to the victim pin in Fig. 9. Here, several I-V curves are compared against each other in terms of turn ON voltage and dynamic resistance. The external diode that turns ON at lower voltage than the victim's ON-chip protection diodes (red curve) will provide stronger protection. In current situation, TVS1 turns ON faster than the victim's ON-chip protection and has much lower dynamic resistance. This is expected to improve the robustness of the pin. TVS2 turns ON at a much higher voltage and, therefore, is not a viable protection option if used standalone. Two additional configurations are explored with TVS2 diode, where series resistors of $R = 5\ \Omega$ and $R = 10\ \Omega$ are placed between the victim and the diode. Measurement results and a qualitative model are presented in the following section.

V. Results and Discussion

A. Measurement Results

For each of the evaluated mitigation techniques, the DUT "expansion board" is modified, then tested for SF likelihood. The shift in the threshold is the criterium that quantifies an improvement of the interface pin robustness. "No protection" case is used as a reference. All other configurations are tested with 100 ns and 2 ns TLP. The former is commonly used to represent a whole IEC discharge pulse directly into the pin. The short 1-2 ns pulses represent the stress coupled indirectly.

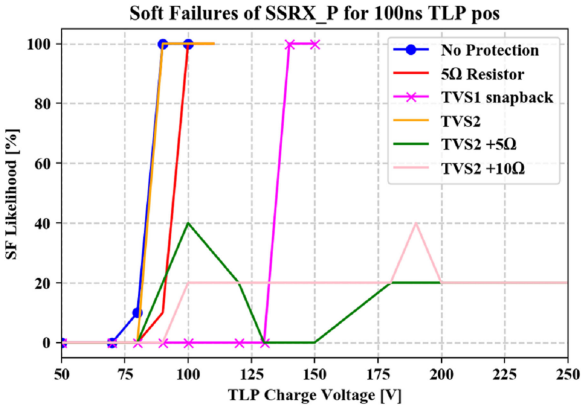

Fig. 10. Measured overall SF threshold shift due to external protection placement, results for positive 100 ns TLP.

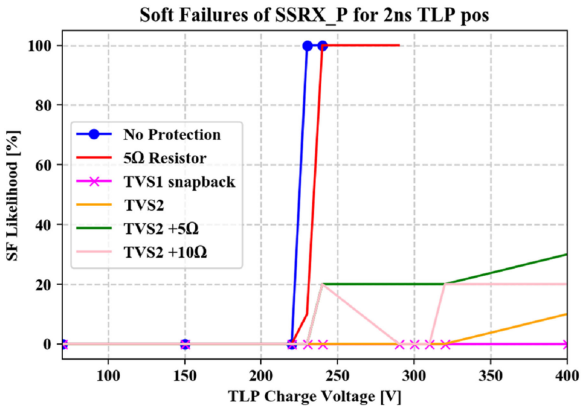

Fig. 11. Measured overall SF threshold shift due to external protection placement, results for positive 2 ns TLP.

Fig. 10 shows 100 ns TLP results and the improvement of SF robustness of USB3 interface SSRX_P pin. For the long pulses, adding a series resistor shows about +20 V improvement in SF threshold. Placing one TVS2 diode has no significant effect, while TVS1 diode improves the robustness by about +50 V. In order to achieve more effective results, TVS2 is combined with a series resistor (cases "TVS2 + 5 Ω" and "TVS2 + 10 Ω"). Both these cases show at least 150 V shift in SF threshold of P_{total}. There is a background rate of ∼20% SF rate at lower stress levels. This can be explained if the DUT has multiple failure modes that manifest the same way, but have different root causes. Thus, only a part of the SF (∼80%) has reduced, while ∼20% have not been mitigated by the protection scheme.

Fig. 11 shows the results of the various protection schemes for 2 ns TLP. Placing a series 5 Ω resistor only gives a marginal difference of +10–20 V. Placing one TVS2 diode improves the result for 2 ns pulses by +200 V. TVS2 + 5 Ω scheme also improves the robustness, but the levels are tested only till +160 V, to avoid interface damage. The best improvement is observed for TVS1 device, it snaps back at much lower voltage (V_{t1} = 5 V) and has low dynamic resistance. No SFs were observed for this case at least up to +160 V above the reference threshold levels. Higher cases were not tested to avoid damage to the interface.

TABLE II
SUMMARY OF 100% SF THRESHOLDS IN MODEL VERSUS MEASUREMENT IN TERMS OF TLP CHARGE VOLTAGE. WITHOUT PROTECTION THE 100 NS TLP FAILURE THRESHOLD IS AT 90 V AND FOR 2 NS TLP AT 230 V. THE SHOWN VALUES ARE IMPROVEMENTS IN THE THRESHOLD LEVEL

	100ns TLP Shift in threshold		2ns TLP Shift in threshold	
Configuration	**Model**	**Meas.**	**Model**	**Meas.**
5Ω in series	+10 V	+20 V	+20 V	+10 V
TVS1 (snapback)	+140 V	+70 V	+270 V	>+160 V*
TVS2 (9v turn-on)	+0 V	+0 V	+160 V	>+160 V*
TVS2 + 5 Ω	+170 V	>+150 V*	+500 V	>+160 V*
TVS2 + 10 Ω	+500 V	>+150 V*	+800 V	>+160 V*

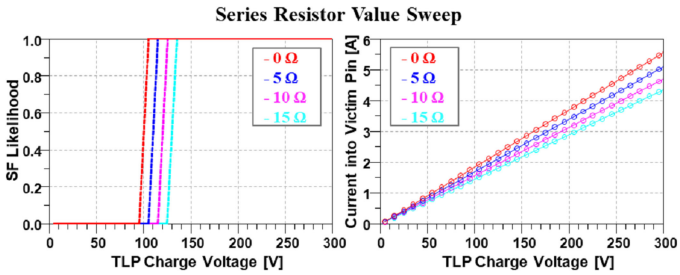

Fig. 12. Left: shift in SF threshold as the series resistor limits current into the victim pin. Resistor value swept 0–15 Ω, simulation result Right: current entering the victim pin, reduced as resistance increases.

It is shown that SFs can be mitigated to some degree by applying the same protection schemes typically used in hard failure prevention.

B. Quantitative Circuit Model Results

Equivalent circuit simulations are performed for the protection schemes tested in the experiment. The model includes the victim diode, SF pin model, and the PCB. The outcomes are compared in TABLE II, which shows that the proposed model generally predicts the change in SF threshold in cases of a standalone resistor and a TVS2 diode for 100 ns pulses. In case of TVS1 snapback diode, the model overestimates the improvement, while for cases of TVS2 + 5 Ω and TVS2 + 10 Ω the observed threshold improvement was at least +150 V, but the tests were not pushed higher, for the risk of DUT damage. For 2 ns pulses the model also either predicts the change, or shows qualitative improvement.

The model provides results for two pulse lengths: 100 ns and 2 ns. The values of $I_{\mathrm{avg}}(100\ \mathrm{ns})$ and $I_{\mathrm{avg}}(2\ \mathrm{ns})$ were measured during the characterization and are used as the threshold value in the simulation. The model outputs change in threshold of overall failure likelihood P_{total}.

Adding a series resistor in order to limit the current flowing into the victim pin yields marginal improvements. Fig. 12 shows the voltage output of P_{total} output terminal of the SF pin model (left) and the current flowing into the pin versus TLP charge voltage (right). This result closely correlates to the observations: SF threshold shift is proportional to the resistor value.

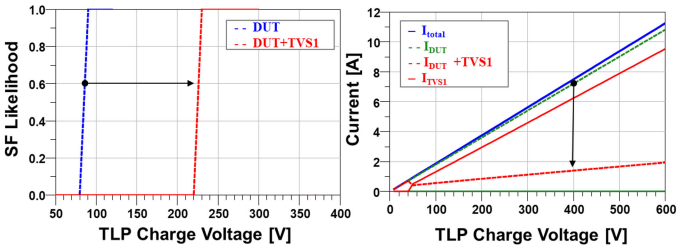

Fig. 13. Simulation result using TVS1 as external protection. Left: the shift of SF threshold versus TLP voltage. Right: currents versus TLP voltage. The snapback is evident by the knee and sharp drop in the victim current.

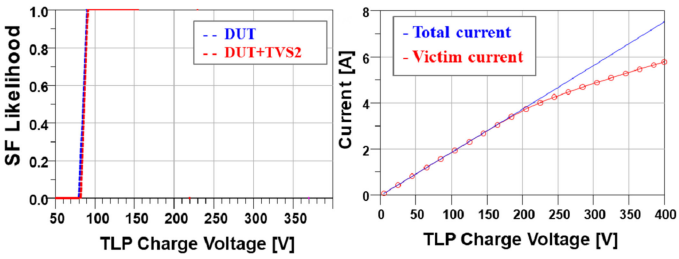

Fig. 14. Simulation result using TVS2 as external protection. Left: no shift of SF threshold versus TLP voltage. Right: currents versus TLP voltage. This TVS diode turns ON at higher voltage, thus, no current is diverted away from the victim until much higher TLP levels.

The case with TVS diodes varies from device-to-device and requires careful consideration of diode characteristics. The main purpose of the TVS devices is to clamp voltage on the pin and divert current. The outcome depends on both the diode choice and the victim characteristics.

In the case of TVS1, a diode with low trigger voltage V_{t1}, $+140$ V improvement is predicted by the model, as illustrated in Fig. 13. The left side shows the shift in the SF threshold, the right-side current split between the victim DUT, and the TVS diode. At $\sim$50 V, it is observed that the snapback occurs and TVS1 goes into low-impedance mode, thus diverting vast majority of current away from the victim. This qualitatively matches the measurement, but overestimates the observed $+70$ V shift in the measurement. This can be explained, in part, if some failure modes are caused by the peak stress current, instead of the average current. A possible explanation is that peak voltage due to inductive overshoot is the cause of this particular failure mode. This was ruled out by additional tests with rise time swept from 0.6 to 10 ns. The results showed significant reduction in voltage overshoot, but no significant change in the observed failure threshold. This confirms the findings in the existing research, which shows that SFs in USB3.0 interface are not rise-time dependent [4].

TVS2 has higher turn-ON voltage $V_{br} = 9$ V, while the victim turns ON at $V_{br} = 1.5$ V. This means that the diode will not have much effect on the current until much higher stress levels. Fig. 14 (right) shows comparison between total current injected by TLP and victim pin current. The effect of the TVS2 diode, as expected, is small. Thus, the SF threshold is not affected by this device, as shown in Fig. 14 (left) and confirmed by the measurement.

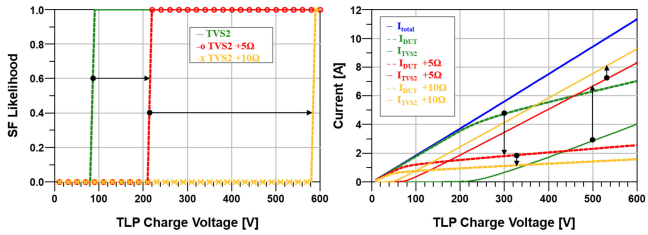

Fig. 15. Simulation result using TVS2 and a resistor as external protection shows shifts of SF threshold versus TLP voltage.

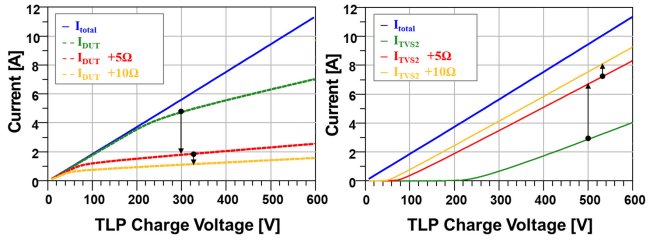

Fig. 16. Simulation result using TVS2 and a resistor as external protection shows currents versus TLP voltage. With added resistance, the victim's impedance rises, thus, TVS2 turns ON at lower TLP voltage and diverts current more effectively. Left: shows DUT current reduction because of adding the resistor; right: shows TVS current increase. The total current is given as a reference.

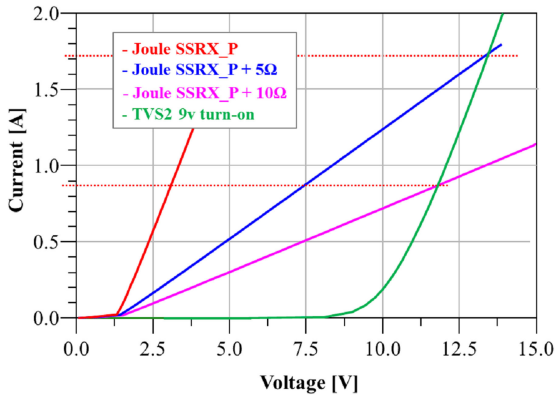

Fig. 17. I-V characteristic of combined victim and a series resistor. The intersection points with TVS2 characteristic are, where the diode becomes dominant and diverts the current away from the victim.

However, a possible way to improve the performance of a diode such as TVS2 is to combine it with 5 Ω resistor series with the signal path. When combined—the victim and the resistor impedances combine into higher impedance path than TVS2. In this case, the diode turns ON at lower stress levels and efficiently diverts the current away from the victim, improving robustness by at least $+160$ V. The shift in threshold is shown Fig. 15 for R $=$ 5 Ω and R $=$ 10 Ω values. The configuration of R $=$ 10 Ω predicts $+500$ V improvement, however, the result is confirmed only until $+160$ V, to avoid damage to the DUT interface. The resulting DUT current reduction and TVS current increase are shown in Fig. 16. The impedance combination effect is illustrated in Fig. 17. The intersections of the TVS2 diode with the other curves is where the diode becomes the dominant sink for the stress current.

VI. Outlook

Based on this example that a SF SEED concept can be applied in a prehardware design optimization; multiple directions of methodology enhancement can be considered as follows.

1) A full system-level simulation can be performed for an IEC test to the system to extract the actual energy coupling into the victim pin indirectly.
2) As the power delivery network can have a strong influence on certain SF types, the methodology can be expanded to account for the PDN [3].
3) The method is not limited to diodes and resistors. CMC are also known to improve ESD robustness against hard fails, especially when used together with a TVS device [17]–[20]. SF SEED can help to investigate whether CMC can be used to improve SF robustness as well.

VII. Conclusion

For the first time, this article demonstrates that conventional ESD hard failure protection techniques can also be used to improve the system level ESD SF robustness for direct pin injection. This is achieved by diverting most of the ESD-induced current away from the victim pin. This does not avoid bit-errors, but it prevents current injection into VSS, VDD, or the substrate of the victim IC, which can lead to errors that cannot be corrected by the protocol of the I/O. A well selected TVS clamps the voltage at the IC close to the signal levels, such that only a small amount of current will be forced by the ESD induced current into the IC.

The reduction of the SF likelihood is investigated in a SEED-like simulation. This requires SEED models that include the SF behavior; 100 ns and 2 ns TLP are used to represent direct and indirect pulse injection.

The simulation of a large signal circuit model of the victim pin, comprising a virtual detector circuit and the SF threshold dependency, show a good correlation to the measurement. The proposed version of the system model is circuit based; however, the same methodology can be applied in cosimulation with three-dimensional full-wave solvers.

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