Measurement Investigation of MLCC Mounting Variation Impact on Acoustic Noise in Power Distribution Network

Yin Sun
Missouri University of Science and Technology
Rolla, MO, USA
ysc26@mst.edu

Songping Wu
Google inc.
Mountain View, CA, USA
songpingwu@google.com

Jianmin Zhang
Google inc.
Mountain View, CA, USA
jianmin@google.com

Zhiping Yang
Google inc.
Mountain View, CA, USA
songpingwu@google.com

Chulsoon Hwang
Missouri University of Science and Technology
Rolla, MO, USA
hwangc@mst.edu

***Abstract*—The multilayer ceramic capacitors (MLCCs) mounting method impact on the MLCC induced acoustic noise in printed circuit board (PCB) is investigated through measurement. The influence of MLCC soldering stencil height, MLCC orientation and MLCC pair offset distance are evaluated on a series of test boards. The sound pressure level (SPL) is measured to evaluate the PCB acoustic noise performance. In the investigated mounting variation range, the acoustic noise performance does not exhibit noticeable changes.**

Keywords—Acoustic noise, multilayer ceramic capacitors, mounting, mirrored layout, power distribution network, sound pressure level

I. Introduction

The multilayer ceramic capacitors (MLCCs) have been widely adopted in printed circuit board (PCB) for the power distribution network (PDN) as decoupling capacitors to reduce the power supply voltage ripple [1]. The popularization of MLCC originates from the high permittivity dielectric material, allowing high capacitance value with small package size. However, the piezoelectric characteristic possessed by the dielectric material can lead to acoustic noise in the mobile systems [2]-[4], which could be a concern for the user experience. Due to the piezoelectric effect of the MLCC dielectric material, when electrical signal in audio frequency range (20 Hz – 200000 Hz) is applied on the capacitor, the capacitor will vibrate with the pace of the electrical signal. Since the size of MLCC is relatively small, the generated noise is too weak for human to hear [2]. However, as the MLCCs are attached to PCB through rigid soldering joints, the MLCC vibration will pass on to PCB. As a result, the PCB vibration will generate the acoustic noise that user can perceive [3][4].

The electrical root cause of the acoustic noise problem is the audio frequency noise on the power rail. Reducing noise voltage on PDN can help to reduce the acoustic noise [5]. However, even with the reduced noise voltage, with hundreds of MLCCs on board, the acoustic noise could still be noticeable [5]. Targeting the acoustic noise from mechanical perspective can help to release the requirement for PDN impedance in low frequency range and there have been some related studies conducted on real products. The acoustic noise in a solid state drive (SSD) product is investigated through vibration measurement and sound pressure level measurement [6]. The acoustic noise in a notebook product is studied through electrical-vibration co-analysis and a vibration simulation method is developed [4][7]. In addition to the acoustic noise analysis on the fabricated products, a series of design guidelines regarding MLCC placement and layout on PCB are proposed for acoustic noise reduction [8]. However, besides the effect of various MLCC layout, the impact of MLCC mounting method on the acoustic noise performance should also be investigated, as there will be fabrication variation during the assemble process [9].

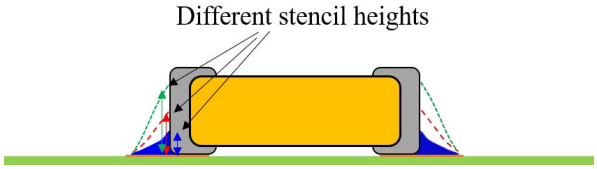


Figure 1: MLCC soldering stencil height.

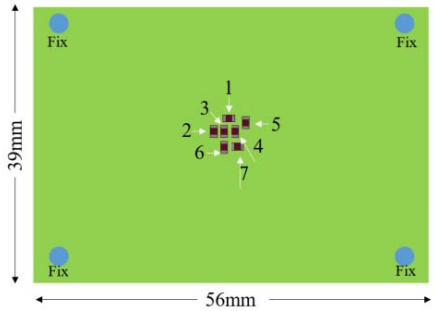
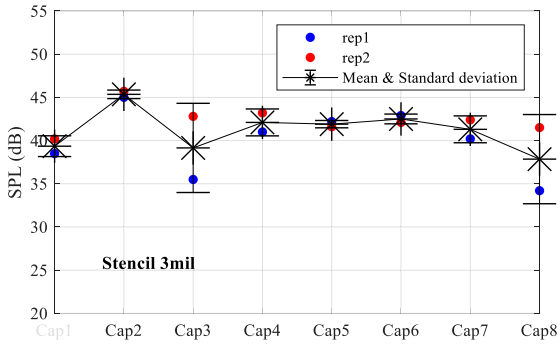
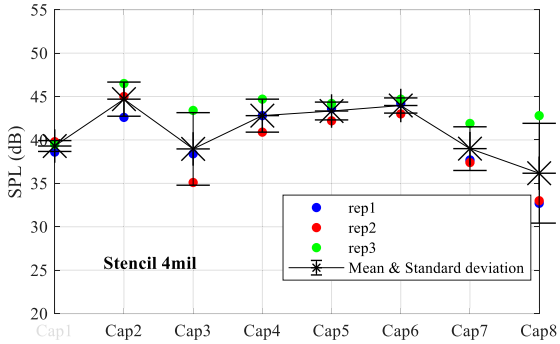


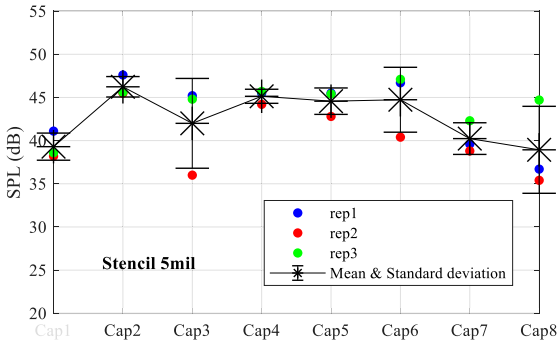
Figure 2: Test board for stencil height and MLCC orientation investigation.



(a)



(b)



(c)

Figure 3: SPL of PCB with different MLCC soldering stencil heights. (a) 3mil, (b) 4mil, (c) 5mil.

Table I: SPL mean and standard deviation under different stencil height

Stencil Height		C #1	C #2	C #3	C #4	C #5	C #6	C #7	C #8
3 mil	M(dB)	39	45	39	42	42	43	41	38
	SD(dB)	1.2	0.5	5.1	1.5	0.4	0.6	1.5	5.2
4 mil	M(dB)	39	45	39	43	43	44	39	36
	SD(dB)	0.6	1.9	4.1	1.9	1	0.8	2.5	5.7
5 mil	M(dB)	39	46	42	45	44	44	40	39
	SD(dB)	1.6	1.2	5.2	0.8	1.5	3.7	1.8	5

In this work, the MLCC mounting variation impact on the PCB acoustic noise performance is evaluated through sound pressure level (SPL) measurement. The influence of soldering stencil height, MLCC orientation and MLCC pair offset distance are tested on a series of test boards. The soldering stencil height varies from 3 mil to 5 mil. The MLCC mounting orientation can be either parallel or perpendicular to the PCB. For the MLCC pair case, the offset distance varies from 0 mm to 1.6 mm.

II. MLCC Mounting Variation Impact on Acoustic Noise

As PCB vibration is caused by the mounted MLCCs, it is preferable to investigate whether different MLCC mounting conditions will lead to any distinct PCB acoustic noise performance. The influence of solder stencil height, MLCC orientation and MLCC pair offset distance are investigated through sound pressure measurement.

A. MLCC Stencil Height Impact

The illustration of different MLCC solder stencil heights are shown in Fig. 1. The stencil height effect is investigated on a designed test board as depicted in Fig. 2. An eight-capacitor group is placed in the middle of the board. Seven capacitors are on the top side and the 8th capacitor is on the bottom side of the board mirroring the 3rd capacitor. The eight capacitors have individual power supplies to control the applied electrical signals. The sound pressure measurement is conducted in the acoustic chamber and the detailed setup is described in [8], Fig. 6.

Various soldering stencil heights are achieved by the controlled fabrication process of the PCB fabrication house. Three soldering stencil heights, 3mil, 4mil and 5 mil are investigated. These are typical values for commercial application provided by the PCB house. MLCCs with 0603 package, 22uF are used during the test. The SPL measurement results are summarized in Fig. 3 (a), (b) and (c) for 3mil, 4mil and 5 mil stencil heights, respectively. For each test case, three samples are evaluated. The dotted data represents each repetition for the corresponding case. The mean (M) and standard deviation (SD) are labeled with star and bar symbols and are summarized in Table I. The SPL readings are referenced to 2e10^{-5} Pa and displayed in dB scale. The electrical signals are kept to an average AC level of 25 mV, with 4 V DC offset. It can be observed that, there are no obvious changes of acoustic noise with the variation of soldering stencil heights.

B. MLCC Mounting Orientation Impact

Considering the layered internal electrodes structure of MLCC, when MLCCs are mounted on the PCBs, the internal electrodes could be either in parallel with underlying PCB or perpendicular to the board, as illustrated in Fig. 4. In this work, unless otherwise specified, the MLCCs are mounted with the internal electrodes in parallel with board. The SPL measurement results are shown in Fig. 5 (a) and (b) for the parallel and vertical mounting cases respectively. The MLCCs applied in the experiments are with 0603 package, 4.7uF. The electrical signals are kept to an average AC level of 25 mV, with 4 V DC offset. For each test case, ten samples are evaluated. The mean and standard deviation are summarized in Table II. It can be seen

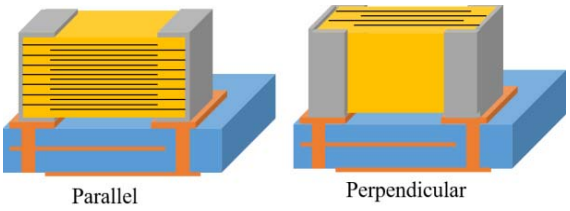


Figure 4: MLCC orientation.

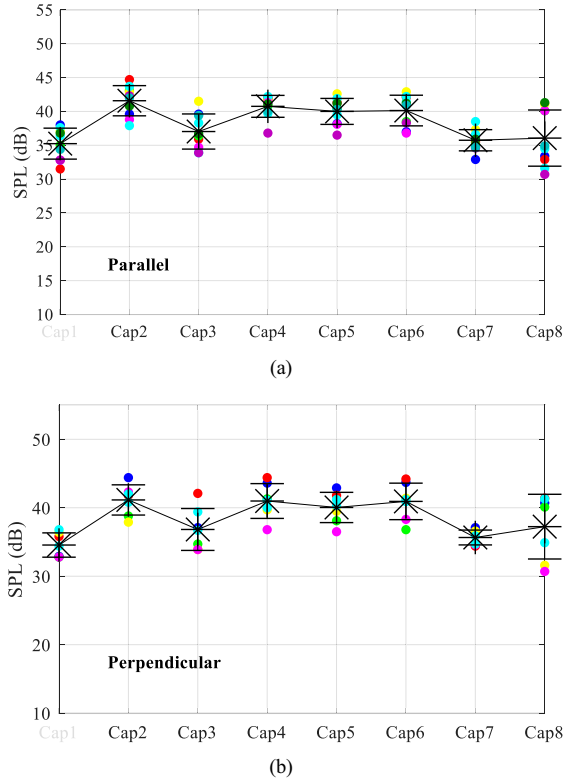


Figure 5: SPL of PCB with different MLCC orientation. (a) Parallel, (b) perpendicular.

Table II: SPL mean and standard deviation under different orientation

Direction		C #1	C #2	C #3	C #4	C #5	C #6	C #7	C #8
Par	M(dB)	35	42	37	41	40	40	36	36
	SD(dB)	2.2	2.2	2.6	1.6	1.9	2.3	1.5	4.1
Per	M(dB)	35	41	37	41	40	41	36	37
	SD(dB)	1.7	2.2	3	2.5	2.2	2.7	1	4.7

that the acoustic noise performance for parallel mounted and vertically mounted MLCCs are similar. When AC noise in audio frequency range is applied on the capacitor, the capacitor will vibrate in the direction of the applied electrical fields. For MLCC with parallel mounting, the MLCC vibration is in the vertical direction. On the other hand, for MLCC with vertical mounting, the MLCC vibration is in the horizontal direction.

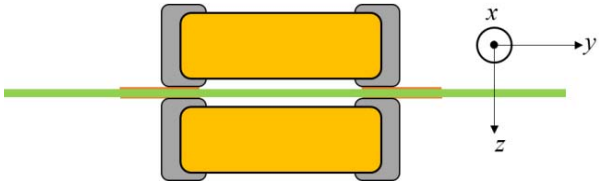


Figure 6: Mirrored MLCC pair layout.

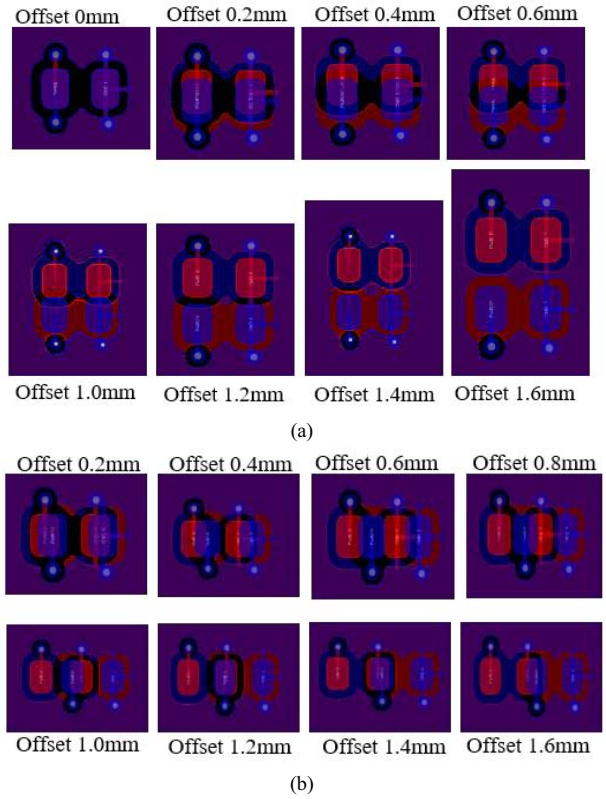


Figure 7: Mirrored MLCC pair offset distance test boards. (a) *x* direction, (b) *y* direction.

From these test results, it seems that either of the MLCC vibration direction will lead to similar level of acoustic noise of PCB.

C. MLCC Pairs Offset Distance Impact

As discussed in [9], the mirrored capacitor pair layout can effectively reduce the acoustic noise, as shown in Fig. 6. It is desirable to evaluate the effectiveness of this layout structure when offset is presented. A series of test boards are designed to test the offset influence. The test boards with offset in *x* and *y* directions are sketched in Fig. 7 (a) and (b), respectively. The top and bottom capacitors can be excited separately. The boards are fixed at the four corners on a platform in the acoustic chamber. The offset distance is varied from 0 to 1.6mm. This set of tests is conducted on MLCCs with 0603 package, 22uF.

To evaluate the offset distance impact on the vibration cancellation effectiveness of mirrored cap layout, two excitation

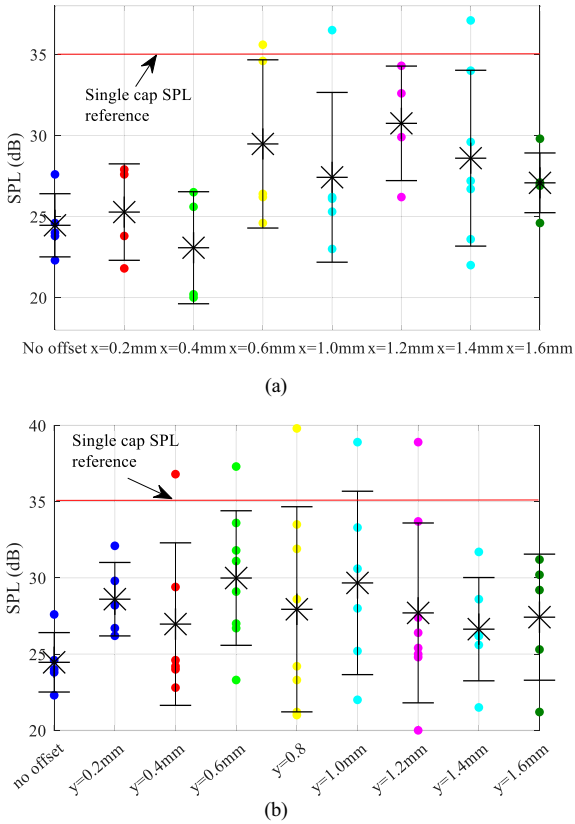


Figure 8: SPL reduction of MLCC mirrored layout with different offset distance under test scheme one. (a) *x* direction, (b) *y* direction.

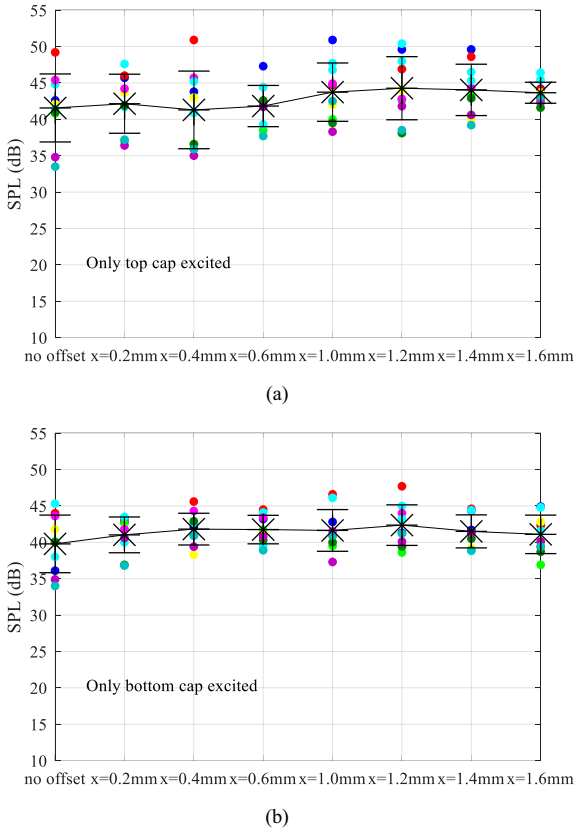


Figure 9: *x* direction offset boards, single cap excitation SPL results. (a) only top cap excited, (b) only bottom cap excited.

Table III: SPL mean and standard deviation with different offset, scheme1

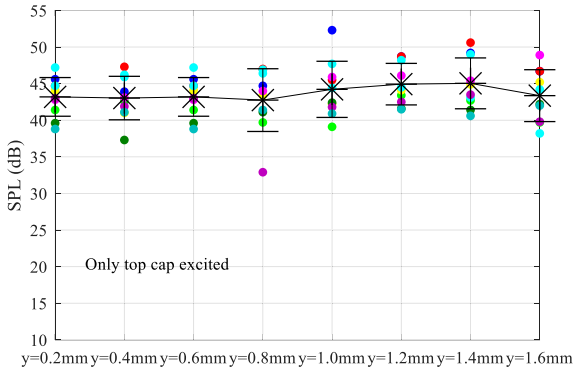
Offset (mm)		0	0.2	0.4	0.6	0.8	1.0	1.2	1.4	1.6
x (dB)	M	24	25	23	29	NA	27	31	29	27
	SD	1.9	2.9	3.5	5.2	NA	5.2	3.5	5.4	1.8
y (dB)	M	24	29	27	30	28	30	28	27	27
	SD	1.9	2.4	5.3	4.4	6.7	6	5.9	3.4	4.1

Table IV: SPL mean and standard deviation of x direction offset test boards with one cap excitation

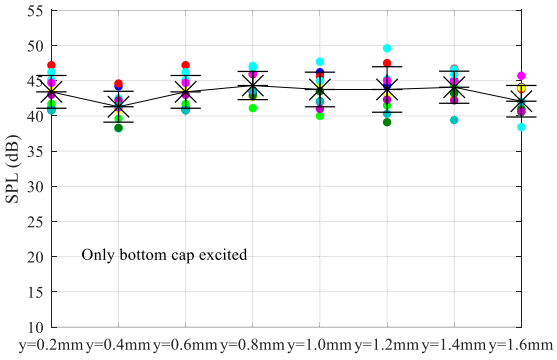
Offset (mm)		0	0.2	0.4	0.6	0.8	1.0	1.2	1.4	1.6
Top (dB)	M	42	42	41	42	NA	44	44	44	44
	SD	4.6	4	5.3	2.8	NA	4	4	3.5	1.4
Bot (dB)	M	40	41	42	42	NA	42	42	41	41
	SD	4	2.5	2.2	2	NA	2.9	2.8	2.3	2.6

schemes are tested. Since the piezoelectric characteristic of MLCCs can vary, even for the same package size cap with same value, when the same electric signals are applied, the SPL level can be different. In the first test scheme, the SPL where only the top MLCC is excited is kept to 35 dB. The obtained corresponding voltage for each offset distance board is then applied to both the top and bottom capacitors to check the reduction of acoustic noise. The SPL measurement results for the offset in *x* and *y* directions using this first test scheme are shown in Fig. 8 (a) and (b). For each test case, ten samples are evaluated.

The mean and standard deviation are summarized in Table III. It can be observed that the variation is quite large when the two caps are excited. This may be due to the different voltage to vibration transfer ratio of the top and bottom capacitors [4]. Nonetheless, from the averaged SPL results, it can be shown that even with distance offset, the mirrored layout can still reduce the acoustic noise effectively. This maybe because for the vibration in the audio frequency range, the wavelength is very large compared to the offset distance.



(a)



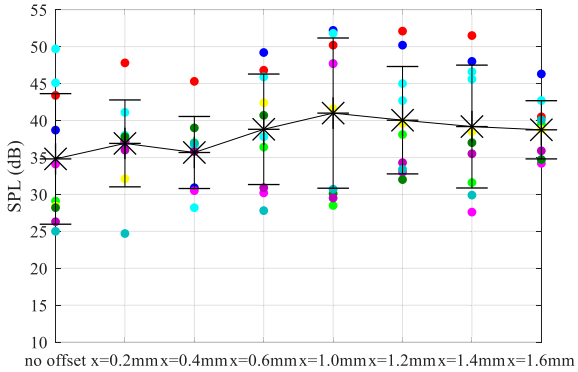
(b)

Figure 10: *y* direction offset boards, single cap excitation SPL results. (a) only top cap excited, (b) only bottom cap excited.

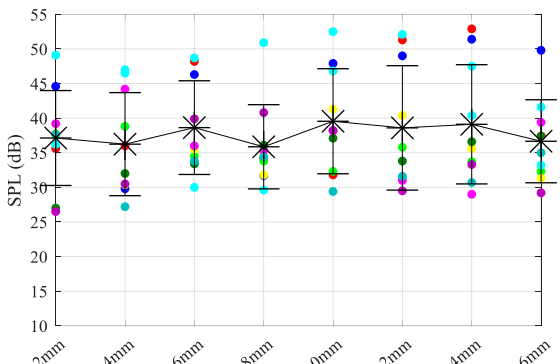
Table V: SPL mean and standard deviation of y direction offset test boards with one cap excitation

Offset (mm)		0	0.2	0.4	0.6	0.8	1.0	1.2	1.4	1.6
Top (dB)	M	42	43	43	43	43	44	45	45	43
	SD	4.6	2.6	3	2.6	4.3	3.8	2.8	3.4	3.5
Bot (dB)	M	40	43	41	43	44	44	44	44	42
	SD	4	2.3	2.1	2.3	2	2.5	3.2	2.3	2.2

For the second test scheme, the voltages on all the test boards with different offset distance are kept to the same as 35 mV AC with 4 V DC. Firstly, the SPL level of single capacitor excitation is measured. For *x* direction offset boards, the SPL results for top cap only and bottom cap only cases are summarized in Fig. 9 (a) and (b) for reference. The mean and standard deviation are summarized in Table IV. For *y* direction offset boards, the SPL results for top cap only and bottom cap only cases are summarized in Fig. 10 (a) and (b). The mean and standard deviation are summarized in Table V. The SPL measurement



(a)



(b)

Figure 11: SPL reduction of MLCC mirrored layout with different offset distance under test scheme two. (a) *x* direction, (b) *y* direction.

Table VI: SPL mean and standard deviation with different offset, scheme2

Offset (mm)		0	0.2	0.4	0.6	0.8	1.0	1.2	1.4	1.6
x (dB)	M	35	37	36	39	NA	41	40	39	39
	SD	8.8	5.9	4.9	7.5	NA	10	7.3	8.3	4
y (dB)	M	35	37	36	39	36	40	39	39	37
	SD	8.8	6.9	7.4	6.8	6	7.6	9	9	6

results for the two caps excited cases are shown in Fig. 11 (a) and (b) for the offset in *x* and *y* directions respectively. The mean and standard deviation are summarized in Table VI. Similarly, despite the relatively large variation, it can be observed from the averaged results that the offset distance will not influence the vibration cancellation of the mirrored capacitor layout.

III. Conclusion

The MLCC mounting method variation impact on the PCB acoustic noise are tested on a series of designed test boards. Three soldering stencil heights are investigated and there is no

obvious change of the SPL of the PCB. Two MLCC orientations are also evaluated. The internal electrodes of MLCC can be either in parallel with the underlying board or perpendicular to the PCB. Based on the SPL results, the orientation of MLCC does not exhibits strong impact to the acoustic noise performance of the board. As a pair of MLCC is usually adopted to reduce the parasitic inductance and the acoustic noise, the influence of offset distance of these two capacitors in a pair is tested. As the wavelength of the audio frequency range signal is very large, small offset distance does not influence the acoustic noise level in the PCB.

REFERENCES

[1] L.D. Smith, R.E. Anderson, D.W. Forehan, T.J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology." *IEEE Trans. Adv. Packag.*, vol. 22, no. 3, pp. 284-291, Aug 1999.

[2] B.H. Ko, S.G. Jeong, Y.G. Ahn, K.S. Park, N.C. Park and Y.P. Park "Analysis of the correlation between acoustic noise and vibration generated by a multi-layer ceramic capacitor." *Microsyst. Technol.*, vol. 20, no. 8, pp.1671-1677, May. 2014.

[3] Y. Sun, J. Zhang, Z, Yang, C. Hwang and S. Wu, "Measurement investigation on acoustic noise caused by 'singing' capacitors on mobile devices," in *Proc. IEEE Int. Symp. Electromagn. Compat*. Jul. 2019, pp. 505-510.

[4] Y. Sun, S. Wu, Z. Yang, C. Hwang and J. Zhang, "Measurement methodologies for acoustic noise induce by multilayer ceramic capacitors of power distribution network in mobile systems," *IEEE trans. Electromagn. Compat.*, submitted for publication.

[5] H. Baek, D. Yu, J. Lee, H. Shim and J. H. Kim, "Electrical approach to acoustic noise for MLCCs of power delivery network in mobile system," in *Proc. IEEE Electri. Des. Adv. Packag. Sys. Symp.,* Dec. 2015, pp. 62-66.

[6] D. Kim, N.C. Park, and Y.P. Park, "Analysis of high-pitched noise from solid-state drives generated by multilayer ceramic capacitors." *Microsyst. Technol.*, vol. 22, no. 6, pp.1367-1374, Jun. 2016.

[7] Y. Sun, J. Zhang, Z, Yang, C. Hwang and S. Wu, "Simulation investigation on acoustic noise caused by 'singing' capacitors on mobile devices," in *Proc. IEEE Int. Symp. Electromagn. Compat*. Jul. 2019, pp. 406-410.

[8] Y. Sun, S. Wu, Z. Yang, C. Hwang and J. Zhang, "Decoupling Capacitor Layout Design Guidelines with Acoustic Noise Consideration in Power Distribution Network," *IEEE trans. Electromagn. Compat.*, submitted for publication.

[9] Y. Wang, B.H. Ko, S.G. Jeong, K.S. Park, N.C. Park and Y.P. Park "Analysis of the influence of soldering parameters on multi-layer ceramic capacitor vibration." *Microsyst. Technol.*, vol. 21, no. 12, pp.2565-2571, Dec. 2015.