Modeling and Analysis of On-Chip Power Noise Induced by an On-Chip Linear Voltage Regulator Module With a High-Speed Output Buffer

Heegon Kim, Jonghyun Cho, Changwook Yoon, Brice Achkir, James Drewniak, and Jun Fan

***Abstract*—In this paper, analytical models of on-chip power noise induced by an on-chip linear voltage regulator module (VRM) circuit with a high-speed output buffer are proposed. Based on the piecewise linear approximated MOSFET *I–V* curve model, closed-form equations for the on-chip power noise induced by an on-chip low-dropout regulator are derived. The accuracy of the proposed analytical model is validated by SPICE simulation with a 110-nm CMOS technology library. Based on the proposed analytical models, the impacts of VRM design parameters on VRM output noise induced by load current and external noises are analyzed. Because self-impedance at the VRM output and external noise transfer functions share a common resonant frequency, the on-chip power noise is minimized by avoiding the resonant frequency from peak frequencies of noise source spectrums. The larger on-chip decoupling capacitance at load reduces, the overall on-chip VRM output noise. While the larger pass transistor size reduces the on-chip VRM output noise induced by the reference voltage fluctuation, it increases the noise generated by off-chip power fluctuation. The reference voltage node needs to be carefully designed, as opposed to an off-chip power distribution network, due to its dominant impact on the on-chip VRM output noise. The analysis results based on the proposed model provide an in-depth understanding of and useful design guidance for on-chip power noise induced by the on-chip linear VRM with a high-speed output buffer.**

***Index Terms*—High-speed output buffer, on-chip linear voltage regulator module (VRM), on-chip low-dropout (LDO) regulator, on-chip power distribution network (PDN), on-chip power noise.**

I. Introduction

INDUSTRIAL demands have focused on high performance and low power consumption for state-of-the-art applications such as smartphones. To achieve low power consumption in the system, the voltage supply level needs to be minimized, resulting in a reduction of the power noise margin. As the power noise margin decreases, controlling the on-chip power distribution network (PDN) noise is becoming more and more important. Because it is extremely difficult to reduce the amount of current consumption for high-performance systems, the PDN should be carefully designed to achieve low impedance. However, the PDN impedance between the power-consuming IC and off-chip power supply is difficult to reduce below a certain level due to the physical distance. Although decoupling capacitors have exhibited excellent performance in lowering the PDN impedance, continuously increasing the number of decoupling capacitors is not viable due to the cost and the allowable design area.

Recently, an on-chip voltage regulator module (VRM) using the same silicon technology for other power-consuming IC and implemented on the same silicon die has become a potential solution [1]–[12]. It reduces the physical distance to the current-consuming IC, resulting in reduced PDN parasitics and PDN impedance. Despite using the on-chip VRM, the on-chip PDN noise still can be unsatisfactory due to the continuously tightened power noise margin. Moreover, considerable noise sources, such as simultaneous switching noise (SSN) from high-speed output buffers, make it difficult for the on-chip PDN noise to satisfy the target margin [13]–[19]. The analysis of the on-chip PDN noise induced by the on-chip VRM circuit is of significant importance for the development of high-performance and low-power applications.

Most previous researches regarding on-chip VRM have been related to the proposal of new topologies and analysis of the on-chip VRM itself [1]–[12]. Though several papers related to analysis of the on-chip VRM impact on on-chip PDN noise have been published recently, they have only focused on comparisons of the on-chip PDN noises with and without the on-chip VRMs [20]–[22]. Research related to the in-depth analysis of the on-chip PDN noise induced by on-chip VRM has not been sufficient. Thus, modeling and analysis of the on-chip PDN noise induced by the on-chip VRM circuit are strongly required.

In this paper, the on-chip power noise induced by the on-chip linear VRM with a high-speed output buffer is analytically modeled and analyzed. An on-chip low-dropout (LDO) regulator is selected as the modeling and analysis target because it is usually employed in practical systems due to its compact size. Because of the considerable impact of SSN on the on-chip power noise, the high-speed output buffer is chosen as the aggressor current source at load. Based on the piecewise approximated MOSFET

Manuscript received January 1, 2018; revised April 24, 2018; accepted May 18, 2018. Date of publication June 25, 2019; date of current version June 11, 2020. This work was supported by the National Science Foundation under Grant IIP-1440110. *(Corresponding author: Jun Fan.)*

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Digital Object Identifier 10.1109/TEMC.2019.2921008

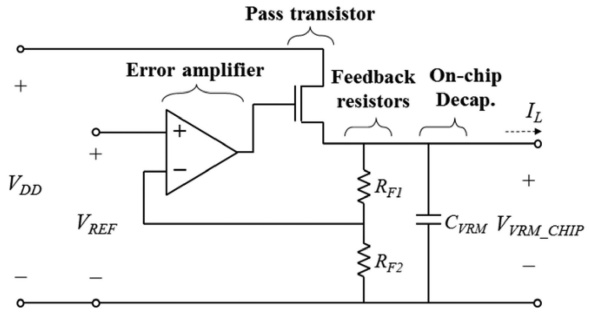

Fig. 1. Topology of a typical on-chip linear VRM circuit, which is a simple on-chip LDO voltage regulator.

I–V curve model, closed-form equations of the on-chip linear VRM output noises induced by the load current and external noises are proposed. The accuracy of the proposed analytical models is validated by SPICE simulation. In addition, impacts of the load current and external noises on the on-chip VRM output noise are analyzed based on the proposed analytical models. Off-chip power noise and reference voltage noise are selected as external noise sources. On-chip decoupling capacitance at load and pass transistor size are selected as VRM design parameters for analysis. Finally, several design guidances to minimize the on-chip VRM output noise are discussed.

II. Transient Response Analysis of a Typical On-Chip Linear VRM With a High-Speed Output Buffer

Fig. 1 shows the topology of a typical on-chip linear VRM circuit for modeling and analysis. The circuit is a typical LDO voltage regulator, which consists of an error amplifier, pass transistor, feedback resistors (R_{F1} and R_{F2}), and on-chip decoupling capacitor at load ($C_{\rm VRM}$). When the off-chip PDN supplies the appropriate level of on-chip linear VRM input voltage (V_{DD}), the on-chip linear VRM output voltage ($V_{\rm VRM\_CHIP}$) converges to a specific level determined by the reference voltage ($V_{\rm REF}$) and feedback resistors, as shown in

$$V_{\rm VRM\_CHIP} = V_{\rm REF} \times \left(1 + \frac{R_{F1}}{R_{F2}}\right). \tag{1}$$

Figs. 2 and 3 show the transient response of the typical on-chip linear VRM with low- and high-speed output buffers at load. The output buffer has a very short transmission line at load, which looks similar to the capacitive load. Because this section explains the concept of the different transient responses at low- and high-speed buffers, the large current peaks with this load condition were utilized to dramatically change the voltage levels. In addition, this paper assumes that there is no VRM input (V_{DD}) noise, which means that the pass transistor shown in Fig. 1 never goes into the linear mode.

When the load current (I_L) from the operating low-speed output buffer, which is a 2-ns pulse train, changes as shown in Fig. 2(a), the gate voltage of the pass transistor ($V_{\rm PASS}$) and the $V_{\rm VRM\_CHIP}$ fluctuate, as shown in Fig. 2(b). The default level shown in Fig. 2(b) is the dc level of the VRM output without noise. When I_L starts changing from time t_0, a large I_L pulse rapidly reduces $V_{\rm VRM\_CHIP}$ and $V_{\rm PASS}$ in a moment. Soon after,

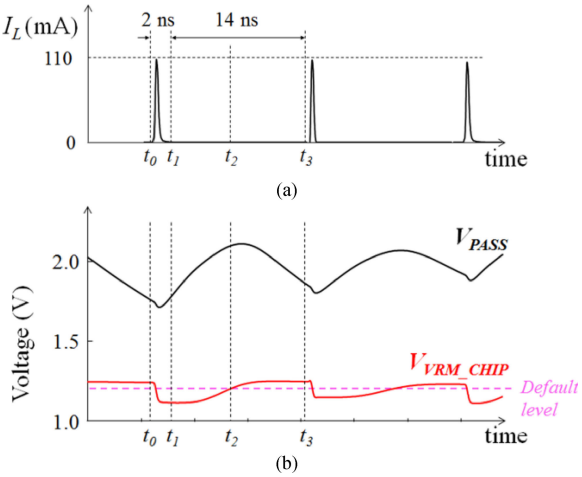

Fig. 2. Transient responses of the typical on-chip linear VRM circuit with a low-speed output buffer as load. (a) Current waveform from the low-speed output buffer at load (I_L). (b) Corresponding voltage waveforms at the on-chip linear VRM output ($V_{\rm VRM\_CHIP}$) and the gate of the pass transistor ($V_{\rm PASS}$).

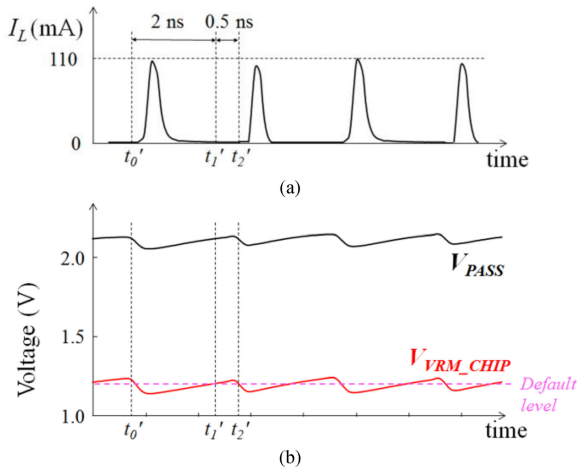

Fig. 3. Transient responses of the typical on-chip linear VRM circuit with high-speed output buffer as load. (a) Current waveform from the high-speed output buffer at load (I_L). (b) Corresponding voltage waveforms at the on-chip linear VRM output ($V_{\rm VRM\_CHIP}$) and the gate of pass transistor ($V_{\rm PASS}$).

$V_{\rm PASS}$ is increased due to the negative feedback loop. It turns ON the pass transistor, resulting in an increased $V_{\rm VRM\_CHIP}$ level by charging $C_{\rm VRM}$; this period is $t_0 < t < t_1$. Even though I_L becomes zero from time t_1, the negative feedback loop keeps increasing $V_{\rm VRM\_CHIP}$ to its default level; this period is $t_1 < t < t_2$. When $V_{\rm VRM\_CHIP}$ reaches its default level at time t_2, the pass transistor current starts decreasing. A noticeable point is that the non-zero current from the pass transistor keeps increasing $V_{\rm VRM\_CHIP}$ until the pass transistor is turned OFF. When the pass transistor is turned OFF, the feedback loop is broken. After that $V_{\rm VRM\_CHIP}$ steadily decreases depending on the *RC* time constant at the load stage. Because the *RC* time constant is usually much longer than the time interval of the I_L pulses, $V_{\rm VRM\_CHIP}$ looks similar to the constant in this period. $V_{\rm PASS}$ decreases for a while because the feedback voltage is higher than $V_{\rm REF}$; this period is $t_2 < t < t_3$. When a new I_L pulse occurs at time t_3, $V_{\rm VRM\_CHIP}$ is rapidly decreased by the discharged $C_{\rm VRM}$. If the decreased $V_{\rm VRM\_CHIP}$ becomes lower than the

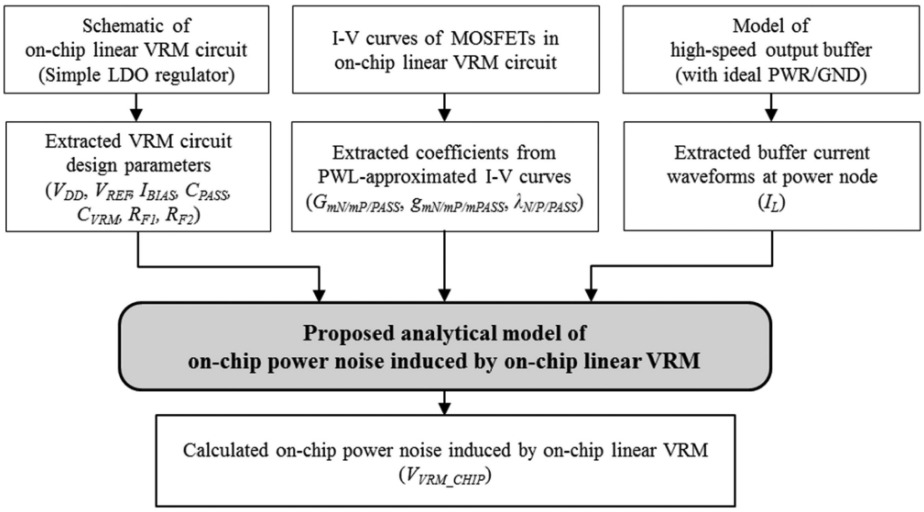

Fig. 4. Calculation procedure of the proposed on-chip power noise model induced by the on-chip linear VRM with high-speed output buffer.

default level, $V_{\rm PASS}$ starts increasing. Then, the fluctuations of the $V_{\rm VRM\_CHIP}$ and the $V_{\rm PASS}$ waveforms between time t_0 and time t_3 are repeated in the same manner.

Fig. 3 shows transient responses of the typical on-chip linear VRM circuit with a high-speed output buffer as load. When I_L from the high-speed output buffer flows, as shown in Fig. 3(a), the fluctuations of $V_{\rm PASS}$ and $V_{\rm VRM\_CHIP}$, which are shown in Fig. 3(b), are different from those of the low-speed output buffer case. The fluctuated waveforms between time t_0' and t_1' are similar to those of the low-speed output buffer case between time t_0 and t_1. During this period, the rapidly reduced $V_{\rm VRM\_CHIP}$ by the I_L pulse increases $V_{\rm PASS}$ and the pass transistor current. It is noteworthy that the pass transistor with a high-speed output buffer is always turned ON, whereas the pass transistor with a low-speed buffer is frequently turned OFF. In the case of the high-speed output buffer, the period between the I_L pulse (t_0'–t_2') is very short. Because a new I_L pulse reduces the $V_{\rm VRM\_CHIP}$ level before the pass transistor is turned OFF, $V_{\rm PASS}$ always maintains a high level. Because this paper assumes that there is no V_{DD} noise, which means no operations in the linear mode, the pass transistor always turns ON and operates in saturation mode. As a result, it is reasonable to assume that the pass transistor of the on-chip linear VRM always operates in saturation mode under the high-speed output buffer operation at load.

III. Proposed Analytical Models of On-Chip Power Noises Induced by the On-Chip Linear VRM

A. Proposed Analytical Models of On-Chip Power Noises Induced by the On-Chip Linear VRM

Fig. 4 shows the calculation procedure of the proposed on-chip power noise model induced by the on-chip linear VRM with a high-speed output buffer. The proposed model requires a schematic of the on-chip linear VRM circuit, *I–V* curves of the MOSFETs in the on-chip linear VRM circuit, and a model of the high-speed aggressor output buffer.

Fig. 5 shows the schematic of the target on-chip linear VRM circuit for modeling. It is a typical on-chip LDO voltage regulator, which consists of a simple error amplifier, a pass transistor, two feedback resistors, and an on-chip decoupling capacitor at load. From the schematic of the on-chip linear VRM circuit shown in Fig. 5, circuit design parameters, such as the on-chip linear VRM input voltage (V_{DD}), reference voltage of error amplifier ($V_{\rm REF}$), bias current of error amplifier ($I_{\rm BIAS}$), gate capacitances of pass transistor ($C_{\rm PASS} = C_{GS\_\rm PASS} + C_{GD\_\rm PASS} + C_{GB\_\rm PASS}$), source-to-body capacitance of pass transistor ($C_{SB\_\rm PASS}$), feedback resistances (R_{F1}, R_{F2}), and on-chip decoupling capacitance ($C_{\rm VRM}$), are extracted for on-chip power noise ($V_{\rm VRM\_CHIP}$) calculation.

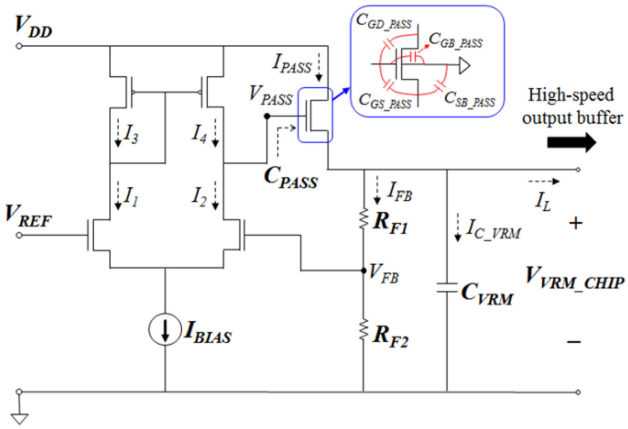

Fig. 5. Schematic of target on-chip linear VRM circuit for modeling, which is the typical LDO voltage regulator circuit.

The high-speed output buffer is located at the output stage of the on-chip linear VRM circuit, as indicated in Fig. 5. The operating high-speed output buffer generates a current waveform at load (I_L), which induces the $V_{\rm VRM\_CHIP}$ fluctuation. For the $V_{\rm VRM\_CHIP}$ calculation, I_L needs to be extracted from transient simulation by using the aggressor output buffer model at load. To reduce the simulation time and complexity, the proposed model employs the ideal power and ground for the high-speed output buffer simulation.

To calculate $V_{\rm VRM\_CHIP}$, closed-form equations are derived. The proposed analytical model employs piecewise linear (PWL)

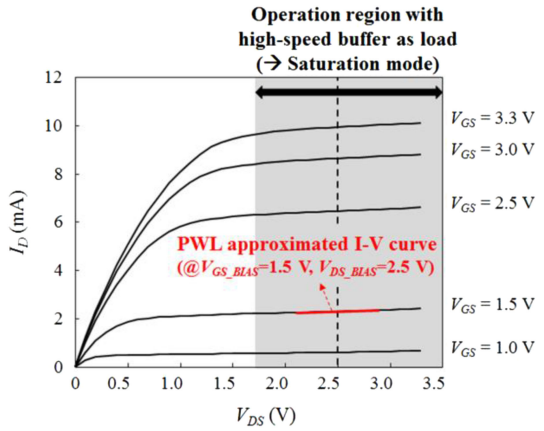

Fig. 6. PWL-approximated NMOS *I–V* curve. The *I–V* curve is simply modeled by a linear equation as long as the high-speed buffer operates at load. The PWL-approximated PMOS *I–V* curve is modeled in the same way.

approximated MOSFET *I–V* curves to derive closed-form equations. A red line in Fig. 6 shows the concept of the PWL-approximated NMOS *I–V* curve at a specific bias condition (V_{GS} of 1.5 V and V_{DS} of 2.5 V). Because MOSFETs mostly operate in saturation mode as long as the high-speed buffer operates at load and there is no V_{DD} noise, the non-linear *I–V* curve is simply modeled by the following linear equation:

$$I_D = I_{D0} + g_m V_{GS} + \lambda V_{DS} \tag{2}$$

where

$$I_{D0} = (G_m - g_m)\, V_{GS\_\mathrm{BIAS}} - \lambda V_{DS\_\mathrm{BIAS}} \tag{2a}$$

$$G_m = \frac{I_D}{V_{GS}} \tag{2b}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2c}$$

$$\lambda = \frac{\partial I_D}{\partial V_{DS}} \tag{2d}$$

$$V_{GS} = V_{GS\_\mathrm{BIAS}} + \Delta V_{GS} \tag{2e}$$

$$V_{DS} = V_{DS\_\mathrm{BIAS}} + \Delta V_{DS}. \tag{2f}$$

The coefficients G_m, g_m, and λ refer to large-signal trans-conductance, small-signal trans-conductance, and the channel-length modulation factors, as shown in (2b), (2c), and (2d), respectively [23], [24]. If the amounts of voltage fluctuations at each MOSFET node are sufficiently small, dc biases of each node can be defined. Under this condition, V_{GS} and V_{DS} are defined as (2e) and (2f), respectively. V_{GS_BIAS} and V_{DS_BIAS} are dc bias voltages of V_{GS} and V_{DS}, respectively. I_{D0} in (2a) indicates an offset drain current of an NMOS. The non-linear *I–V* curve of PMOS is also modeled in the same manner. The proposed analytical model requires the NMOS coefficients of the error amplifier (G_{mN}, g_{mN}, λ_N, and I_{D0N}), PMOS coefficients of the error amplifier (G_{mP}, g_{mP}, and λ_P, I_{D0P}), and coefficients of the pass transistor ($G_{m\mathrm{PASS}}$, $g_{m\mathrm{PASS}}$, λ_{PASS}, and I_{D0PASS}).

Following equations indicate the linearized equations of the drain currents of each MOSFET (I_1, I_2, I_3, I_4, and I_{PASS} in Fig. 5) based on the PWL-approximated MOSFET *I–V* curves:

$$\begin{aligned} I_1(t) &= I_{D0N} + g_{mN} \times (V_{\mathrm{REF}}(t) - V_S(t)) \\ &\quad + \lambda_N \times (V_G(t) - V_S(t)) \end{aligned} \tag{3}$$

$$\begin{aligned} I_2(t) &= I_{D0N} + g_{mN} \times (V_{FB}(t) - V_S(t)) \\ &\quad + \lambda_N \times (V_{\mathrm{PASS}}(t) - V_S(t)) \end{aligned} \tag{4}$$

$$\begin{aligned} I_3(t) &= I_{D0P} + g_{mP} \times (V_G(t) - V_{DD}(t)) \\ &\quad + \lambda_P \times (V_G(t) - V_{DD}(t)) \end{aligned} \tag{5}$$

$$\begin{aligned} I_4(t) &= I_{D0P} + g_{mP} \times (V_G(t) - V_{DD}(t)) \\ &\quad + \lambda_P \times (V_{\mathrm{PASS}}(t) - V_{DD}(t)) \end{aligned} \tag{6}$$

$$\begin{aligned} I_{\mathrm{PASS}}(t) &= I_{D0\mathrm{PASS}} + g_{m\mathrm{PASS}} \times \big(V_{\mathrm{PASS}}(t) \\ &\quad - V_{\mathrm{VRM\_CHIP}}(t)\big) + \lambda_{\mathrm{PASS}} \times \big(V_{DD}(t) \\ &\quad - V_{\mathrm{VRM\_CHIP}}(t)\big). \end{aligned} \tag{7}$$

From the schematic shown in Fig. 5, we can build additional equations of currents at the other branches and feedback voltage (V_{FB}) node as

$$\begin{aligned} &I_4(t) - I_2(t) + C_{GD\_\mathrm{PASS}} \frac{dV_{DD}(t) - dV_{\mathrm{PASS}}(t)}{dt} \\ &= C_{GS\_\mathrm{PASS}} \frac{dV_{\mathrm{PASS}}(t) - dV_{\mathrm{VRM\_CHIP}}(t)}{dt} \\ &\quad + C_{GB\_\mathrm{PASS}} \frac{dV_{\mathrm{PASS}}(t)}{dt} \end{aligned} \tag{8}$$

$$\begin{aligned} I_L(t) &= I_{\mathrm{PASS}}(t) + C_{GS\_\mathrm{PASS}} \frac{dV_{\mathrm{PASS}}(t) - dV_{\mathrm{VRM\_CHIP}}(t)}{dt} \\ &\quad + C_{SB\_\mathrm{PASS}} \frac{dV_{\mathrm{VRM\_CHIP}}(t)}{dt} - \frac{V_{\mathrm{VRM\_CHIP}}(t)}{R_{F1} + R_{F2}} \\ &\quad + C_{\mathrm{VRM}} \frac{dV_{\mathrm{VRM\_CHIP}}(t)}{dt} \end{aligned} \tag{9}$$

$$I_1(t) = I_3(t) \tag{10}$$

$$I_{\mathrm{BIAS}}(t) = I_1(t) + I_2(t) \tag{11}$$

$$V_{FB}(t) = \frac{R_{F2}}{R_{F1} + R_{F2}} V_{\mathrm{VRM\_CHIP}}(t). \tag{12}$$

The currents at pass transistor gate and VRM output are modeled by (8) and (9), respectively. The size of the pass transistor is usually much larger than the MOSFETs in the error amplifier. This means that the impact of the parasitic capacitances on the error amplifier is negligible. Because the gate currents of the PMOSs in the error amplifier should be almost zero, I_1 is almost the same as I_3; it is modeled by (10). Equation (11) indicates the relationship between I_1, I_2, and I_{BIAS}. V_{FB} is obtained from voltage dividing at feedback resistors: it is modeled by (12). Because there are ten unknown ($I_1, I_2, I_3, I_4, I_{\mathrm{PASS}}, V_G, V_S, V_{\mathrm{PASS}}$, V_{FB}, and $V_{\mathrm{VRM\_CHIP}}$) and 10 known equations, a closed-form equation of $V_{\mathrm{VRM\_CHIP}}$ can be derived.

From (3)–(12), a second-order differential equation for $V_{\mathrm{VRM\_CHIP}}$ is obtained as (13). This second-order differential

equation has five solutions:

$$\frac{d^2V_{\mathrm{VRM\_CHIP}}(t)}{dt^2}+m_1\frac{dV_{\mathrm{VRM\_CHIP}}(t)}{dt}+m_2V_{\mathrm{VRM\_CHIP}}(t)$$
$$=y_{\mathrm{VRM\_CHIP\_DC}}+y_{\mathrm{VRM\_CHIP}\_IL}(t)$$
$$+\ y_{\mathrm{VRM\_CHIP}\_VDD}(t)+y_{\mathrm{VRM\_CHIP}\_V\mathrm{REF}}(t) \tag{13}$$

$$y_{\mathrm{VRM\_CHIP\_DC}}=\frac{1}{C_{\mathrm{PASS}}}\Big[g_{mN}g_{m\mathrm{PASS}}V_{\mathrm{REF0}}+(\lambda_N+\lambda_P)$$
$$(g_{m\mathrm{PASS}}+\lambda_{\mathrm{PASS}})V_{DD0}-\frac{(\lambda_N+\lambda_P)(I_{\mathrm{BIAS}}-2I_{D0P})}{(2g_{mP}+\lambda_N+2\lambda_P)}$$
$$g_{m\mathrm{PASS}}+(\lambda_N+\lambda_P)I_{D0\mathrm{PASS}}\Big] \tag{13a}$$

$$y_{\mathrm{VRM\_CHIP}\_IL}=m_3\frac{dI_L(t)}{dt}+m_4I_L(t) \tag{13b}$$

$$y_{\mathrm{VRM\_CHIP}\_VDD}=m_5\frac{d^2V_{DDN}(t)}{dt^2}+m_6\frac{dV_{DDN}(t)}{dt}$$
$$+\ m_7V_{DDN}(t) \tag{13c}$$

$$y_{\mathrm{VRM\_CHIP}\_V\mathrm{REF}}=m_8\frac{dV_{\mathrm{REF}N}(t)}{dt}+m_9V_{\mathrm{REF}N}(t) \tag{13d}$$

$$V_{\mathrm{VRM\_CHIP}}(t)=V_{\mathrm{VRM\_CHIP\_DC}}+V_{\mathrm{VRM\_CHIP}\_IL}(t)$$
$$+V_{\mathrm{VRM\_CHIP}\_VDD}(t)+V_{\mathrm{VRM\_CHIP}\_V\mathrm{REF}}(t) \tag{14}$$

The terms $y_{\mathrm{VRM\_CHIP\_DC}}$, $y_{\mathrm{VRM\_CHIP}\_IL}(t)$, $y_{\mathrm{VRM\_CHIP}\_VDD}(t)$, and $y_{\mathrm{VRM\_CHIP}\_V\mathrm{REF}}(t)$ indicate the dc level of $V_{\mathrm{VRM\_CHIP}}$, load current (I_L) impact, off-chip power (V_{DD}) impact, and reference voltage (V_{REF}) impact, respectively. Each noise source independently affects $V_{\mathrm{VRM\_CHIP}}$. The coefficients p, q, and s can be replaced by G_m, g_m, and λ, respectively, because the MOSFETs in the on-chip linear VRM mostly operate in saturation mode as long as the high-speed buffer operates at load. Detailed equations for coefficients m_1 to m_9 are listed in the Appendix. V_{REF0} and V_{DD0} are dc components of V_{REF} and V_{DD}, respectively. $V_{\mathrm{REF}N}$ and V_{DDN} are ac components of V_{REF} and V_{DD}, respectively. The homogeneous solution of (13) only affects the early transition state due to the exponential terms, which means that it is eliminated in steady state. If we focus on the noise in steady state, particular solutions for each noise term in (13) correspond to the analytical models of the on-chip linear VRM output noises induced by each noise source. Then, an analytical model of $V_{\mathrm{VRM\_CHIP}}$ is derived as (14). $V_{\mathrm{VRM\_CHIP\_DC}}$, $V_{\mathrm{VRM\_CHIP}\_IL}(t)$, $V_{\mathrm{VRM\_CHIP}\_VDD}(t)$, and $V_{\mathrm{VRM\_CHIP}\_V\mathrm{REF}}(t)$ indicate the default dc level of the VRM output, VRM output noise waveform induced by the load current, VRM output noise waveform induced by off-chip power noise, and VRM output noise induced by reference voltage noise, respectively. Equations (15)–(18) shown at bottom of this page, are the detailed equations for (14).

$$V_{\mathrm{VRM\_CHIP\_DC}}=\left(1+\frac{R_{F2}}{R_{F1}}\right)V_{\mathrm{REF\_0}}+\left(1+\frac{R_{F2}}{R_{F1}}\right)\frac{(\lambda_N+\lambda_P)}{g_{mN}g_{m\mathrm{PASS}}}\Bigg[(g_{m\mathrm{PASS}}+\lambda_{\mathrm{PASS}})V_{DD0}+I_{D0\mathrm{PASS}}$$
$$-\frac{I_{\mathrm{BIAS}}-2I_{D0P}}{2g_{mP}+2\lambda_P+\lambda_N}g_{m\mathrm{PASS}}\Bigg] \tag{15}$$

$$V_{\mathrm{VRM\_CHIP}\_IL}(t)=\sum_n i_{L(n)}\times\frac{\sqrt{(m_3\omega_n)^2+{m_4}^2}}{\sqrt{(m_1\omega_n)^2+(m_2-{\omega_n}^2)^2}}\cos\left(\omega_nt+\varphi_n+\mathrm{atan2}\left(m_2-\omega_n^2,m_1\omega_n\right)-\mathrm{atan2}\left(m_4,m_3\omega_n\right)\right),$$
$$\text{where } I_L(t)=\sum_n i_{L(n)}\cos(\omega_nt+\varphi_n) \tag{16}$$

$$V_{\mathrm{VRM\_CHIP}\_VDD}(t)=\sum_n v_{DD(n)}\times\frac{\sqrt{(m_6\omega_n)^2+(m_5{\omega_n}^2-m_7)^2}}{\sqrt{(m_1\omega_n)^2+(m_2-{\omega_n}^2)^2}}\cos\big(\omega_nt+\varphi_n+\mathrm{atan2}\left(m_2-{\omega_n}^2,m_1\omega_n\right)$$
$$+\ \mathrm{atan2}\left(m_5{\omega_n}^2-m_7,m_6\omega_n\right)\big),$$
$$\text{where } V_{DDN}(t)=\sum_n v_{DD(n)}\cos(\omega_nt+\varphi_n) \tag{17}$$

$$V_{\mathrm{VRM\_CHIP}\_V\mathrm{REF}}(t)=\sum_n v_{\mathrm{REF}(n)}\times\frac{\sqrt{(m_8\omega_n)^2+{m_9}^2}}{\sqrt{(m_1\omega_n)^2+(m_2-{\omega_n}^2)^2}}\cos\big(\pi+\omega_nt+\varphi_n+\mathrm{atan2}\left(m_2-{\omega_n}^2,m_1\omega_n\right)$$
$$+\ \mathrm{atan2}\left(m_9,m_8\omega_n\right)\big)\text{where,}$$
$$V_{\mathrm{REF}N}(t)=\sum_n v_{\mathrm{REF}(n)}\cos(\omega_nt+\varphi_n). \tag{18}$$

TABLE I
SIMULATION AND DESIGN PARAMETERS OF THE ON-CHIP LINEAR VRM

Symbol	Value	Symbol	Value
I_{D0N}	-0.0092 A	R_{F1}	1 kΩ
g_{mN}	0.0078 S	R_{F2}	5.4 kΩ
λ_N	85 μA/V	V_{DD0}	3.3 V
I_{D0P}	-0.0025 A	V_{REF0}	1.0 V
g_{mP}	-0.0042 S	I_{BIAS}	0.9 mA
λ_P	-40 μA/V	C_{VRM}	300 pF
Symbol	Value	Symbol	Value
I_{D0PASS}	-0.0326 A	C_{GS_PASS}	2.85 pF
g_{mPASS}	0.0432 S	C_{GD_PASS}	1.5 pF
λ_{PASS}	717 μA/V	C_{GB_PASS}	3 pF
		C_{SB_PASS}	6.2 pF

B. Simulation-Based Validation of the Proposed Analytical Models

To validate the proposed analytical model, an on-chip linear VRM circuit shown in Fig. 5 was designed with 110-nm CMOS technology. To demonstrate the accuracy of the proposed model, the VRM circuit and the output buffer were designed to have large on-chip power noises. The simulation and design parameters of the on-chip linear VRM circuit are given in Table I. Coefficients of the PWL-approximated *I–V* curves are extracted from SPICE-based ac simulation. The VRM input voltage and reference voltage are 3.3 and 1.0 V, respectively. The default dc level of the on-chip linear VRM output is 1.2 V. The amount of on-chip decoupling capacitance at load ($C_{\rm VRM}$) is 300 pF. To generate a load current from the aggressor high-speed output buffer (I_L), a clock signal is employed as the aggressor buffer input sequences. The speed of the clock signal is 400 MHz. Under high-speed output buffer operation, a single-tone off-chip power (V_{DD}) noise and a single-tone reference voltage ($V_{\rm REF}$) noise are additionally added in simulation. The peak-to-peak amounts of V_{DD} noise and $V_{\rm REF}$ noise are 100 and 4 mV, respectively. The frequencies of V_{DD} noise and $V_{\rm REF}$ noise are the same at 50 MHz.

Fig. 7 shows the simulated $V_{\rm VRM\_CHIP}$ using the SPICE simulation and the proposed analytical model. The black and red curves indicate the on-chip power noise waveforms obtained from the SPICE simulations and proposed model, respectively. The blue curve shows the load current waveform. The arrows in each plot point represent the axes for each curve. Fig. 7(a) shows the simulated $V_{\rm VRM\_CHIP}$ induced by a load current. The simulated on-chip power noise waveform using the proposed analytical model shows good correlation with the SPICE simulation result. The trend of $V_{\rm VRM\_CHIP}$ induced by the load current is almost the same as the waveform shown in Fig. 3(b). The $V_{\rm VRM\_CHIP}$ level is mostly smaller than its default value of 1.2 V because the load current generated by the high-speed output buffer constantly reduces the $V_{\rm VRM\_CHIP}$ level. Thus, the pass transistor is mostly turned ON and operates in saturation mode. Fig. 7(b) and (c) shows the simulated $V_{\rm VRM\_CHIP}$ induced by a load current, as well as a single-tone off-chip power noise and a single-tone $V_{\rm REF}$ noise, respectively. The overall trend of the simulated $V_{\rm VRM\_CHIP}$ by utilizing the proposed model shows good correlation to the SPICE simulation results.

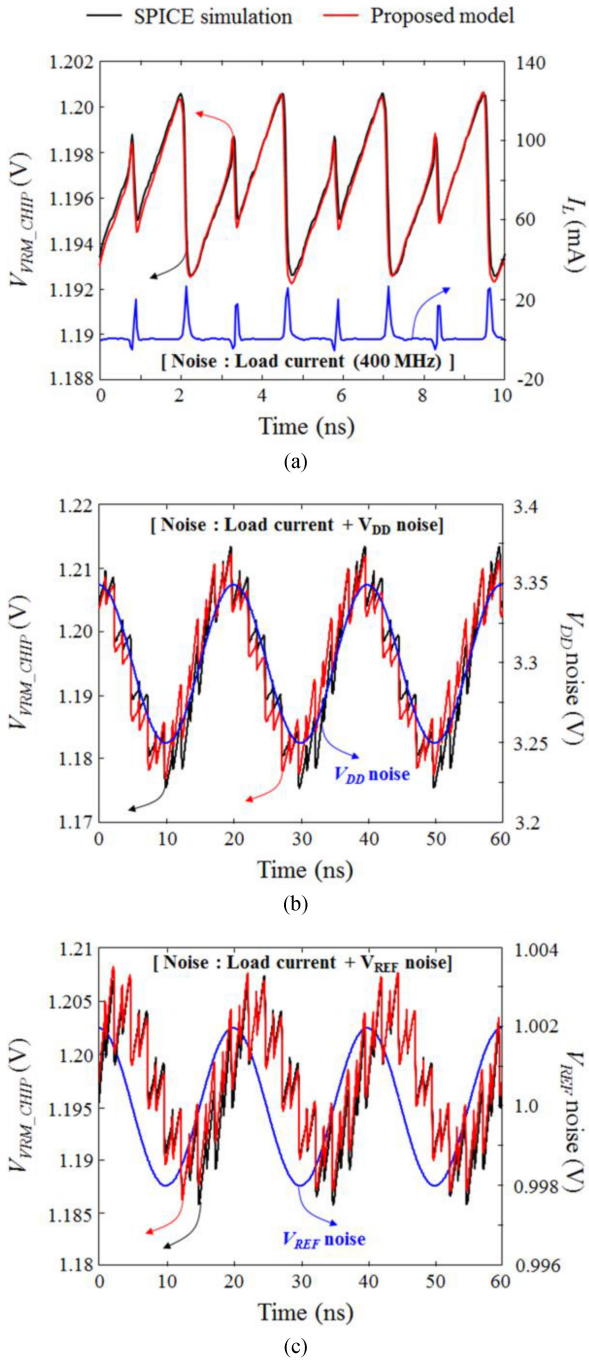

Fig. 7. Simulated on-chip power noises induced by the on-chip linear VRM ($V_{\rm VRM\_CHIP}$) using SPICE simulation and the proposed analytical models. Noise sources for each case are (a) load current only, (b) load current and off-chip power (V_{DD}) noise, and (c) load current and reference voltage ($V_{\rm REF}$) noise.

However, the exact waveform is slightly different, especially in the case of off-chip power noise, because a considerable portion of the induced on-chip power noise waveform is higher than 1.2 V. The VRM output voltage level higher than 1.2 V means that the pass transistor approaches cut-off mode. Even though the high-speed output buffer operates at load, we cannot guarantee the saturation mode operation of the pass transistor under sufficiently large external noises. As the amounts of the off-chip

power and reference voltage noises increase, the pass transistor can be turned OFF for a longer period of time, resulting in the larger discrepancy of the proposed analytical models. From (8) and (14), the gate voltage of the pass transistor ($V_{\rm PASS}$) fluctuated by external noises can be calculated. To guarantee the saturation mode operation of the pass transistor, $V_{\rm PASS-}V_{\rm OUT}$ should be larger than the threshold voltage of the pass transistor.

Even though 400 MHz in this validation section is not a high speed as per today's standards, this paper utilizes this buffer speed to clearly demonstrate the accuracy of the proposed model because the amount of power noise is decreased as the speed goes up. The details regarding this characteristic are explained in Section IV.

IV. Analysis of On-Chip Power Noise Induced by an On-Chip Linear VRM With a High-Speed Output Buffer

In this section, on-chip power noise induced by an on-chip linear VRM is simulated and analyzed based on the proposed analytical models. The analysis focuses on load current (I_L) and external noise impacts on the on-chip power noise induced by the on-chip linear VRM. The off-chip power (V_{DD}) and reference voltage of the on-chip linear VRM ($V_{\rm REF}$) are selected as the external noise sources. In addition, design guidance to reduce on-chip power noise induced by the on-chip linear VRM is discussed.

A. Load Current Impact on the On-Chip Power Noise Induced by the On-Chip Linear VRM

The proposed model (16) indicates on-chip power noise at the VRM output induced by the load current. Because $V_{\rm VRM\_CHIP\_}{}_{IL}$ and I_L correspond to the voltage and current at the on-chip linear VRM output node, respectively, the ratio between them becomes self-impedance (Z_{11}) at the on-chip linear VRM output. From (16), the magnitude and phase expressions of Z_{11} at the on-chip linear VRM output are derived as

$$\text{mag}\left[Z_{11}(\omega)\right] = \frac{\sqrt{(m_3\omega)^2 + {m_4}^2}}{\sqrt{(m_1\omega)^2 + (m_2-\omega^2)^2}} \tag{19}$$

$$\text{phase}\left[Z_{11}(\omega)\right] = \text{atan2}\left(m_2-\omega^2, m_1\omega\right) - \text{atan2}\left(m_4, m_3\omega\right). \tag{20}$$

Simulated Z_{11} values at the on-chip linear VRM output using the SPICE simulation and (19) and (20) are shown in Fig. 8. The simulated magnitude and phase of Z_{11} using the proposed model show very good correlation to the SPICE simulation results. While the resonant peak of 29 Ω is overpredicted by the proposed model (predicted value = 36 Ω), the resonant frequency of 56 MHz is precisely predicted within 1.5 MHz.

At the very low frequency range near dc, the ω term is almost negligible. Then, (19) is simplified to a ratio between m_4 and m_2, which is an equation for the dc characteristic of Z_{11} at the on-chip linear VRM output ($Z_{\rm DC}$). From (A2) and (A4), the corresponding equation is derived as

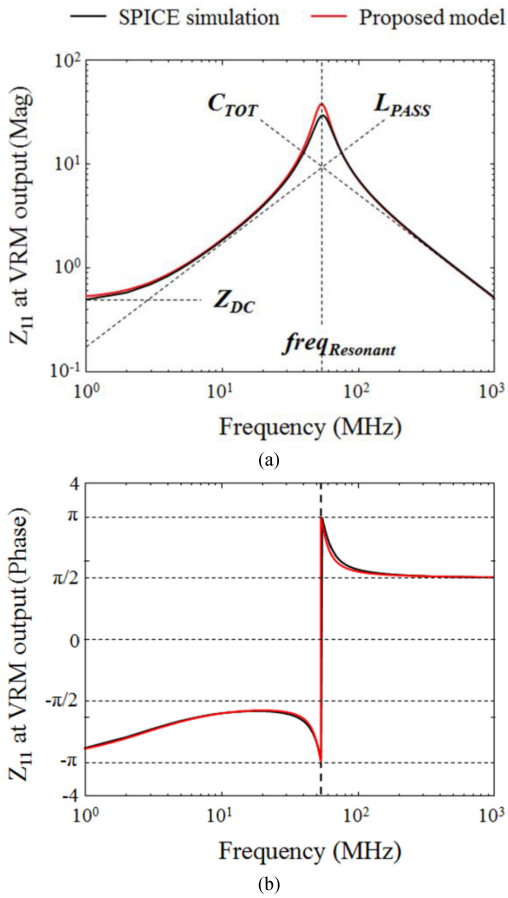

Fig. 8. Simulated self-impedances (Z_{11}) at the on-chip linear VRM output using the SPICE simulation and the proposed models in (19) and (20). (a) Z_{11} magnitudes. (b) Z_{11} phases. The magnitude curve is determined by $Z_{\rm DC}$, $C_{\rm TOT}$, and $L_{\rm PASS}$, which are calculated by (21), (23), and (24), respectively.

$$Z_{\rm DC} = \frac{\lambda_N + \lambda_P}{g_{mN}g_{m\rm PASS}}\left(1+\frac{R_{F1}}{R_{F2}}\right). \tag{21}$$

Z_{11} at the on-chip linear VRM output should be minimized to reduce the on-chip power noise. To reduce Z_{11} from dc to the low-frequency range, $Z_{\rm DC}$ should be minimized. A simple way to reduce $Z_{\rm DC}$ is to enlarge the pass transistor size, which increases the trans-conductance of pass transistor ($g_{m\rm PASS}$).

The denominator of (19) can be simplified to ($m_2-\omega^2$) because ($m_1\omega$) is usually much smaller than ($m_2-\omega^2$). When m_2 equals ω^2, Z_{11} becomes maximized, which means a resonant peak appears. From (A2), the equation of the resonant frequency of Z_{11} at the on-chip linear VRM output ($\text{freq}_{\rm Resonant}$) (22) is derived as

$$\text{freq}_{\rm Resonant} = \frac{1}{2\pi\sqrt{C_{TOT}L_{\rm PASS}}} \tag{22}$$

$$C_{\rm TOT} = C_{\rm VRM} + C_{GS\_\rm PASS} + C_{SB\_\rm PASS} \tag{23}$$

$$L_{\rm PASS} \approx \frac{C_{\rm PASS}}{g_{mN}g_{m\rm PASS}}\left(1+\frac{R_{F1}}{R_{F2}}\right). \tag{24}$$

$\text{freq}_{\text{Resonant}}$ should be far from the peak frequency of the aggressor current spectrum to reduce the on-chip power noise. $\text{freq}_{\text{Resonant}}$ is determined by the total capacitances at load (C_{TOT}) and active inductance of the pass transistor (L_{PASS}). Even though L_{PASS} is simply adjusted by changing the pass transistor size, it is hard to freely change because the allowable load current is determined by pass transistor size. Thus, adjustment of C_{TOT} is an easier way to control $\text{freq}_{\text{Resonant}}$ than L_{PASS}. In general, C_{GS_PASS} and C_{SB_PASS} are much smaller than C_{VRM}, which means that C_{TOT} almost equals C_{VRM}. Under the given aggressor current spectrum, the Z_{11} resonant frequency can avoid the peak current frequency by simply adjusting the amount of C_{VRM}.

B. Off-Chip Power Noise Impact on On-Chip Power Noise Induced by the On-Chip Linear VRM

The proposed model (17) indicates the on-chip VRM output noise induced by off-chip power noise. In the same manner as the Z_{11} model derivation, an analytical model of the voltage noise transfer function from the off-chip PDN to on-chip linear VRM output ($H_{\text{VRM\_CHIP\_VDD}}$) is derived as (25) and (26). To consider peak-to-peak noise, the magnitude expression is increased by a factor of 2

$$|H_{\text{VRM\_CHIP\_VDD}}(\omega)| = 2 \times \frac{\sqrt{(m_6\omega)^2 + (m_5\omega^2 - m_7)^2}}{\sqrt{(m_1\omega)^2 + (m_2 - \omega^2)^2}} \tag{25}$$

$$\angle H_{\text{VRM\_CHIP\_VDD}}(\omega) = \text{atan}\left(\frac{m_2 - \omega^2}{m_1\omega}\right) + \text{atan}\left(\frac{m_5\omega^2 - m_7}{m_6\omega}\right). \tag{26}$$

Simulated magnitude and phase of $H_{\text{VRM\_CHIP\_VDD}}$ using (25) and (26) are shown in Fig. 9. $H_{\text{VRM\_CHIP\_VDD}}$ can be divided into three regions: the low-frequency region below several tens of MHz, mid-frequency region from several tens of MHz to several hundred MHz, and high-frequency region over several hundred MHz. Fig. 9 indicates which expressions determine the noise transfer function curves at each frequency region.

$H_{\text{VRM\_CHIP\_VDD}}$ at the low-frequency region is frequency independent. It is a function of λ_N, λ_P, g_{mN}, R_{F1}, and R_{F2}. Even though the reduced (R_{F1}/R_{F2}) term decreases the magnitude of the noise transfer function, the (R_{F1}/R_{F2}) term is difficult to adjust because it directly determines the dc level of the VRM output. λ_N, λ_P, and g_{mN} are MOSFET parameters of the error amplifier. When we choose MOSFETs with small λ_N and λ_P and large g_m for error amplifier design, $H_{\text{VRM\_CHIP\_VDD}}$ at the low-frequency region can be reduced.

From the mid-frequency region over several tens of MHz, impacts of parasitic capacitances arise. Off-chip power noise that passes through C_{GD_PASS} fluctuates the voltage at the pass transistor gate, resulting in on-chip linear VRM output fluctuation. Because $H_{\text{VRM\_CHIP\_VDD}}$ has an inductance characteristic at several tens of MHz, as shown in Fig. 9, its magnitude increases as the frequency goes up. As the frequency goes up more, impacts of capacitances, including C_{VRM}, become dominant, resulting in a resonance of the noise transfer function. A noticeable point is that the resonant frequency of $H_{\text{VRM\_CHIP\_VDD}}$ equals that of Z_{11} at the VRM output. Because the denominator expressions of (19) and (25) are the same, their resonant frequencies, where the denominator equals zero, also become identical. The same resonant frequencies of Z_{11} at the VRM output and $H_{\text{VRM\_CHIP\_VDD}}$ enable efficient VRM output noise control. Under the given spectrums of the high-speed load current and off-chip power noise, peak frequencies of the spectrums can be extracted. Then, the VRM output noises induced by the load current and off-chip power noise can be minimized at the same time by avoiding the resonant frequency from the extracted peak frequencies of those spectrums.

Most high-frequency noise transfers through parasitic capacitances due to their low impedances at the high-frequency region. Thus, $H_{\text{VRM\_CHIP\_VDD}}$ at high frequency over several GHz converges to a specific level determined by a ratio between

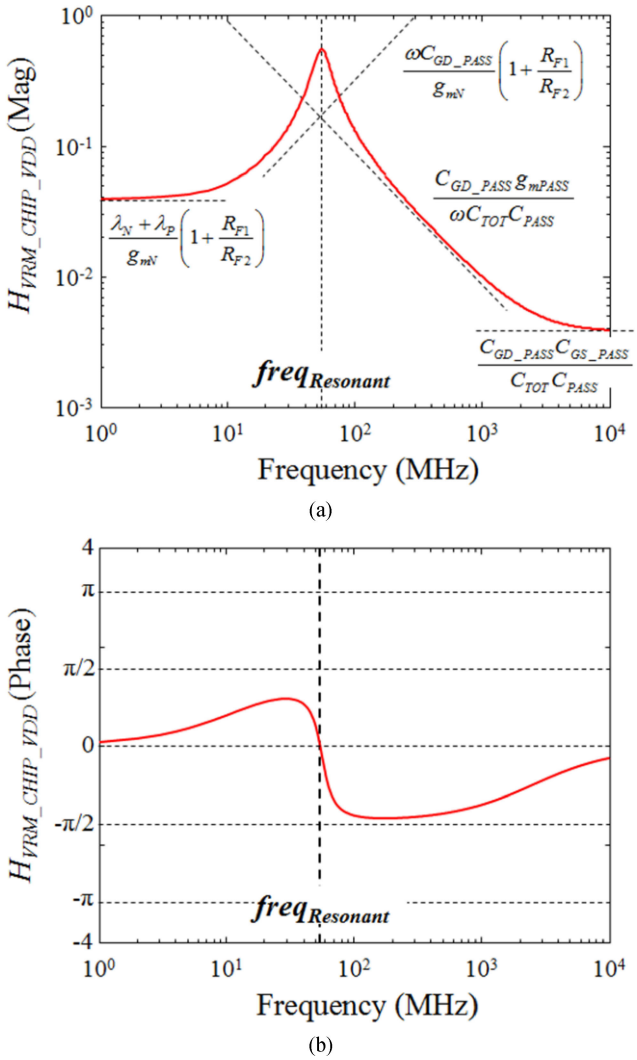

Fig. 9. Simulated voltage noise transfer function from off-chip PDN to on-chip linear VRM output ($H_{\text{VRM\_CHIP\_VDD}}$). (a) Magnitude. (b) Phase. The expressions that determine $H_{\text{VRM\_CHIP\_VDD}}$ at each frequency region are indicated.

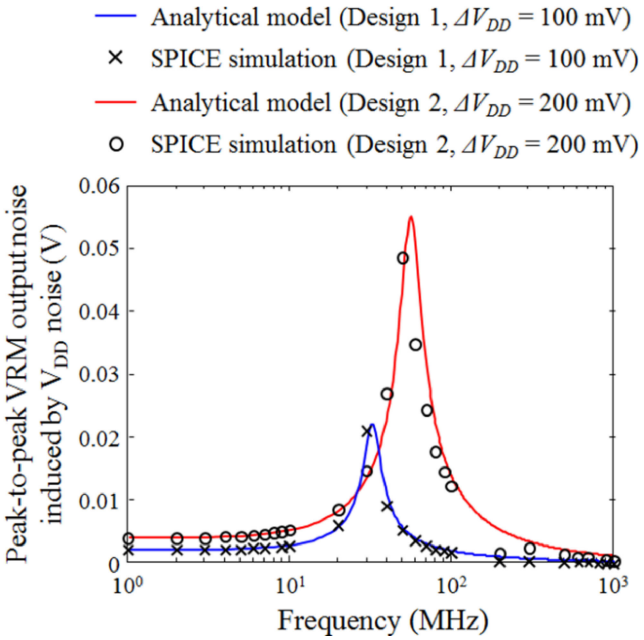

Fig. 10. Simulated peak-to-peak VRM output noise induced by off-chip power (V_{DD}) noise. To verify the proposed analytical model, the noises are estimated by using the SPICE model and (25). Two different VRM designs and different amounts of off-chip power noises (ΔV_{DD}) are employed for verification.

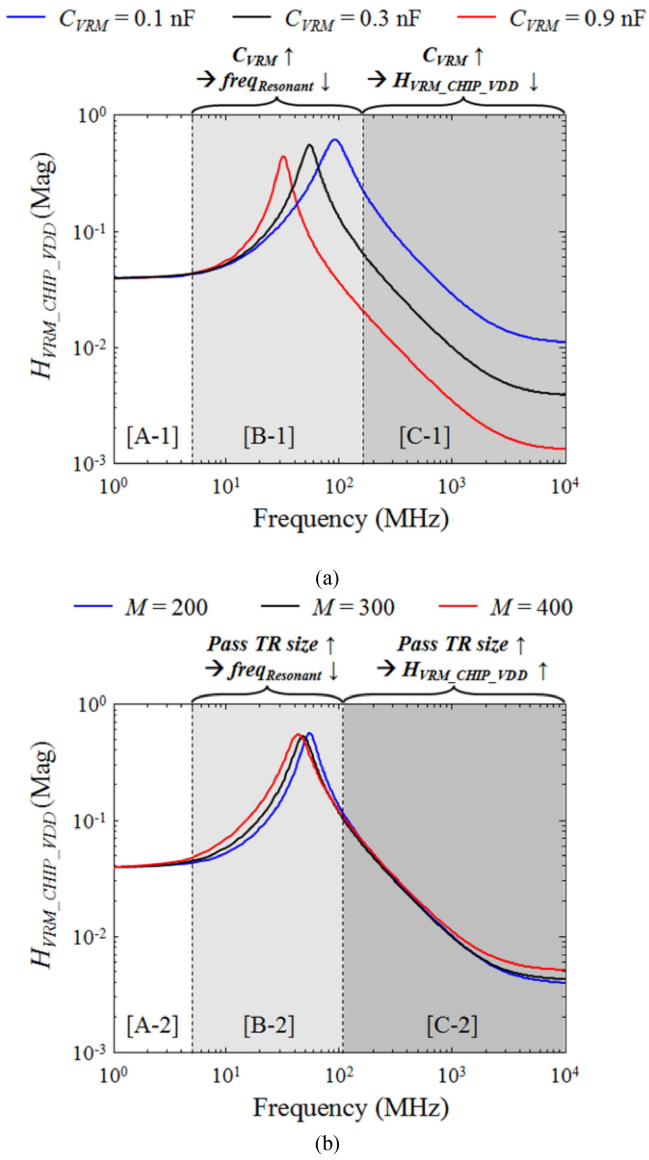

Fig. 11. Simulated $H_{\mathrm{VRM\_CHIP\_VDD}}$ with different VRM design parameters. On-chip decoupling capacitance at (a) load (C_{VRM}) variations and (b) pass transistor size variations. *M* is the multiplication factor that determines the pass transistor size.

parasitic capacitances of the pass transistor and C_{VRM}. To reduce $H_{\mathrm{VRM\_CHIP\_VDD}}$ at the high-frequency region, we need to adjust the amounts of the capacitances. If C_{PASS} is changed by adjusting the pass transistor size, C_{GS_PASS} and C_{GD_PASS} are also changed in the identical ratio. An effective way to reduce $H_{\mathrm{VRM\_CHIP\_VDD}}$ at high frequency is to increase C_{VRM}.

The phase of $H_{\mathrm{VRM\_CHIP\_VDD}}$ has an increasing trend below the resonant frequency due to the inductive characteristic, similar to Z_{11} shown in Fig. 8(b). Because $m_6\omega$ is still much larger than $(m_5\omega^2 - m_7)$ at the resonant frequency, the phase of $H_{\mathrm{VRM\_CHIP\_VDD}}$ is almost zero near the resonant frequency. As the frequency approaches the high-frequency range, the phase approaches zero because two atan() terms approach $-\pi$ and π, respectively, and they are cancelled out.

To validate the proposed analytical model of $H_{\mathrm{VRM\_CHIP\_VDD}}$, peak-to-peak amounts of VRM output noises with different noise frequencies are simulated based on the SPICE model. An aggressor buffer at load operates with a 400-MHz clock signal to see the off-chip noise (ΔV_{DD}) impact under high-speed output buffer operation. The VRM output noise induced by off-chip power noise is extracted by subtracting the VRM output noise only induced by the load current from the total VRM output noise. Fig. 10 shows the estimated peak-to-peak VRM output noises induced by off-chip power noise using SPICE simulation and (25). Two different VRM designs and different amounts of off-chip power noises are employed for verification. The estimated noises using the proposed analytical model show good correlation with those using the SPICE simulation. The proposed analytical model precisely estimates the noise transfer function from the off-chip PDN to the on-chip VRM output as long as the off-chip power noise is sufficiently small to guarantee the pass transistor operation in saturation mode. If the amount of off-chip power noise is considerably large, the proposed model may estimate inaccurate VRM output noise due to the pass transistor operation in cut-off mode.

Fig. 11(a) and (b) shows simulated $H_{\mathrm{VRM\_CHIP\_VDD}}$ with different C_{VRM} and pass transistor sizes, respectively. *M* refers to the multiplication factor of a MOSFET that determines the pass transistor size. $H_{\mathrm{VRM\_CHIP\_VDD}}$ at the low-frequency region is independent of C_{VRM}, as analyzed in Fig. 9. Thus, $H_{\mathrm{VRM\_CHIP\_VDD}}$ at region [A-1] is constant regardless of C_{VRM}, as shown in Fig. 11(a). There is a resonance at the mid-frequency region [B-1]. Because the resonant frequency is inversely proportional to C_{TOT}, as shown in (22), larger C_{VRM}

leads to reduced resonant frequency. At the high-frequency region [C-1], the magnitude of $H_{\mathrm{VRM\_CHIP\_VDD}}$ drops as C_{VRM} increases. As analyzed in Fig. 9, the magnitude of $H_{\mathrm{VRM\_CHIP\_VDD}}$ is inversely proportional to C_{TOT} at high frequency. The larger C_{VRM} leads to larger C_{TOT}, resulting in smaller $H_{\mathrm{VRM\_CHIP\_VDD}}$.

Similar to the C_{VRM} case, $H_{\mathrm{VRM\_CHIP\_VDD}}$ at low frequency is also independent of the pass transistor design. Thus, $H_{\mathrm{VRM\_CHIP\_VDD}}$ at region [A-2] is constant regardless of the pass transistor size, as shown in Fig. 11(b). In the case of the resonant frequency at region [B-2], C_{GS_PASS}, C_{SB_PASS}, C_{PASS}, and $g_{m\mathrm{PASS}}$, which are terms dependent upon the pass transistor size, determine the resonant frequency, as indicated in (23) and (24). Because C_{VRM} is much larger than C_{GS_PASS} and C_{SB_PASS}, in general, C_{TOT} in (23) is almost independent of the pass transistor size. The amount of C_{PASS} is proportional to the pass transistor size, whereas $g_{m\mathrm{PASS}}$ is affected by not only the pass transistor size but also by the bias voltages. Thus, when the pass transistor size increases under fixed load current, the increment of $g_{m\mathrm{PASS}}$ is smaller than that of C_{PASS}. As a result, the resonant frequency decreases as the pass transistor size enlarges. The amount of change is small compared to the C_{VRM} case. At the high-frequency region [C-2], the magnitude of $H_{\mathrm{VRM\_CHIP\_VDD}}$ rises as the pass transistor size increases. C_{TOT} is almost constant regardless of the pass transistor size, whereas C_{GS_PASS}, C_{SB_PASS}, C_{PASS}, and $g_{m\mathrm{PASS}}$ rise as the pass transistor size increases. It results in the higher $H_{\mathrm{VRM\_CHIP\_VDD}}$ at high frequency by the larger pass transistor size. Because the sensitivity of C_{GS_PASS} is larger than that of $g_{m\mathrm{PASS}}$ under a given pass transistor size variation, $H_{\mathrm{VRM\_CHIP\_VDD}}$ becomes sensitive more to the pass transistor size as the frequency increases over 1 GHz.

C. Reference Voltage Noise Impact on the On-Chip Power Noise Induced by the On-Chip Linear VRM

The proposed model (18) indicates on-chip VRM output noise induced by reference voltage noise. In the same manner as the Z_{11} model derivation procedure, an analytical model of the voltage noise transfer function from the reference voltage node to the on-chip linear VRM output ($H_{\mathrm{VRM\_CHIP\_}VREF}$) is derived as (27) and (28). To consider peak-to-peak noise, the magnitude expression is increased by a factor of 2

$$|H_{\mathrm{VRM\_CHIP\_}VREF}(\omega)| = 2 \times \frac{\sqrt{(m_8\omega)^2 + {m_9}^2}}{\sqrt{(m_1\omega)^2 + (m_2 - \omega^2)^2}} \tag{27}$$

$$\angle H_{\mathrm{VRM\_CHIP\_}VREF}(\omega) = \pi + \mathrm{atan}\left(\frac{m_2 - \omega^2}{m_1\omega}\right) + \mathrm{atan}\left(\frac{m_9}{m_8\omega}\right). \tag{28}$$

Fig. 12 shows the simulated magnitude and phase of $H_{\mathrm{VRM\_CHIP\_}VREF}$ using (27) and (28). The precise expressions before and after the resonant frequency are indicated at the top as

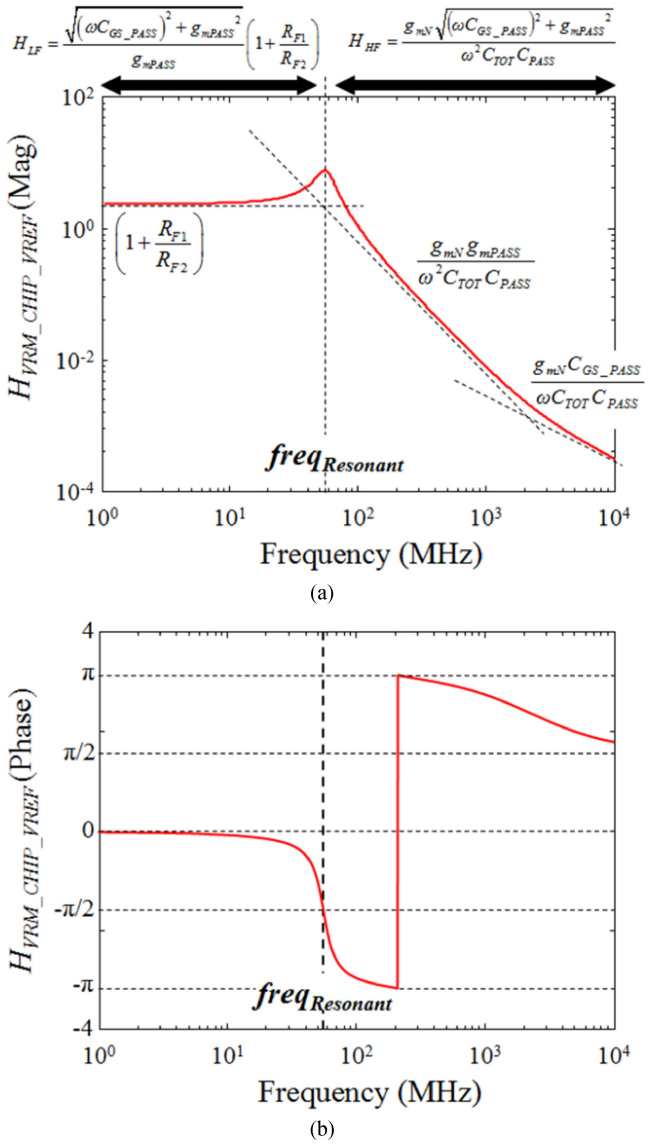

Fig. 12. Simulated voltage noise transfer function from the reference voltage node to the on-chip linear VRM output ($H_{\mathrm{VRM\_CHIP\_VREF}}$). (a) Magnitude. (b) Phase. The precise expressions before and after the resonant frequency (H_{LF} and H_{HF}) are indicated at the top. The simplified expressions that determine $H_{\mathrm{VRM\cdot CHIP\cdot VREF}}$ at each frequency region are indicated inside the graph.

H_{LF} and H_{HF}, respectively. In general, the amount of $g_{m\mathrm{PASS}}$ is much larger than $\omega C_{GS\_\mathrm{PASS}}$ at the frequency range below 1 GHz. The region in which this condition is valid can be divided into low-, mid-, and high-frequency regions. The simplified expressions that determine $H_{\mathrm{VRM\_CHIP\_}VREF}$ at each frequency region are shown in Fig. 12.

At the low-frequency region of several MHz, $H_{\mathrm{VRM\_CHIP\_}VREF}$ is constant. In this frequency range, $H_{\mathrm{VRM\_CHIP\_}VREF}$ is only determined by (R_{F1}/R_{F2}). Because the reference voltage fluctuation by low-frequency noise is almost equivalent to the dc level variation of V_{REF}, the expression at low frequency equals the ratio between V_{REF} and $V_{\mathrm{VRM\_CHIP}}$ in (1). It is noteworthy that the reference

voltage noise at low frequency induces a significant amount of VRM output noise. The (R_{F1}/R_{F2}) term is hard to adjust for a stable dc level of the VRM output. Even though this ratio is minimized, $H_{\mathrm{VRM\_CHIP\_}VREF}$ is always larger than 1, which means the low-frequency reference voltage noise transferred to the VRM output is always amplified.

At the mid-frequency range from several tens of MHz to several hundred MHz, impacts of parasitic capacitances rise. As the frequency goes up, the dominant impact of the parasitic capacitances and C_{VRM} make a resonant frequency. Because the denominator expression of (27) is the same to that of (19), the resonant frequency of $H_{\mathrm{VRM\_CHIP\_}VREF}$ equals that of Z_{11} at the VRM output. In the same manner as the off-chip power noise reduction, the VRM output noise induced by the reference voltage noise can be minimized when the spectrum of the reference voltage noise is given. The VRM output noise induced by the reference voltage noise is minimized by avoiding the resonant frequency of $H_{\mathrm{VRM\_CHIP\_}VREF}$ from the peak frequency of the reference voltage noise spectrum.

At the high-frequency range over several hundred MHz, noises mostly transfer through parasitic capacitances because of their low impedances. A reference voltage noise fluctuates a voltage at the pass transistor gate. $g_{m\mathrm{PASS}}$ mostly determines the transferred gate noise to the VRM output up to several hundred MHz, whereas the gate noise at high frequency over several GHz mostly transfers through C_{GS_PASS}. To reduce the VRM output noise induced by reference voltage noise, g_{mN} or C_{GS_PASS} need to be reduced. However, g_{mN} is usually hard to change because it relates to the error amplifier gain. C_{GS_PASS} reduction is also not effective because the smaller C_{GS_PASS} also decreases C_{PASS} at the same time. An effective way to reduce $H_{\mathrm{VRM\_CHIP\_}VREF}$ is to increase C_{VRM}. As the reference voltage noise frequency increases, the VRM output noise induced by the reference voltage noise becomes negligible because $H_{\mathrm{VRM\_CHIP\_}VREF}$ inverse-proportionally decreases.

The phase of $H_{\mathrm{VRM\_CHIP\_}VREF}$ is almost zero at the low-frequency range because m_9 is much larger than $m_8\omega$, which means that $g_{m\mathrm{PASS}}$ is much larger than $\omega C_{GS\_\mathrm{PASS}}$. Even though the frequency reaches the resonant frequency, the large $g_{m\mathrm{PASS}}$ and m_9 term still provide the phase of $\pi/2$. As the frequency goes up, the atan$((m_2-\omega^2)/m_1\omega)$ term changes from zero to $-\pi/2$. Alternately, the atan$(m_9/m_8\omega)$ term changes from $\pi/2$ to zero. As a result, the phase of $H_{\mathrm{VRM\_CHIP\_}VREF}$ converges to $\pi/2$ at high frequency behind several GHz.

To validate the proposed analytical model based on SPICE simulation, the peak-to-peak amounts of the VRM output noise are simulated with different reference voltage noise frequencies. An aggressor buffer at load operates with a 400-MHz clock input signal to generate high-speed load current. The VRM output noise induced by the reference voltage noise is estimated by subtracting the VRM output noise only induced by the load current from the total VRM output noise. Fig. 13 shows the estimated VRM output noise induced by the reference voltage noise using the SPICE model and (27). Even though the VRM design and amount of reference voltage noise are changed, the proposed analytical model shows good correlation with the SPICE simulation result. The proposed model accurately estimates the VRM output noise induced by the reference voltage noise as long as the amount of reference voltage noise is sufficiently small to guarantee pass transistor operation in saturation mode.

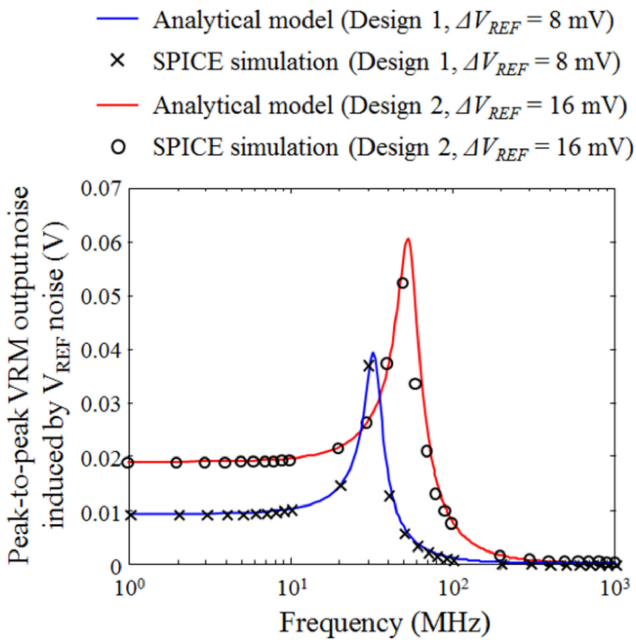

Fig. 13. Simulated peak-to-peak VRM output noise induced by V_{REF} noise. To verify the analytical model, the noises are estimated by using the SPICE model and the proposed model. Two different VRM designs and different amounts of reference voltage noises (ΔV_{REF}) are employed for verification.

Fig. 14(a) and (b) shows the simulated $H_{\mathrm{VRM\_CHIP\_}VREF}$ based on the proposed model with different C_{VRM} and pass transistor sizes, respectively. In the case of C_{VRM} variation, the trend is the same as in the off-chip power noise case. As shown in Fig. 12, $H_{\mathrm{VRM\_CHIP\_VREF}}$ at low frequency is independent of C_{VRM} and only dependent on the feedback resistors. Thus, $H_{\mathrm{VRM\_CHIP\_}VREF}$ at region [A-3] is constant regardless of the C_{VRM} variation. Because the resonant frequency at region [B-3] is inversely proportional to C_{TOT}, as indicated in (22), the increased C_{VRM} reduces the resonant frequency. At the high-frequency region [C-3], $H_{\mathrm{VRM\_CHIP\_}VREF}$ inverse proportionally decreases as C_{VRM} increases.

In the case of pass transistor size variation, $H_{\mathrm{VRM\_CHIP\_}VREF}$ at region [A-4] is constant regardless of the pass transistor size because it is only determined by feedback resistors. Because the resonant frequency of $H_{\mathrm{VRM\_CHIP\_}VREF}$ at region [B-4] equals that of Z_{11} at the VRM output, the trend of the resonant frequency with pass transistor size variation is the same as that of the off-chip power noise case. While C_{TOT} is almost independent of the pass transistor size, the larger pass transistor size slightly increases L_{PASS}, resulting in the reduced resonant frequency. $H_{\mathrm{VRM\_CHIP\_}VREF}$ at the high-frequency region [C-4] decreases as the pass transistor size increases. This trend is opposite to that of the off-chip power noise case. While C_{PASS} is proportional to the pass transistor size, the change

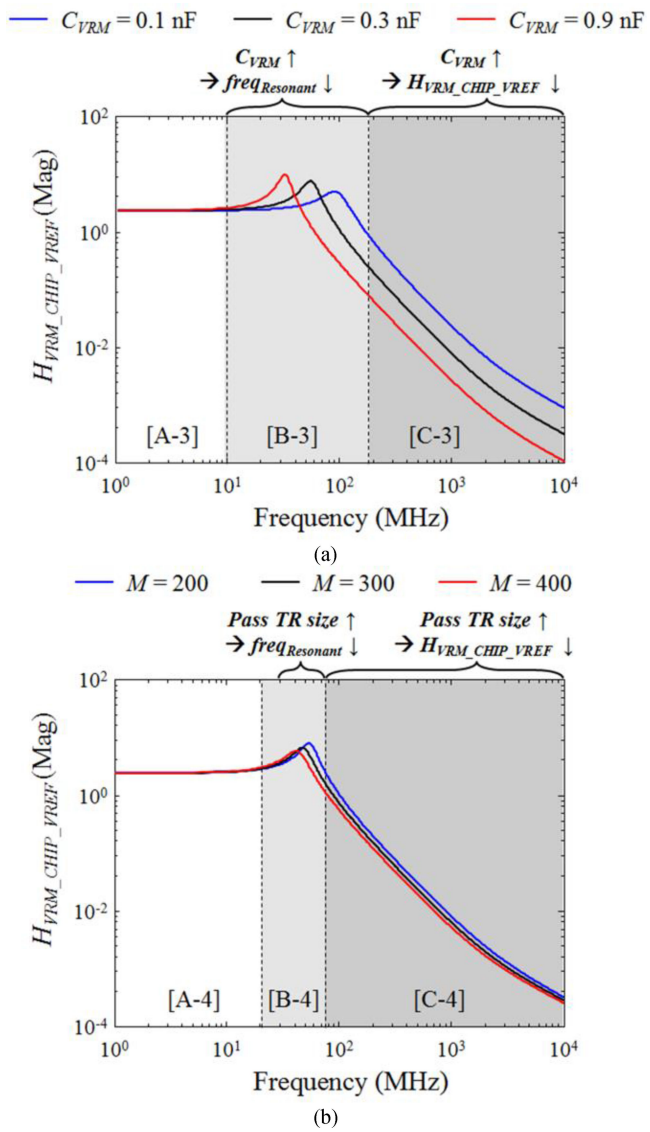

Fig. 14. Simulated $H_{\mathrm{VRM\_CHIP\_VREF}}$ with different VRM design parameters. On-chip decoupling capacitance at (a) load (C_{VRM}) variations and (b) pass transistor size variations. *M* is the multiplication factor that determines the pass transistor size.

ratio of $g_{m\mathrm{PASS}}$ by pass transistor size variation is smaller than that of C_{PASS}. Thus, $H_{\mathrm{VRM\_CHIP\_}VREF}$ decreases as the pass transistor size increases. Because the impact of C_{GS_PASS} becomes dominant rather than $g_{m\mathrm{PASS}}$ as the frequency goes up, $H_{\mathrm{VRM\_CHIP\_}VREF}$ becomes independent of the pass transistor sizes as the frequency increases over several GHz.

Fig. 15 shows the comparison result between $H_{\mathrm{VRM\_CHIP\_VDD}}$ and $H_{\mathrm{VRM\_CHIP\_}VREF}$. While $H_{\mathrm{VRM\_CHIP\_}VREF}$ only depends upon feedback resistors at the frequency region [A], $H_{\mathrm{VRM\_CHIP\_VDD}}$ is also affected by $(\lambda_N + \lambda_P)/g_{mN}$. Because $(\lambda_N + \lambda_P)$ is generally much lower than g_{mN}, the magnitude of $H_{\mathrm{VRM\_CHIP\_VDD}}$ is smaller than $H_{\mathrm{VRM\_CHIP\_}VREF}$ at the low-frequency region [A]. Therefore, the reference voltage node needs to be carefully designed rather than the off-chip PDN to reduce the VRM output noise at

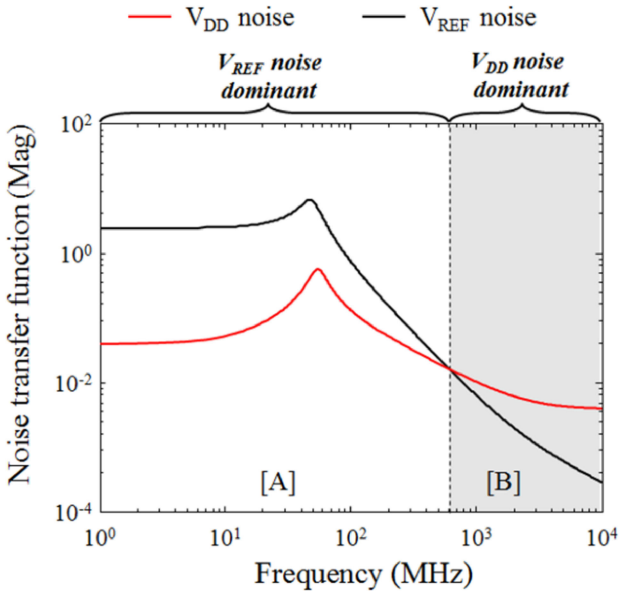

Fig. 15. Comparison result between $H_{\mathrm{VRM\_CHIP\_VDD}}$ and $H_{\mathrm{VRM\_CHIP\_VREF}}$. The reference voltage (V_{REF}) noise has dominant impact at the low-frequency region [A], whereas the off-chip power (V_{DD}) noise becomes dominant at the high-frequency region [B].

low frequency. Alternately, the magnitude of $H_{\mathrm{VRM\_CHIP\_VDD}}$ becomes larger than that of $H_{\mathrm{VRM\_CHIP\_}VREF}$ at the high-frequency region [B]. $H_{\mathrm{VRM\_CHIP\_}VREF}$ decreases as the frequency increases at the high-frequency region [B], whereas $H_{\mathrm{VRM\_CHIP\_VDD}}$ approaches a specific value determined by the parasitic capacitance of the pass transistor and C_{VRM}. However, the magnitude of $H_{\mathrm{VRM\_CHIP\_VDD}}$ itself is quite small at the high-frequency range because C_{VRM} is usually much larger than the parasitic capacitances of the pass transistor. If the amount of C_{VRM} is not sufficient, the off-chip PDN needs to be carefully designed, rather than the reference voltage node, to reduce the VRM output noise at high frequency. Another noticeable point is that the resonant frequencies of Z_{11} at the VRM output, $H_{\mathrm{VRM\_CHIP\_VDD}}$, and $H_{\mathrm{VRM\_CHIP\_}VREF}$ are almost identical. If the designer adjusts this common resonant frequency to avoid the peak frequencies of the load current, off-chip power noise, and reference voltage noise spectrums, we can minimize not only the internal on-chip VRM output noise induced by load current but also the VRM output noises induced by external noises at the same time.

V. Conclusion

In this paper, analytical models of the on-chip power noise induced by an on-chip linear VRM with a high-speed output buffer were proposed. When the high-speed output buffer operates at load, the pass transistor of the on-chip linear VRM mostly operates in saturation mode. Under this condition, closed-form equations for the on-chip power noises induced by a typical on-chip LDO regulator were derived based on the PWL approximated MOSFET *I–V* curve model. The simulated on-chip VRM

output noise waveforms using the proposed analytical models show very good correlation with the SPICE simulation results.

Based on the proposed analytical models, on-chip power noise induced by the on-chip linear VRM was analyzed in the frequency domain. The self-impedance at the VRM output, noise transfer function of the off-chip PDN to the VRM output, and noise transfer function of the reference voltage to the VRM output share a common resonant frequency. If the spectrums of the load current from a high-speed output buffer, off-chip power voltage noise, and reference voltage noise are given, the on-chip VRM output noise can be minimized by avoiding the common resonant frequency from the peak frequencies of the given spectrums. An efficient way to control the resonant frequency is to adjust the on-chip decoupling capacitance at load.

The on-chip VRM output noises induced by off-chip power noise and reference voltage noise at low frequency below the resonant frequency were almost independent of the on-chip decoupling capacitance at load and the pass transistor size. As the on-chip decoupling capacitance at load decreased, the on-chip linear VRM output noises induced by the load current, off-chip power noise, and reference voltage noise were all reduced at the frequency range over the resonant frequency. As the pass transistor size increased, the VRM output noise induced by the reference voltage noise at the frequency range over the resonant frequency decreased, whereas that induced by off-chip power noise increased. At the low-frequency range below several GHz, the reference voltage dominantly induces the on-chip VRM output noise rather than the off-chip power noise. Alternately, the off-chip power noise dominantly generates the on-chip VRM output noise rather than the reference voltage noise at the high-frequency range over several GHz. Because the magnitude of the VRM output noise itself at high frequency is small in general, the reference voltage node needs to be carefully designed. The analysis results based on the proposed analytical models provide not only an in-depth physical understanding but also useful design guidance to minimize the on-chip power noise induced by an on-chip linear VRM with a high-speed output buffer.

APPENDIX

Equations of the Coefficients (m1−m9) for the Proposed Analytical Model

$$m_1 = \frac{\left(1-\frac{C_{GS\_\mathrm{PASS}}}{C_{\mathrm{PASS}}}\right) g_{m\mathrm{PASS}} + \lambda_{\mathrm{PASS}} + \frac{1}{R_{F1}+R_{F2}}\left(1+\frac{C_{GS\_\mathrm{PASS}} R_{F1} g_{mN}}{C_{\mathrm{PASS}}}\right)}{C_{\mathrm{VRM}} + C_{GS\_\mathrm{PASS}} + C_{SB\_\mathrm{PASS}}} + \frac{\lambda_N + \lambda_P}{C_{\mathrm{PASS}}} \tag{A1}$$

$$m_2 = \frac{g_{mN} g_{m\mathrm{PASS}}}{(C_{\mathrm{VRM}} + C_{GS\_\mathrm{PASS}} + C_{SB\_\mathrm{PASS}}) \times C_{\mathrm{PASS}}} \frac{R_{F1}}{R_{F1}+R_{F2}} \tag{A2}$$

$$m_3 = -\frac{1}{(C_{\mathrm{VRM}} + C_{GS\_\mathrm{PASS}} + C_{SB\_\mathrm{PASS}})} \tag{A3}$$

$$m_4 = -\frac{\lambda_N + \lambda_P}{(C_{\mathrm{VRM}} + C_{GS\_\mathrm{PASS}} + C_{SB\_\mathrm{PASS}}) \times C_{\mathrm{PASS}}} \tag{A4}$$

$$m_5 = \frac{C_{\mathrm{PASS}}}{(C_{\mathrm{VRM}} + C_{GS\_\mathrm{PASS}} + C_{SB\_\mathrm{PASS}}) \times C_{GS\_\mathrm{PASS}} C_{GD\_\mathrm{PASS}}} \tag{A5}$$

$$m_6 = \frac{\frac{C_{GD\_\mathrm{PASS}}}{C_{\mathrm{PASS}}} g_{m\mathrm{PASS}} + \lambda_{\mathrm{PASS}}}{(C_{\mathrm{VRM}} + C_{GS\_\mathrm{PASS}} + C_{SB\_\mathrm{PASS}})} \tag{A6}$$

$$m_7 = \frac{(g_{m\mathrm{PASS}} + \lambda_{\mathrm{PASS}}) \times (\lambda_N + \lambda_P)}{(C_{\mathrm{VRM}} + C_{GS\_\mathrm{PASS}} + C_{SB\_\mathrm{PASS}}) \times C_{\mathrm{PASS}}} \tag{A7}$$

$$m_8 = \frac{C_{GS\_\mathrm{PASS}} g_{mN}}{(C_{\mathrm{VRM}} + C_{GS\_\mathrm{PASS}} + C_{SB\_\mathrm{PASS}}) \times C_{\mathrm{PASS}}} \tag{A8}$$

$$m_9 = \frac{g_{m\mathrm{PASS}} g_{mN}}{(C_{\mathrm{VRM}} + C_{GS\_\mathrm{PASS}} + C_{SB\_\mathrm{PASS}}) \times C_{\mathrm{PASS}}}. \tag{A9}$$

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