

Modeling Strategy for EMI Filters

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Abstract—Performance of electromagnetic interference (EMI) filters in power-electronics applications is limited by the parasitic coupling between the components of the filters and the self-parasitic of each component. While these parasitic effects can be partially taken into account on the circuit level, it is difficult to estimate their values. In this article, a full-wave modeling methodology is proposed to predict the performance of a complete EMI filter up to 1 GHz. Following the proposed methodology, the mutual couplings among the EMI filter components are taken into account as well as the self-parasitics of each individual component. Experiments and simulations are carried out to validate the modeling methodology. A self-parasitic cancellation technique is also applied to demonstrate the benefits of three-dimensional modeling methodology in EMI filter design.

Index Terms—Common-mode choke (CMC), EMI filter, film capacitor, full-wave modeling, mutual coupling.

I. INTRODUCTION

EMI FILTERS are commonly used to address conducted emission issues. With the process of miniaturization, modularization, and integration in power electronic systems, the electromagnetic interference (EMI) filters are required to have smaller volume and better performance [1]. At the design stage of an EMI filter, however, parasitic behavior and mutual coupling among the components are hard to predict accurately. These effects are responsible for degradation of the filter performance, as reported in [2]. Different methodologies have been proposed to estimate parasitics and coupling. A circuit model has been proposed in [3], which contains both self and mutual parasitics of an EMI filter (capacitor-to-capacitor and capacitor-to-common-mode chokes (CMCs) mutual inductances). But the values of these mutual inductances are determined using measurements, which require to have filter prototypes. A 3-D model in [4] uses a

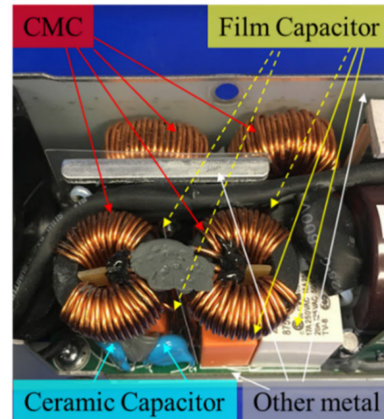


Fig. 1. Example of a compact EMI filter design.

simple structure to represent two coupled current paths. The mutual inductance obtained from the 3-D model is back-annotated into a circuit model to predict the filter performance. Transverse electromagnetic (TEM) cell measurements for individual components are implemented in [5] to obtain the mutual inductance between every two components.

However, as the filter geometry gets more and more complicated, the reliability of these methods becomes questionable. As shown in Fig. 1, a compact EMI filter design can include not only the individual electrical components such as capacitors and CMCs, but also wires, printed circuit board (PCB) board, chassis, and other metallic parts for mechanical purposes. Therefore, identifying all coupling mechanisms in such structures can become difficult as inductive and capacitive coupling exists not only between the electrical components but also between them and external elements, such as chassis and wires. Besides this, previous studies have been concentrating mainly on modeling and predicting the inductive mutual coupling, while few investigations were done upon the capacitive couplings.

On the other hand, during the iterative stage of EMI filter design, the methods mentioned previously require remeasurement and recalculating each mutual parasitics even if only the geometry of the filter has changed.

Several different techniques have been proposed to reduce the self or mutual parasitics [1], [2], [6], [7]. These techniques can help to improve filter performance. However, they all introduce other parasitics. The study in [6] has shown that the combination of different parasitic-cancellation techniques may lead to degraded filter performance.

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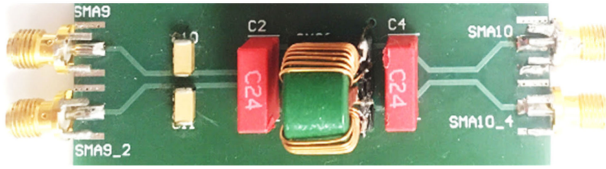


Fig. 2. EMI filter under investigation.

The 3-D modeling of the whole EMI filter can, therefore, provide a solution for both predicting the filter performance and validating different parasitic-cancellation techniques. The 3-D model of an EMI filter can help at both initial and iterative design stages.

Using 3-D models for EMI filter is not new. For example in [8]–[10], the authors modeled the parasitics and mutual coupling in EMI filters using 3D-PEEC-BIM method. Results obtained by the 3D-PEEC-BIM method were presented for frequency range up to 30 MHz. Moonen *et al.* [11], Asmanis *et al.* [12], and Asmanis *et al.* [13] reported the modeling procedure for individual components such as multilayer ceramic capacitors (MLCC) and CMCs. However, 3-D modeling of complete EMI filters up to 1 GHz based on a more common and readily commercially available method such as finite element method (FEM) has not been reported in the literature. Full-wave simulations up to 1 GHz reveal not only the performance of the EMI filter in suppressing conducted EMI but potentially can also predict the role of the EMI filter in radiated EMI tests, increasing the value of the model for EMC-aware design.

In [14], a 3-D modeling strategy for film capacitors has been proposed and validated. The mentioned modeling strategy uses a simple structure to avoid explicit modeling of the film roll inside the film capacitor. In this way, the model is easy to build and is computationally efficient. The FEM-based solver is able to perform full-wave simulation for the film capacitors with good accuracy up to 1 GHz in a relatively short time (up to tens of minutes maximum).

In this article, a full-wave modeling strategy for an entire EMI filter (including capacitors and CMCs) is proposed and validated. The filter performance is correctly predicted by the 3-D full-wave model up to 1 GHz including common and differential mode responses. Besides this, a parasitic-cancellation technique is implemented in 3-D modeling to demonstrate the benefit brought by the model at the iterative stage of the filter design.

The rest of this article is organized as follows. In Section II, a typical EMI filter is presented. The components are anatomized to provide information for constructing a 3-D model. In Section III, the modeling procedure for each component is described. In Section IV, an example is shown to display the advantages of using 3-D model to help improve the EMI filter design. Finally, Section V concludes this article.

II. EMI FILTER AND COMPONENTS

A one-stage EMI filter is analyzed in this work. The layout of the EMI filter is demonstrated in Fig. 2. This filter uses two film-capacitors as X-capacitors and two ceramic capacitors as Y-capacitors.

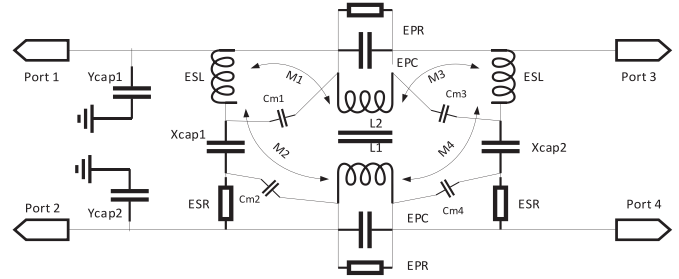


Fig. 3. Equivalent model of the EMI filter under investigation.

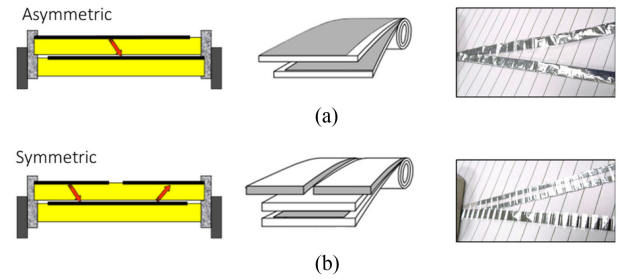


Fig. 4. (a) Asymmetric winding and (b) symmetric winding of film capacitors. The film of capacitor from each type is unwound to show the difference.

The Y-capacitors are relatively far away from the other components, thus, the mutual coupling between other components and the Y-capacitors is of less relevance. As for the X-capacitors, they are inductively and capacitively coupled to the CMC. Taking this into account, a circuit diagram for the filter containing self and mutual parasitics can be drawn (see Fig. 3).

In the proposed methodology, the self-parasitics of the components are captured by 3-D modeling their geometry (in some cases measurements are needed to determine model parameters, such as the permeability of the CMC core). The mutual parasitics are modeled in a 3-D model exclusively, without relying on measurements. The following subsections demonstrate how 3-D models of every EMI filter component can be created.

A. Internal Structure of Film Capacitors

In most cases film capacitors are made of two pieces of plastic film covered with metallic electrodes rolled into a cylindrically shaped winding. The capacitor is finalized by attaching terminals and encapsulation [15]. The electrodes are interchangeable because the film capacitors are not polarized. However, as demonstrated in [14], the film capacitor is not necessarily electrically symmetric. The capacitive coupling between the film capacitor and another film capacitor may be dependent on the film capacitor's orientation. Two winding technologies—symmetric and asymmetric—have been investigated in [14]. These two technologies are shown in Fig. 4. The symmetric winding in film capacitors effectively forms multiple smaller capacitors connected in series. In this way, the effective breakdown voltage of the film capacitor is raised.

Correspondingly, two modeling structures were proposed in [14] for electrically symmetrical and asymmetrical film capacitors (see Fig. 5). It is essential to determine, which type of

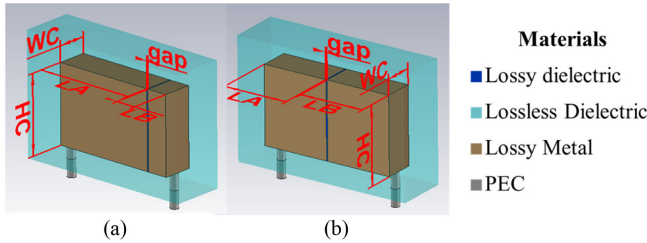


Fig. 5. Three-dimensional model for film capacitors. (a) Asymmetric winding. (b) Symmetric winding.

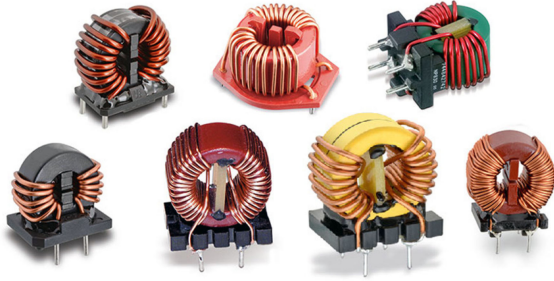


Fig. 6. Group of CMC used in EMI filter applications.

winding technology is applied in the film capacitors especially when they are mounted close to other components to capture the capacitive coupling effects correctly and what is the actual orientation of the capacitor mounted on the PCB. The winding type and orientation can be determined by dissecting the capacitor or nondestructively by measuring the electric potential on the capacitor surface as described in [14].

The models in Fig. 5 represent capacitors as solid metal blocks and its nominal capacitance is modeled by inserting a dielectric material between the metal blocks. The permittivity of the dielectric layer is calculated using a parallel plate capacitor formula [14].

B. Internal Structure of the Toroidal CMCs

A group of toroidal CMCs commonly used in EMI filters is shown in Fig. 6. These CMCs, although they share the same shape of core, could have different properties. Three types of core material are used: Nanocrystalline, Mn-Zn ferrite, and Ni-Zn ferrite. The Nanocrystalline core is highly conductive and usually is placed inside a plastic shell with relatively large gaps (up to several mm) between the core and the shell. Thus, the capacitive coupling to the core is small or even negligible. Other than a difference in the core material, the CMCs can differ in the number of the winding layers. Besides this, they can be mounted on a PCB in either standing or flat fashion. The modeling procedure proposed in this article can cover all these variations.

The windings of the CMCs will exhibit a transmission line effect at high frequencies [16], similar to the transmission line effect found in film capacitors [17]. A 3-D model following the strategy proposed in this article can reproduce the transmission line effect since the model for CMC is very close to the actual structure, with little geometrical features discarded.

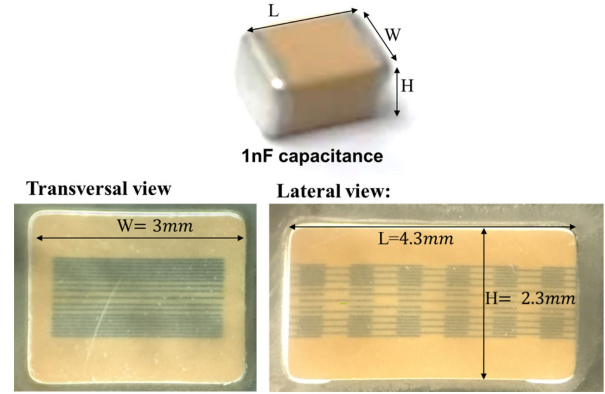


Fig. 7. Cross section of a 1 nF MLCC. Multiple smaller capacitors are found inside the MLCC, connected in series. The length L , width W , and height H are measured.

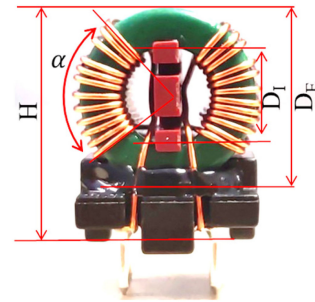


Fig. 8. Dimensions of a CMC.

C. Internal Structure of Ceramic Capacitors

Ceramic capacitors usually have small package size. However, their parasitic inductance and inductive coupling with other components could be still relevant. Mutual capacitances contributed by the ceramic capacitors—although small—can still be measured. To create a 3-D model a MLCC was cut open. The cross section shows that the capacitor can have a complicated internal structure (see Fig. 7). Other than laminated electrodes, the capacitor can consist of several smaller capacitors, connected in series to increase the voltage rating of the capacitor.

III. EMI FILTER MODELING PROCEDURE

The primary goal of the modeling strategy is to predict the filter performance accurately. Saving computational resources comes secondly. In this section, the modeling procedure is broken down into the modeling of each component. The component models are validated separately before being inserted into the filter model. He *et al.* [14] described the film capacitor modeling in detail. As for the modeling of CMCs, characterization through simple measurements is required before the modeling procedure starts.

A. Characterization of CMC

CMC WE7448252311 [18] is used in the EMI filter shown in Fig. 2. The dimensions of this CMC are measured and displayed in Fig. 8 and Table I.

TABLE I
DIMENSION OF THE CMC

H	20.0 mm	Wire radius (a)	0.3 mm
α	107°	Core Width(W_E)	9.3 mm
D_I	14.2 mm	Number of turns (N)	12
D_E	18.6 mm	Single/Multi-layer winding	Single Layer

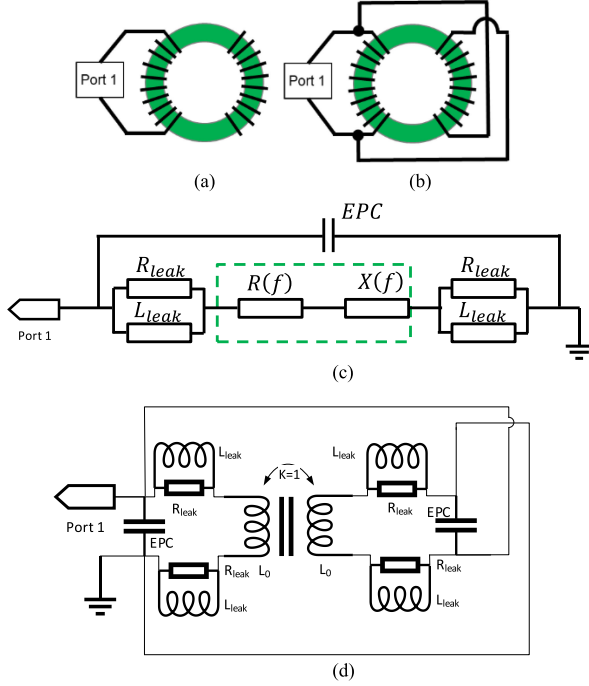


Fig. 9. (a) Single-winding CMC configuration. (b) Cross-winding CMC configuration. (c) Equivalent circuit for single-winding configuration. (d) Equivalent circuit for cross-winding configuration.

Other than physical dimensions, the electrical properties are also measured under two configurations: single-winding configuration and cross-winding configuration [19]. The measurement circuits and the equivalent circuits of the choke in two configurations are presented in Fig. 9.

The equivalent circuit shown in Fig. 9(c) is used in [20] to extract the permeability of the core material. Equivalent parallel capacitance (EPC) denotes the equivalent parallel capacitance of the winding on CMC. The green box in Fig. 9(c) represents the actual inductance and magnetization loss contributed by the flux inside the core material with a total impedance equal to

$$Z_{core} = jX(f) + R(f). \quad (1)$$

The impedance $Z_{leak} = \frac{j\omega L_{leak} R_{leak}}{j\omega L_{leak} + R_{leak}}$ represent the leakage inductance and its loss.

The real and imaginary part of the core material permeability can be related to the core geometry [20]

$$\begin{aligned} \mu' &= \frac{2\pi X(f)}{\omega N^2 \mu_0 W_E \ln\left(\frac{D_E}{D_I}\right)} \\ \mu'' &= \frac{2\pi R(f)}{\omega N^2 \mu_0 W_E \ln\left(\frac{D_E}{D_I}\right)} \end{aligned} \quad (2)$$

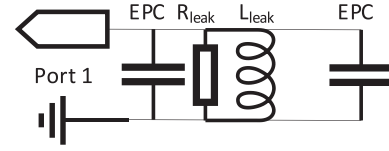


Fig. 10. Simplified circuit for cross-winding configuration.

where W_E , D_E , and D_I are the width, outer diameter, and inner diameter of the core, respectively, N is the number of turns in the winding.

The measured impedance following the single-winding configuration is denoted as Z_{meas} . According to the equivalent circuit diagram in Fig. 9(c), the relationship between measured impedance and Z_{core} is

$$Z_{meas} = \frac{Z_c \cdot (Z_{core} + 2Z_{leak})}{Z_c + (Z_{core} + 2Z_{leak})} \quad (3)$$

where

$$Z_c = \frac{1}{j\omega \cdot EPC}. \quad (4)$$

Thus, the leakage impedance Z_{leak} needs to be determined before obtaining Z_{core} . As suggested in [19], the cross-winding configuration needs to be measured to obtain Z_c and Z_{leak} . The configuration and the corresponding equivalent circuit diagram is shown in Fig. 9(b). The circuit in Fig. 1(d) can be simplified into the circuit in Fig. 10, as the cross-winding configuration let the perfectly coupled portion of the inductances to cancel each other.

According to the circuit, the Z_{leak} can be obtained from the measurement result under cross-winding configuration. The procedure is straightforward since the measured impedance shows a clear resistor-inductor-capacitor (RLC) parallel resonance pattern.

The measured impedances from both configurations are shown in Fig. 11. Both the magnitude and phase are displayed. Substituting the parameters obtained from the cross-winding measurement into (2), along with the dimensions from Table I, the real and imaginary parts of the core permeability μ' , μ'' are extracted and plotted in Fig. 12.

B. Modeling of CMC

With the dimensions listed in Table I, a 3-D model of the CMC can be constructed. A macro program is developed to generate the model in CST STUDIO SUITE, in frequency domain solver environment. (Fig. 13).

In the entry of the macro, there are two options for the wire, either a thin wire model or a solid wire model. To reduce the mesh count required to represent solid wires, the wires are built to have square cross section instead of round cross section. The difference in wire settings leads to a difference in the parasitic capacitance.

In order to save computation resources, wires in the 3-D model have no insulation coating. Besides this, the wires in the model are not wound as tight as in the real CMC (due to difficulty of calculating the wire geometry needed to achieve tight winding).

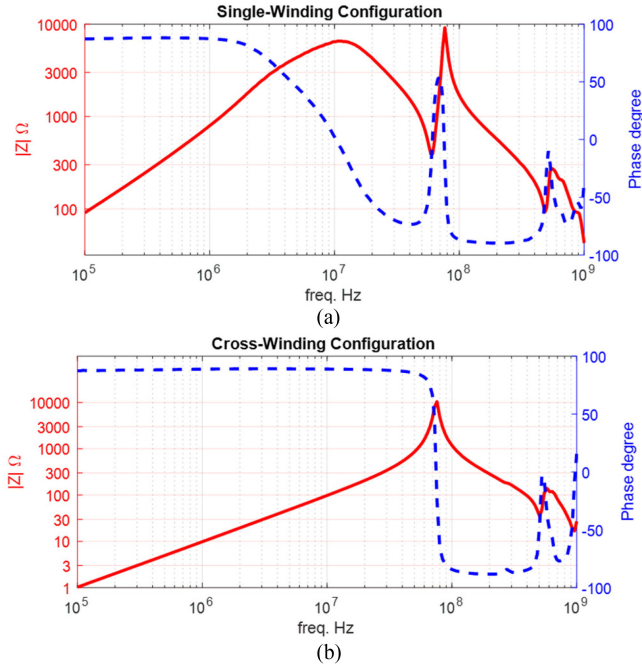


Fig. 11. (a) Single-winding configuration impedance magnitude and phase. (b) Cross-winding configuration impedance magnitude and phase.

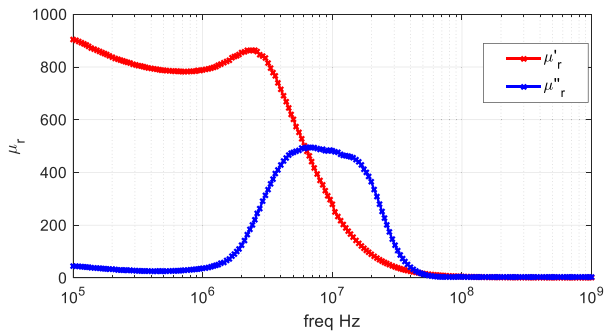


Fig. 12. Extracted permeability of the Ni-Zn core.

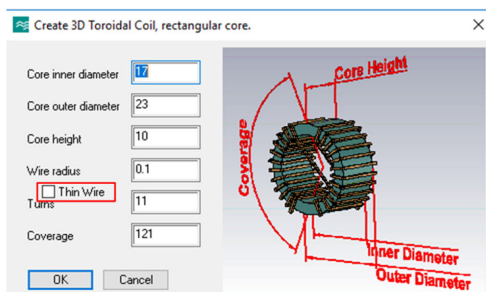


Fig. 13. User interface of the macro program.

As a result of this, the distance between wires is larger than that in reality, which can be as low as tens of micrometers, and the permittivity of the dielectric between the wires is lower. These differences lead to a mismatch in the parallel capacitance of the winding. To compensate for this difference, an additional insulation layer is added into the inner opening of the torus covering all turns. The permittivity of this insulation layer is

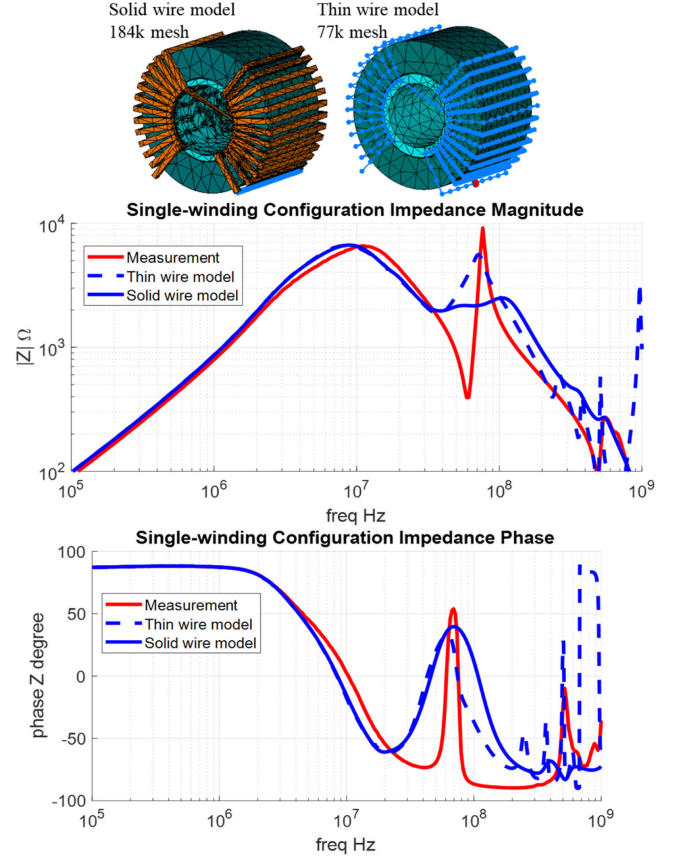


Fig. 14. CMC model and its impedance seen at single-winding configuration comparing against measurement results.

tuned to match the target parasitic capacitance. As mentioned in the previous section, the cross-winding configuration results show a clear *LC* resonance, which makes it an ideal target for parameter tuning. The tuning procedure is simple, since the EPC is dominated by the wire-to-wire capacitance in the winding, which is linearly proportional to the permittivity of the additional insulation layer.

Two versions of the CMC model (solid and thin wire) are displayed in Figs. 14 and 15, followed by their impedances under single-winding and cross-winding configurations, in comparison with the impedances obtained through measurement.

Both models demonstrate relatively good agreement with the measured parameters. However, since the mesh count of the thin wire model is significantly lower, this model will be used henceforth as more computationally efficient.

C. Modeling for the Ceramic Capacitor

An extreme case where two identical MLCCs are closely placed (0.3 mm apart) has been tested to validate the MLCC model. The cross section of the capacitor is shown in Fig. 7. One side of these two capacitors are connected to port 1 and port 2, respectively. The other side of the capacitors are connected to the ground plane by a 0.01 Ω lumped resistance. In the corresponding measurement setup one end of the capacitors is mounted on the microstrip trace (having the gap in the middle) and the other end is connected to the ground plane by vias. The coupling

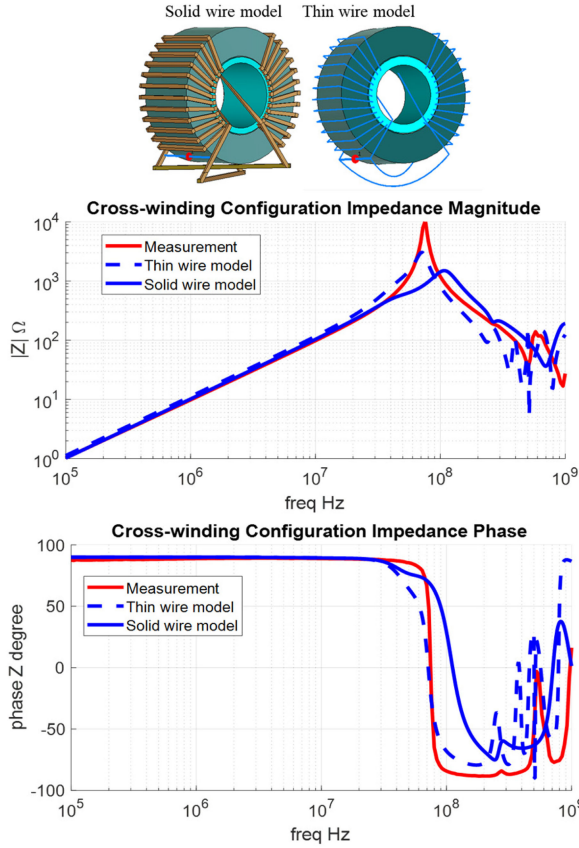


Fig. 15. CMC model and its impedance seen at cross-winding configuration comparing against measurement results.

between these two capacitors are evaluated by measuring and simulating the transmission coefficient S_{21} between the ports. Two models of the capacitors were created: the explicit model reproducing the internal structure of the capacitors and the simplified model, modeling the capacitors as solid blocks (similar to the film capacitors in Fig. 5). The results from both explicit model and simplified model are compared against measurement results (see Fig. 16).

The mechanism of the coupling between the two MLCCs is capacitive at lower frequencies, inductive at higher frequencies (above the resonance). The inductive coupling between the capacitors would be almost identical for both models because the current path geometry is practically the same in both cases. Capacitive coupling potentially could be different (due to a difference in electric field potential between the models), but for the configuration in Fig. 16 it happens to be very similar.

As can be seen from Fig. 16, building an explicit model for the ceramic capacitor does not improve the accuracy when compared with a simplified model. The relevance of coupling would be even less significant for the filter in Fig. 2 due to the increased distance between the capacitors relative to Fig. 16. At the same time the self-impedance of the capacitors is modeled accurately [see Fig. 16(c)].

In the simplified model for MLCC, a thin dielectric layer is inserted between the two solid blocks. The permittivity ε_r of this

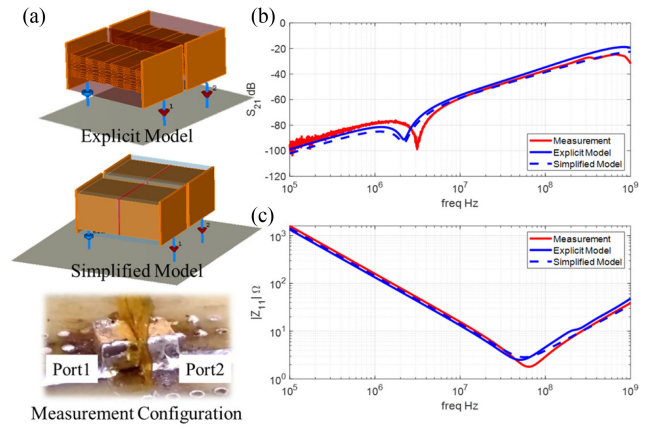


Fig. 16. (a) Three-dimensional models for MLCC capacitors and the measurement configuration for the coupling between the two capacitors. (b) S_{21} results obtained from explicit model, simplified model and measurement. (c) Impedance of a single MLCC from explicit model, simplified model, and measurement.

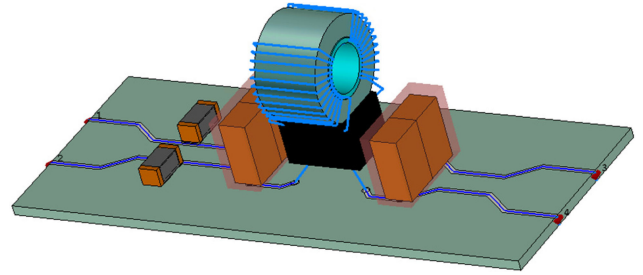


Fig. 17. Three-dimensional model for the EMI filter.

thin layer is obtained from parallel plate capacitance formula

$$\varepsilon_r = \frac{C}{S}d \quad (5)$$

where C is the nominal value of the MLCC; S is the cross-sectional area of the two solid blocks; d is the thickness of the thin dielectric layer.

D. Modeling for the Filter

The filter model integrates the models of the individual components. Other items such as the board, the traces, etc., are also included. Fig. 17 illustrates the final filter model. The CMC is mounted upright on the PCB, the X-capacitors have symmetric winding, and the Y-capacitors are MLCCs modeled as two solid blocks separated by a dielectric layer.

The performance of this filter model is displayed in Fig. 18 together with the measured curves. Coefficients S_{cc21} and S_{dd21} are the mix-mode scattering transmission coefficients for common and differential modes, respectively. Filter performance is predicted very accurately up to 10 MHz. Above 10 MHz, the accuracy of the differential mode suffers, probably due to inaccurate modeling of leakage inductance of the CMC (a similar effect of the leakage inductance is observed in a circuit model in Fig. 3). Relatively large discrepancies are observed above 100 MHz but even in that frequency range, the tendency is captured correctly. At the same time, frequencies where the filter

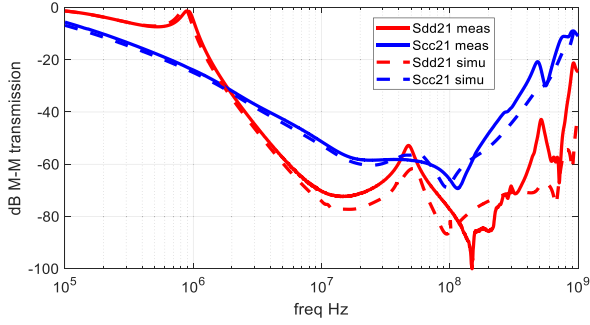


Fig. 18. Performance of the EMI filter. Results are compared between 3-D simulation and measurement.

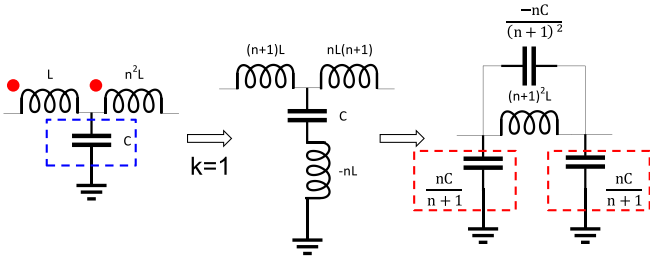


Fig. 19. EPC cancellation technique using a tapping capacitor.

performance changes qualitatively (50 MHz and 100 MHz for the differential mode and 100 MHz for the common mode) are predicted relatively accurately. Because of this, the model can be useful for filter optimization despite quantitative inaccuracies.

IV. PRACTICAL APPLICATION OF THE 3-D MODEL

In this section, an example of applying parasitic cancellation technique to the filter design is discussed. The purpose of this discussion is to give an example of the scenarios, where the 3-D modeling strategy for EMI filters can be used.

The goal of the filter mentioned in Section III is to suppress both differential mode (DM) noise and common mode (CM) noise, especially for the frequency range of 10 MHz–100 MHz. Since the EPC of the CMC dictates the performance of S_{cc21} in this range, an EPC cancellation technique (see Fig. 19) proposed in [21] is, therefore, implemented and evaluated through the 3-D modeling.

This approach adds a tapping capacitor (marked in blue box) to the windings on the CMC. This tapping capacitor—when set at the right value—will cancel the EPC of the winding. The performance of the filter is maximized when the following criterion is met:

$$\frac{nC}{(n+1)^2} = \text{EPC}. \quad (6)$$

However, the EPC of the winding often varies from unit to unit. Besides this, the cancellation technique itself introduces additional capacitances (marked in red dashed boxes in Fig. 19), and the tapping capacitors themselves will be parasitically coupled to the CMC. Because of this, the circuit in Fig. 19 is a relatively rough approximation of the actual situation. The 3-D model provides a solution to find the best tapping capacitor value

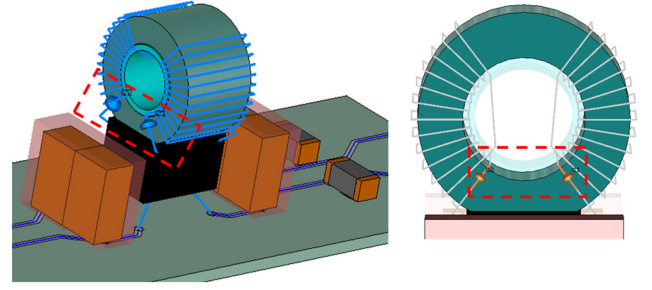


Fig. 20. Three-dimensional model of the filter after applying the EPC cancellation technique.

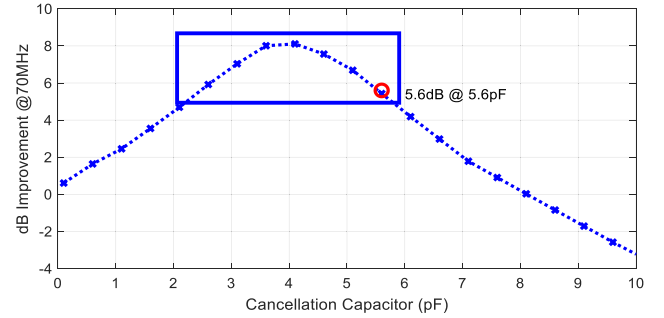


Fig. 21. Improvement of S_{cc21} at 70 MHz as a function of tapping capacitance.

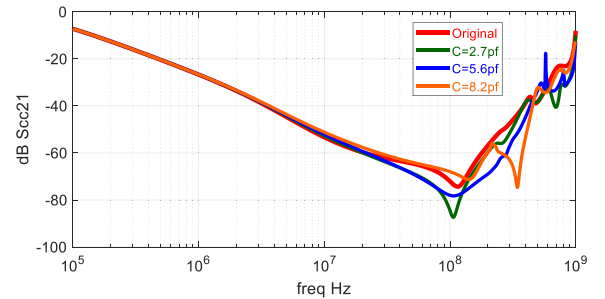


Fig. 22. Simulated performance of the filter (S_{cc21}) with different tapping capacitor values.

and evaluates the influence introduced by the added parasitics. A group of simulation results can quickly be obtained from a 3-D simulation with different values of tapping capacitance. Fig. 20 shows the 3-D model, where the tapping capacitor (modeled as a lumped element) is added between the first turn of the windings and the ground plane.

The effect of the tapping capacitor can be observed in the frequency range from 10 to 100 MHz. We selected a frequency of 70 MHz as a reference point to compare the effect of different capacitor values on the magnitude of S_{cc21} . A parameter sweep is then implemented in 3-D solver, sweeping the tapping capacitance value from 0.1 pF to 10 pF at a step of 0.5 pF. The improvement in S_{cc21} at 70 MHz is then plotted against the tapping capacitance in Fig. 21, while the S_{cc21} at certain capacitance values are plotted in Fig. 22.

At the same time, simulation results also show that adding a tapping capacitor will not affect S_{dd21} (see Fig. 23). Adding a tapping capacitor cancels the EPC of the coupled windings and

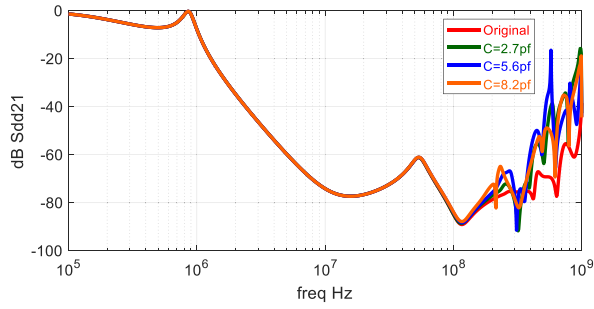


Fig. 23. Simulated S_{dd21} of the filter with different tapping capacitor values.

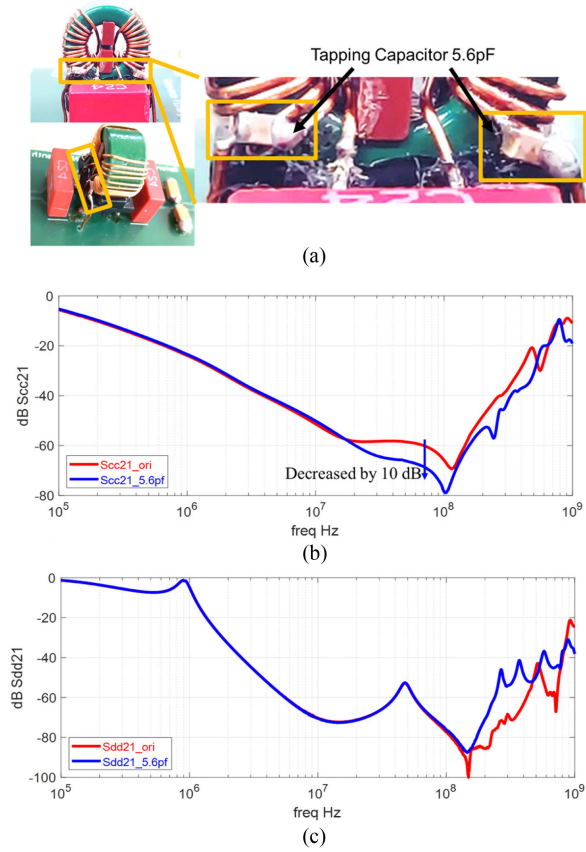


Fig. 24. (a) Installation of the tapping capacitor on the windings of the CMC. (b) Performance of the filter S_{cc21} in comparison with the original filter configuration. (c) Performance of the filter S_{dd21} in comparison with the original filter configuration.

introduces two equivalent Y-caps and a negative capacitor that cancels EPC of coupled inductors, as shown in Fig. 19. Therefore, the tapping capacitor only affects the CM attenuation of the EMI filter (since no asymmetry is added). DM transmission can be affected if additional degrees of freedom are used, such as different tapping points for the windings.

From the curves abovementioned, it can be determined that the capacitance around 4 pF will yield the largest improvement of the CM suppression at 70 MHz. The tapping capacitance within the range of 2–6 pF leads to at least 5 dB improvement in S_{cc21} at 70 MHz. The tapping technique is then put to measurement (see Fig. 24), with a 5.6 pF additional capacitance

added to the first turns of the CMC windings. The measurement shows 10 dB improvement in the S_{cc21} at 70 MHz, which is close to the predicted value in Fig. 21. (5.6 dB improvement). The DM attenuation in the range of 10 MHz–100 MHz is not affected, as shown in both simulation and measurement. At higher frequencies introducing the tapping capacitors reduces the DM attenuation, which is correctly predicted by simulation.

V. SUMMARY

In this article, a 3-D modeling strategy for EMI filters is proposed and evaluated. The model takes into account the internal structure of the film capacitor, the CMC, and the ceramic capacitor. Blocks and thin wires are implemented to avoid explicit modeling of the internal structure of the capacitors and simplify the CMC model, relieving the burden of the solver and mesh generator. The need for model parameter tuning is also minimized in the proposed strategy. The only parameter that requires tuning is the equivalent parallel capacitance of the choke (through the permittivity of the equivalent dielectric layer in the model).

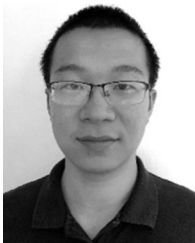
A 3-D model is built for an example EMI filter, the model demonstrated the ability of the proposed strategy to predict the filter performance up to 1 GHz (with various accuracy across the frequency range, but qualitatively correctly). An example of the procedure of improving the filter design utilizing the 3-D model is presented.

Section IV demonstrates that the effect of the tapping capacitors on the filter performance is correctly predicted up to 1 GHz for both common and differential modes. The proposed modeling strategy is, therefore, useful for not only the early design stage of EMI filters, but also at the iterative stage, where multiple parameters need to be changed to fine-tune the filter performance.

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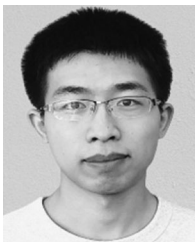
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