

Rapid Cleanroom-Free Fabrication of Thread Based Transistors Using Three-Dimensional Stencil-Based Patterning

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Abstract

Applications such as wearable electronics and flexible displays have led to considerable advancement in flexible electronic materials. Textile threads have recently emerged as a flexible substrate with unique properties like biocompatibility, three-dimensional (3D) interfacing, and processability. However, fabrication of transistors and integrated circuits on threads remains a challenge. We address this need with a low-cost, high-throughput and cleanroom-free fabrication method for ionogel-gated organic Thread-Based Transistors (TBTs). It makes use of a three-dimensional flexible “stencil” to fabricate the active channel area gap. Similar to stencils used in screen printing on 2D substrates, the stencil provides a 3D mask for spatially targeted printing on thread-based substrates. Carbon ink is coated using this 3D stencil on the thread to act as source and drain electrodes, along with poly(3-hexylthiophene) (P3HT), a proven organic semiconductor as a proof of concept. We achieve consistent simultaneous batch fabrication of over tens of transistors with a threshold voltage of $-(1.48 \pm 0.11)$ V, an operating region of 0 to -3V, and an ON/OFF ratio of the order of 10^2 .

1. Introduction

In the past few decades, wearable devices have led to major advances in flexible electronics with improved substrates, semiconductors, gate materials and electrodes.(1,2) These advances are the result of adapting two-dimensional (2D) electronics to three-dimensional (3D) surfaces like the human body, and are complemented by the advancement of the industry towards flexible displays.(1,3,4) Multifilament textile fibers, or threads are one such intrinsically flexible platform with unique applications in wearable electronics.(5,6) Threads can be made out of biocompatible fibers,(7) can interface well with three-dimensional tissues and organs,(5) and spools of threads can be dip coated, or fabricated in a high throughput manner, such as a reel-to-reel process.(8) Previous works on thread-like transistor geometries have produced Organic Electrochemical Transistors (OECTs) and Organic Field Effect Transistors (OFETs) spanning a variety of applications.(9–13)

Much work has been done in the field of thread-based electronics, but previous works are either on wire-like substrates,(10,14) or the fabrication processes for thread based transistors are not high throughput.(7,11) Moreover, workers have previously relied on classical cleanroom deposition methods for fabrication, which limits ambient operation of devices. Recently, Owyung et al. proposed a new method of Thread-Based Transistor (TBT) fabrication which proposes the use of gold wires as source and drain electrodes that are physically knotted onto the base thread, thus creating the active channel area without the use of a cleanroom.(7) The fabrication method allowed for a cleanroom-free approach for creating CNT and P3HT p-type TBTs. However, the manual method of knotting the gold wires in this process limits production scalability, and gold adds to the cost of the TBT. A high throughput, low-cost fabrication method is required so that multiple TBTs can be made to realize more advanced integrated circuits such as amplifiers, transmitters or microcontrollers. These systems require a high number of transistors, with consistency in properties like the threshold voltage and the ON/OFF ratio.

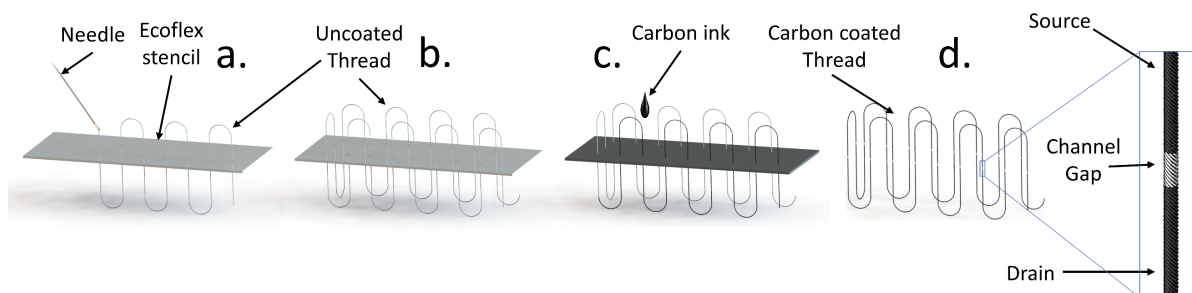


Fig. 1. Schematic of various stages of the fabrication process. A long uncoated thread is sewn through the stencil (a). Once fully sewn (b), the thread is coated with carbon ink (c). Removing the thread from the stencil reveals source and drain channel gaps where the stencil used to be (d). This is followed by coating with the semiconducting channel material (not shown).

In this report, we propose to extend the well-known 2D screen printing to the third dimension. Screen printing uses a stencil or a mask to define spatial patterns where the ink can be deposited and where it cannot. In this report, we employ a three-dimensional stencil using a flexible Ecoflex “stencil” to spatially define the active channel area gaps for multiple TBTs in 3D simultaneously. As shown schematically in Fig. 1, multiple transistors can be realized by sewing threads through the mask, then simply coating the exposed thread with carbon ink. Coated areas will serve as source and drain terminals. Areas of the thread covered by the 3D stencil will not be coated with the carbon ink, thus many active channels can be fabricated on a singular thread or many different individual threads with a one-step carbon coating. The flexibility of the mask allows for easy insertion of the thread substrate when stretched and provides a tight seal around each thread to inhibit electrode ink seepage during coating. With two versions of the fabrication process highlighting the effect of removing excess semiconductor during the process of semiconductor deposition, we demonstrate that the active channel conductivity is of paramount importance to achieving device consistency.

We also present the electrical characteristics of a typical TBT formed by this process as well as parameters for consistency of TBTs within a batch. We find that the proposed method produces TBTs with a consistent threshold voltage and ON/OFF ratio with values in the expected range for flexible organic ionogel-gated transistors, thus providing a novel low-cost, cleanroom-free and high throughput TBT fabrication process. While the process presented here was done manually, an automated process is expected to correct for any residual process variability to provide less device-to-device variations.

2. Methods

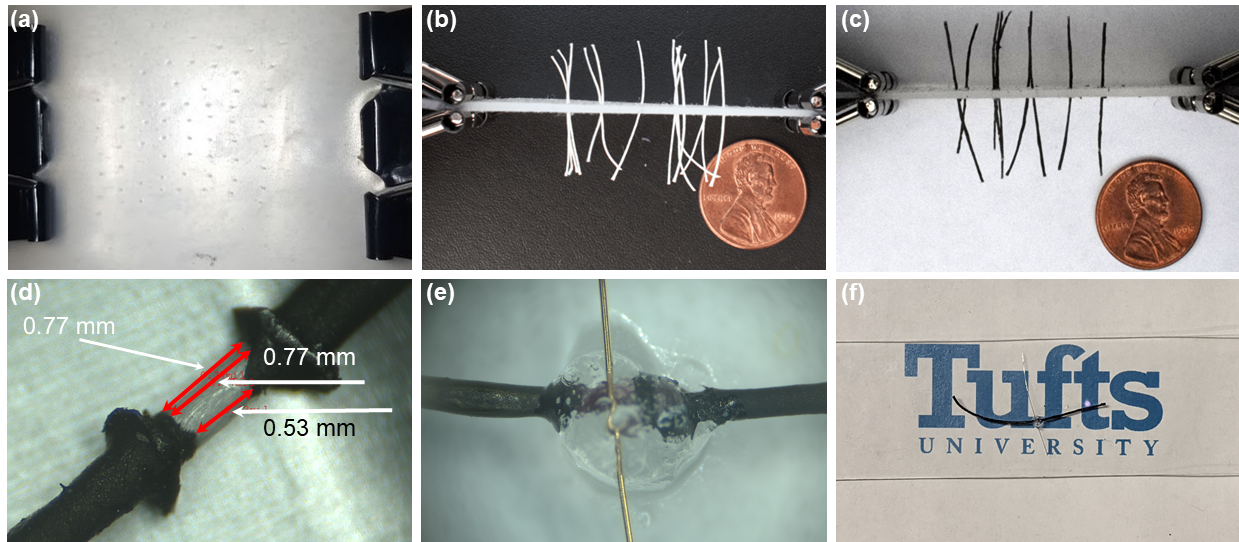


FIG. 2. A three-dimensional Ecoflex stencil mask (a) with holes pierced, (b) with threads embedded, (c) with embedded threads coated with C ink. (d) Microscope image of thread prior to addition of semiconductor. Fully fabricated TBT (e) zoomed in and (f) zoomed out.

Fig. 2(a) shows the various stages of the batch fabrication process. The paramount challenge of batch TBT fabrication is to ensure that a sub-millimeter sized gap between the source and the drain can be reliably formed. Our solution involves a stretchable Ecoflex sheet that the threads are pierced into for a three-dimensional electrode mask. The thickness of the Ecoflex sheet dictates the length of this gap between source and drain electrodes (also the channel length of the transistor). First, holes are pierced into a stretched Ecoflex stencil sheet (Fig. 2(a)). While this stencil is still stretched, linen threads are embedded into the holes (Fig. 2(b)) and the sheet is allowed to contract to its original dimensions (see supplementary section for details). While we employed linen for initial demonstration, other thread/textile materials could easily be substituted instead, so long as the solvent used for semiconductor dispersion does not degrade underlying threads and is readily adherent to the thread. If stretched adequately before holes are pierced, the hole size after the sheet contracts is smaller than the diameter of a thread substrate. This ensures that a tight seal is formed around the threads for well-defined electrodes.

The source and drain contacts in the TBTs are formed by coating Carbon ink on the embedded linen threads with a fine brush (Fig. 2(c)).⁽¹⁵⁾ The resulting resistance was $719 \pm 66 \text{ } \Omega/\text{cm}$. Carbon was chosen as the material for the source and drain electrodes as it has successfully been used in flexible electrodes or electrolyte gated transistors.^(16–18) Carbon ink is also readily available in a low-cost, liquid form, which facilitates rapid application in the high throughput fabrication process. Carbon, apart from noble metals like gold, is also compatible with gel electrolytes,⁽¹⁹⁾ which permits our use of ionogel gating. However, carbon ink properties, such as viscosity, could be optimized to improve device performance, to prevent pooling of excess carbon ink at the thread/ecoflex mask interface, and to prevent ink seepage for thinner ecoflex mask applications. Once the ink has cured, the threads are pulled out of the mask (Fig. 2(d)) and the source/drain gap is realized.

Ideally, the semiconductor gap formed should have the same length as the thickness of the sheet. However, some seepage of the carbon ink into the channel is inevitable, resulting in variance of channel diameter, (see Fig. 2(d)). During current implementation, this is primarily due to manual inaccuracies of using a paint brush for non-systematic application of ink. Transistors fabricated need to be characterized with well-known transistor parameters (channel length, width, threshold voltage, mobility etc.). We determine an equivalent channel length (L_{eq}) to fit TBT characteristics to a general MOSFET model, which would be useful for calculations such as that of mobility. We propose L_{eq} as the harmonic mean of regularly spaced length measurements (L_i) around the thread's perimeter. The harmonic mean is defined mathematically as

$$\frac{1}{L_{eq}} = \frac{1}{n} \sum_{i=1}^n \frac{1}{L_i} . \#(1)$$

A harmonic mean is used instead of an arithmetic mean as the TBT current is inversely proportional to the length. In our experiments, we chose $n = 6$. The width, W , is defined as the circumference of the thread ($W = 2\pi r$).

Following the realization of the source/drain gap, P3HT is dropcast in the gap, which is then coated by the ionogel. We have experimented with two different methods of dropcasting P3HT (versions 1 & 2). The versions differ in whether or not visibly excess P3HT is removed. The two versions were designed to understand how excess P3HT affects the TBTs, and whether removing excess P3HT makes better devices. In the first version (Version 1) of the fabrication method, we fabricated devices with a reduced amount of P3HT in an effort to reduce the thickness of the P3HT layer deposited (See supplementary section for details). This was done to reduce electrochemical doping of the P3HT by the ionogel and possible electrical shielding due to a thick layer of P3HT.^(20–23) In this version, 0.5 μL of a 15 mg/mL regioregular, electronic grade Poly(3-hexylthiophene) (P3HT) (Rieke Metals, Lincoln, NE) solution in 1,2-dichlorobenzene (anhydrous 99%) (DCB) was drop cast between the S/D electrodes, as reported previously.⁽⁷⁾ The visibly excess P3HT was absorbed by a Kimwipe (Fisher Scientific). The TBTs were left in a fume hood for 10 minutes.

In version 2 of dropcasting P3HT, a semiconductor solution was performed as reported in version 1, and P3HT in a DCB solution was drop cast between the S/D electrodes. Instead of removing the excess P3HT, the devices were left in the fume hood for an additional 5 minutes, followed by 20 minutes at 50°C in an oven.

After the addition of P3HT in either version, a silica nanoparticle-based colloidal ionogel was pasted onto the active channel area as reported previously by Owyung et al.⁽⁷⁾ An Au wire is placed on the gel to act as the gate electrode. Thus, after the controlled dropcasting of P3HT in the source/ drain gap followed by application of the ionogel and a gold wire, a fully functional TBT is formed.

3. Results and discussion

a. Stencil material

The need for a high throughput method of fabrication of TBTs gives rise to this batch-processing inspired schema. Furthermore, in order for the method to be low cost and have low complexity, we used materials that are easily available in a laboratory setting and do not require complex instruments. This method improves upon previous manual methods to realize TBTs, as our method can easily be scaled by placing more threads within the mask to realize many source/drain gaps simultaneously.

For this fabrication process, Ecoflex is specifically chosen as the stencil over other materials such as PDMS because of its flexibility. The source/drain gap is formed while the threads are still embedded in the stencil, and they must be extracted before the application of P3HT. During

this extraction, since the sheet is flexible, little to no damage is caused to the pre-existing holes, and the same Ecoflex stencil sheet can be reused multiple times.

b. Electrode material properties

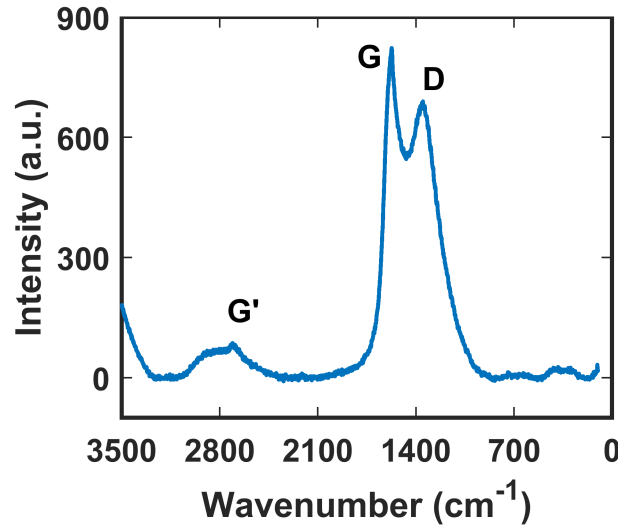


FIG. 3. Raman spectrum of the Carbon ink.

The Raman spectrum of the Carbon ink used in TBTs is shown in Fig. 3 to assess the quality of the carbon. The G band at approximately 1570 cm⁻¹ and the G' band at approximately 2710 cm⁻¹ are indicative of crystalline graphite. The D band at approximately 1350 cm⁻¹ correlates with the presence of defects caused by irregular Carbon symmetry at the edge of crystals.(24) The relative intensity of the D band as compared to that of the G band is indicative of the Carbon purity.(25) The intensities are nearly the same, indicating a degree of impurity, which is to be expected of this carbon ink. Regardless, electrical characterizations of the TBTs show that the carbon ink acts as a good conductor as the source and drain electrodes.

As discussed previously, some seepage of the carbon ink into the channel is inevitable. In future iterations through automation, threads can be ensured to be perpendicular to the mask to a high degree of accuracy and application of the ink can be done using aerosol jet spraying or another systematic applicator. With a sufficiently thin stream of carbon ink in the plane of the mask, ink seepage into the semiconductor channel can be reduced to give TBTs with even better consistency in dimensions for this current proof-of-concept demonstration. We can explore alternative methods for coating of the conductive material, such as automated dip-coating or automated spray-coating. We are encouraged by past works that have shown that carbon can be spray coated onto different substrates,(26,27) with even optimized trajectories for 3D surfaces.(28) Chemical Vapor Deposition (CVD) is another high throughput method that has been used in textile manufacturing to produce wearable electronics.(29) Past works have also

demonstrated inkjet printing on fabrics,(30,31) aerosol jet printing(32) and dip coating(33,34) as viable alternatives that can be adapted to our high throughput fabrication process.

c. Electrical Characteristics of Fabricated TBTs

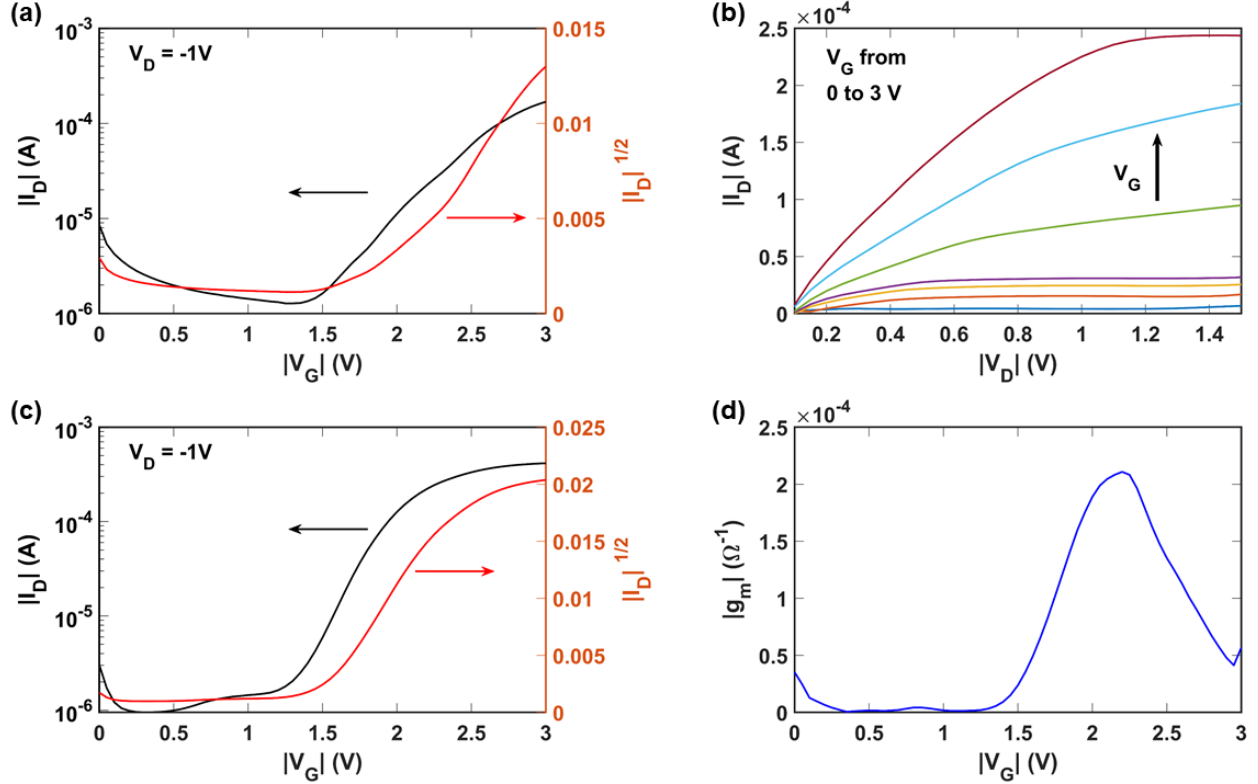


FIG. 4. (a) I_D-V_G and (b) I_D-V_D curves for a device fabricated using version 1. (c) I_D-V_G and $I_D^{1/2}-V_G$ curves for a champion device and (d) transconductance (g_m) for the an average device fabricated using version 2.

Fig. 4(a-b) shows the I_D-V_G and I_D-V_D curve, respectively, for a device fabricated with version 1 of the fabrication process. The threshold voltage is calculated as the intersection of the extrapolation of the OFF current and the linear regions in the $I_D-V_G^{1/2}$ curve. The threshold voltage of this device is approximately -1.4 V with an ON/OFF ratio of approximately 130. However, due to the variation in amounts of the semiconductor deposited and unknown amounts wicked away via kimwipe, this method was found to unsatisfactorily provide consistent TBTs.

Since the excess P3HT wicks down the length of the thread underneath the carbon coating, it does not have a detrimental effect on device performance and wiping may not be necessary. Thus, we can achieve a consistent amount of P3HT deposited by simply dropcasting P3HT from solution, as used in version 2 of the fabrication process. We observed yields of 70% - 90% for for a batch of ten transistors at a time. The I_D-V_G and $I_D^{1/2}-V_G$ curves for a champion device fabricated using version 2 are shown in Fig. 4(c). The operating region of the transistors is from 0 to -3 V. The threshold voltage of this champion device is approximately -1.4 V with an

ON/OFF ratio of approximately 140, and an effective linear mobility of $2.8 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ calculated using Eq. 2(35):

$$\mu_{\text{lin}} = \left(\frac{L}{WC} \right) \left(\frac{I_D}{V_D(V_G - V_T)} \right) \text{ for } |V_G - V_T| \gg |V_D|. \#(2)$$

where L and W are the channel length and width of the transistor and C is gate capacitance. Effective mobilities of these devices are not comparable to true mobilities of other systems, as there are several factors contributing to their appeared inflated mobilities which are computed using expressions for linear highly ordered systems. For one, high surface area of the thread fiber bundles leads to an underestimation of the width of the transistor. We have performed Raman spectroscopy and looked at optical images of the cross section of the P3HT coated thread after deposition and thorough drying (see Supplementary Figure S1). Our results indicate that P3HT is impregnating the fibers, thus the mobilities would be lower than the curves suggest. Additionally, large charge densities from the high capacitance of the ionogel ($18 \text{ } \mu\text{F}/\text{cm}^2$ at 1 Hz) will also contribute to a higher estimate of effective mobilities from experimental data. Finally, these devices do not necessarily follow transport mechanisms used to model solid-state devices, as previously reported elsewhere. Values reported using this model might not account for contact resistance, carrier trapping, and nonuniformities in the semiconductor channel. (19,20,36–38).

Fig. 4(d) shows the transconductance (g_m) of an average device, which relates the input voltage to the output current of a device, and directly correlates to the amplification of the signal. It is also the partial derivative of I_D with respect to V_G . The maximum g_m for the TBT shown in Fig. 4(d) is 2.0×10^{-4} at 2.2 V, but we observed a maximum of 4.8×10^{-4} observed at $V_G = -2.1\text{V}$ for a champion device. The high value of transconductance will facilitate its application in analog circuits such as amplifiers.

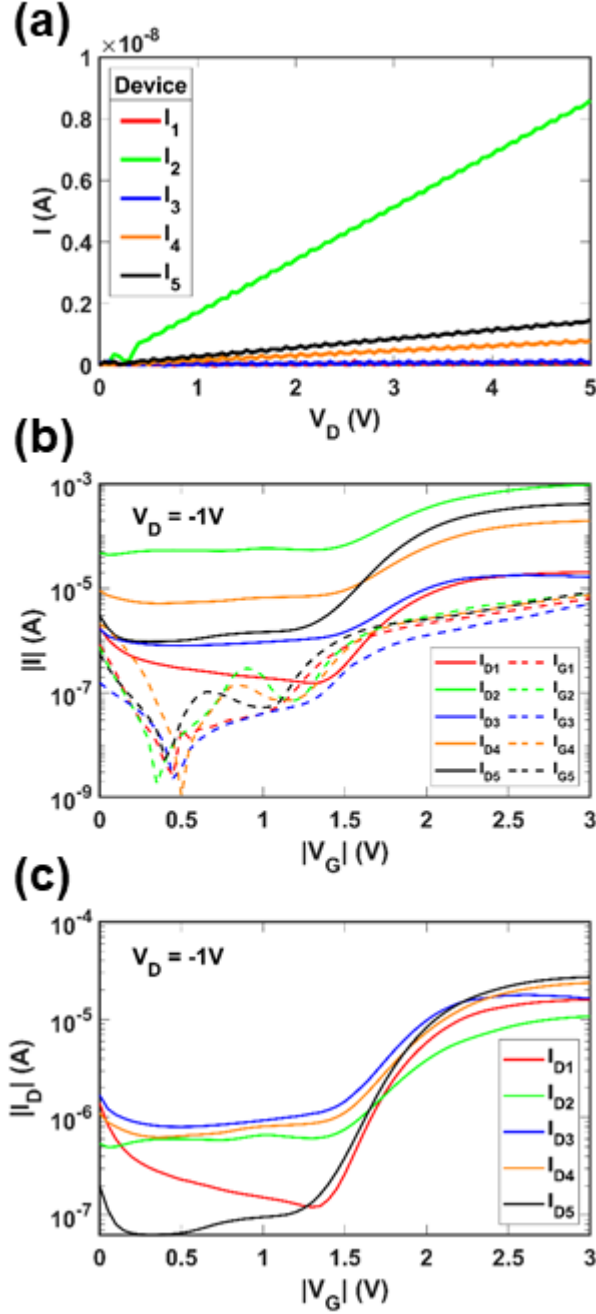


FIG. 5. (a) Current across semiconductor channel v/s applied voltage across drain and source. I_D - V_G curves for a sample set of TBTs (b) Uncorrected, with included gate leakages. (c) Corrected.

Prior to the deposition of the ionogel on a thread (penultimate stage), the current across the semiconductor channel increases linearly with V_D , as expected for ohmic contacts. This is shown for a batch of threads in Fig. 5(a). This resistance varies across devices; inconsistency across different devices within a batch can be attributed to 2 factors: small imprecision of the deposited amounts of the semiconductor, and differing gap lengths. These arise in our

fabrication method due to manual involvement; future automated iterations as discussed previously will improve upon both factors.

The gap resistance in the penultimate stage is also used to correct the I_D - V_G curve by normalizing to the transistor with the lowest OFF current. Each TBT 'i' within a batch is corrected by an amount proportional to its gap resistance as follows:

For a given batch of TBTs, we choose a TBT 'i', and call its slope in the penultimate I_D - V_D curve m_i .

Then,

Define m as the set of all m_i ,

$$m_{\min} = \min(m),$$

$$n_i = \frac{m_i}{m_{\min}} \cdot \#(3)$$

The I_D - V_G curve of each TBT 'i' is then divided by its corresponding n_i to give the corrected curve.

The uncorrected and corrected curves for a batch of TBTs are shown in Figs. 5(b) and 5(c) respectively. The gate leakages observed could be a result of the carbon ink pooling next to the channel gap, and we are actively working to reduce these deposits for improved device performance. The ON/OFF ratio for this batch is 21.9 ± 5.6 excluding the champion device at 140, and the threshold voltage, V_T for the set is $-(1.5 \pm 0.1)$ V. We have commonly observed the ON/OFF ratio to be of the order 10^2 , occasionally going up to 10^3 . The effective linear mobility of the uncorrected set calculated using Eq. (2) is $(2.4 \pm 2.9) \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

The high standard deviation here is expected since the set is uncorrected; the effective linear mobility for the set corrected to the transistor with the lowest OFF current is $(0.14 \pm 0.07) \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. This shows that the mobility is more consistent after accounting for device variability.

4. Conclusion

In conclusion, we have introduced a novel three-dimensional stencil-based patterning of three-dimensional devices. We utilized this new process to demonstrate a high-throughput, low-cost, cleanroom free method for the fabrication of Thread Based Transistors (TBTs). Simple manual deposition of inks was performed for the creation of source and drain contacts, and the organic semiconducting channel. A method with these properties is necessary for realizing interconnected complex thread-based integrated circuits such as amplifiers, transmitters etc. While there are still inconsistencies in device performance due to manual error from coating of the carbon ink, they are not inherent to the deposition process and can be improved in the future through automation. 3D stencil-based patterning is also compatible with other deposition techniques such as aerosol jet printing, spray coating, and chemical vapor deposition. We are

actively exploring alternative or optimized conductive coatings to improve device consistency and reduce channel lengths for better device performance. This work has demonstrated a proof-of-concept, cleanroom-free fabrication process to realize many active channel areas for 3D transistors simultaneously. This can be adapted for any thread or wire substrate to conformally coat conductive ink in a cylindrical pattern, thus making it an ideal manufacturing method for large area circuits using TBTs. The technique can also be extended to high throughput fabrication of sensors, actuators and other electronic devices (e.g. diodes) on threads.

Supplementary Material

See supplementary material for summary of materials and methods of fabrication.

Acknowledgements

Funding for this work was provided by National Science Foundation NSF CBET- 1951104, DRL- 1931978 and CBET-1935555. Authors would also like to thank Prof. Matthew Panzer, Department of Chemical and Biological Engineering, Tufts University for providing some materials to realize ionogels. T.K. wishes to thank Mykhaylo Chumak for assistance in capturing pictures.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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