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High Current Density $SmTiO_3/SrTiO_3$ Field-Effect Transistors

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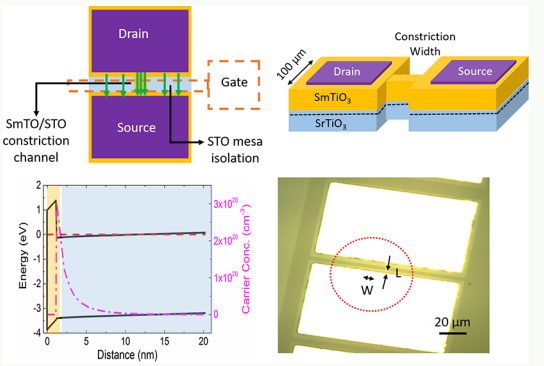
ABSTRACT: $SmTiO_3/SrTiO_3$ interfaces are of potential interest for electronic devices as they exhibit novel electronic phenomena such as metal−insulator transitions. However, good transistor performance from this material system requires advances in both device design and processing. Here, we demonstrate high current density $SmTiO_3/SrTiO_3$ transistors with good pinch-off by minimizing parasitic series resistances and improved field management using a narrow-channel constriction architecture. Constriction devices show improved pinch-off behavior and saturation current densities at room temperatures of 350 mA/mm along with transconductances of 200 mS/mm, which are the highest reported values for $SrTiO_3$-based transistors. Temperature-dependent measurements reveal that these $SmTiO_3/SrTiO_3$ channels exhibit insulating behavior with the sheet resistance of the channel increasing with decreasing temperatures indicative of hopping transport of carriers in these devices.



KEYWORDS: *oxide heterostructures, complex oxides, oxide transistors, parasitic resistance, $SrTiO_3$, hopping transport*

INTRODUCTION

Complex oxide interfaces exhibit a diversity of electronic properties such as ferroelectricity, interface magnetism, metal−insulator transitions, and superconductivity, to name a few.[1−7] This makes them ideal platforms to study fundamental solid-state phenomena as well as potential device applications. For instance, the existence of a 2DEG at $LaAlO_3/SrTiO_3$ interfaces, due to the polarization discontinuity between these materials, has spurred the investigation of field-effect transistors on this material system.[8−11] However, the experimentally observed carrier densities at this interface are significantly lower (in the 10^{13} cm^{-2} range) than the ideal expected value of 3.3×10^{14} cm^{-2}, which has been attributed to inadequate passivation of the $LaAlO_3$ surface.[12] Several proposals such as the use of modulation doping and the use of interlayers and overlayers have been utilized to raise the charge density of $LaAlO_3/SrTiO_3$ 2DEGs.[13−16] On the other hand, very high charge density 2DEGs in $SrTiO_3$, with the complete 0.5 electrons per unit cell, have been realized at interfaces with other rare-earth titanates such as $GdTiO_3$ and $LaTiO_3$ among others.[17,18] These structures are very promising for transistor applications in view of their extremely high channel charge densities.

More recently, 2-D electron systems with very high charge densities have been demonstrated at $SmTiO_3/SrTiO_3$ (SmTO/STO) interfaces along both the (001) and (111) orientations.[19,20] These heterointerfaces also exhibit tunable charge densities based on the thicknesses of the SmTO and STO layers used. Furthermore, the SmTO/STO interface has been shown to exhibit novel metal−insulator transitions (MIT) phenomena, both in proximity to the two-dimensional Mott−Ioffe−Regel (MIR) limit (sheet resistance of h/e^2 = 25.88 kΩ/□) for samples with low sheet charge densities as well as for high charge density samples with sheet resistances far below the MIR limit.[21,22] While the physical origins of this MIT are still under investigation, the strong carrier density dependence of the MIT transition temperature observed at these interfaces raises the possibility of experimentally realizing an electrostatically controlled MIT phase-transition transistor at room temperature, an outcome that would be transformative for next-generation switching devices.

However, several challenges relating to material growth, device design, and fabrication need to be overcome prior to the demonstration of high-performance $SrTiO_3$ field-effect transistors (FETs), whether conventional or phase-transition based. Modulation of the extremely large channel charge densities is one of these challenges. Charge densities greater than 10^{14} cm^{-2} have been successfully modulated by using the high-κ $SrTiO_3$ as the top layer by itself in "inverted" $SrTiO_3/GdTiO_3$ structures[23,24] and in conjunction with a finFET geometry in an inverted STO/SmTO stack.[25] The other related challenge has been realizing high-current density transistors based on STO 2DEGs with good pinch-off behavior. While electric-field induced modulation in SmTO/

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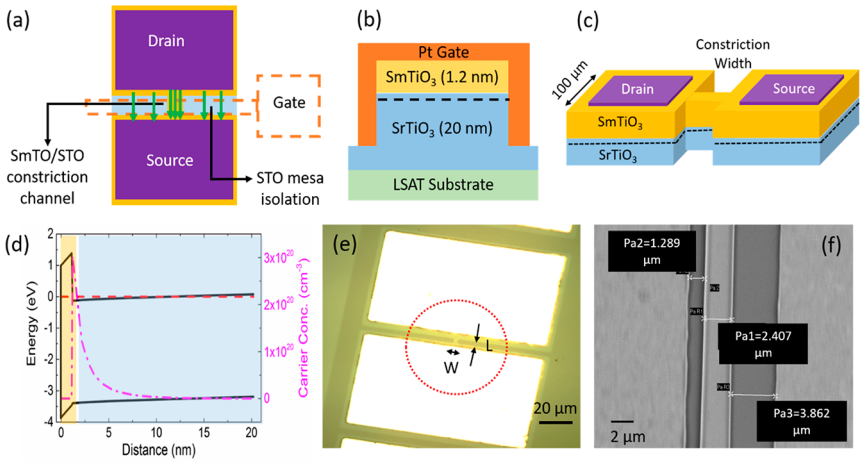

Figure 1. (a–c) Schematic of the top, cross-sectional, and 3-D views respectively of the I-shaped constriction transistor with the narrow SmTO/STO channel. Green arrows in (a) indicate current flow between the source and drain contacts due to the channel as well as surrounding STO mesa isolation as discussed in the text. (d) Band diagram and carrier concentration profile of the SmTO/STO channel (1.2 nm/20 nm) assuming a net interfacial polarization charge density of 10^{14} cm^{-2}, surface barrier height of 1 eV, and 10^{18} cm^{-3} of donor density in the STO layer. (e, f) Optical and SEM micrographs of a constriction structure (within red dotted circle, W = 2.2 μm, L = 2.7 μm) without and with gate metal, respectively.

STO devices have been recently demonstrated,[22] the current densities in these devices and indeed most present-day STO transistors are quite modest. In contrast, those devices that demonstrate relatively high current densities do not exhibit well-behaved pinch-off characteristics primarily due to the modulation challenge alluded to above. More specifically, parasitic resistances in the form of contact and access resistances play a detrimental role in device performance by lowering the current drive of these transistors. It is hence important to understand and highlight the effect of such parasitic resistances on the device performance of oxide channel transistors, while addressing this issue requires the development of low-resistance ohmic contacts as well as reducing the access resistances of the more resistive channels either through scaling or utilizing alternative device architectures, such as I-shaped constriction structures with large contact pads and a thin channel region, thus reducing contact and access resistance contributions to the total device resistance.

In this work, we demonstrate high current density FETs with good pinch-off behavior using resistive SmTO/STO interfaces. The increased saturation current density was achieved by using specially designed I-shaped constriction transistors with reduced parasitic series resistances arising from contact and access resistance effects and improved electric field management. A maximum saturation current density of 350 mA/mm and a transconductance of 200 mS/mm at gate voltages of +1 V were obtained for a scaled device with gate length of 2.4 μm and channel width of 2.2 μm at 300 K, which are the highest reported $I_{D,sat}$ and g_m of any $SrTiO_3$ channel transistor. These results highlight the importance of improved transistor design and reducing the parasitic access resistances to probe the intrinsic performance of transistors made from STO-based 2DEGs and provide a route toward obtaining oxide heterostructure transistors with superior performances. Furthermore, temperature-dependent transistor characteristics also exhibit insulating behavior in the intrinsic SmTO/STO channels, where the channel resistance increases with decreasing temperatures due to the hopping nature of electron transport in these devices.

RESULTS AND DISCUSSION

SmTO/STO transistors using the I-shaped constriction geometries shown in Figure 1 were used in this study. Also shown is the band diagram of the SmTO/STO channel (Figure 1d) generated by using a 1-D Poisson–Schrödinger solver assuming an interfacial polarization charge density of −0.16 C/m^2, corresponding to 10^{14} cm^{-2} sheet carrier density, along with a background doping of 10^{18} cm^{-3} in the STO layer (other material properties as listed in the Supporting Information). The Fermi level falls above the conduction band at the SmTO/STO interface, indicating the presence of a degenerate high-density 2DEG of equivalent 3D density, n_{3D} = 3 × 10^{20} cm^{-3}. While an ideal SmTO/STO interface should have a 2-D carrier density of 3.3 × 10^{14} cm^{-2}, the present 3 unit cell SmTO/20 nm STO samples have been shown to have lower charge densities of ∼10^{14} cm^{-2} due to surface depletion.[22] The sheet resistance of the as-grown SmTO/STO stack as estimated by four-terminal Van der Pauw measurements was 31.56 kΩ/□, close to the 2-D Mott–Ioffe–Regel limit of 25.88 kΩ/□ (= h/e^2) beyond which insulating behavior is expected for a 2-D system.[26] These sheet resistances are on the higher side as compared to commonly used wide-band-gap semiconductor channels such as AlGaN/GaN (R_{sh} ∼ 200–500 Ω/□)[27] or Ga_2O_3 (∼8 kΩ/□),[28] which makes it challenging to reduce the contact and access resistances of any fabricated transistors and hence to probe the intrinsic performance of these SmTO/STO channels. In this regard, specially designed I-shaped constriction structures, with large contact pads but narrow channel widths, are used in this study to minimize the contributions of the contact and access resistances as the total device resistance is now dominated by the channel resistance. The contact and access regions were fabricated having a width of 100 μm while the constriction channel itself had a narrower widths of 2 and 5 μm (see 3-D view in Figure 1c).

The effect of the constriction geometry can be clearly seen in the transistor output characteristics of the constriction devices when compared to control planar transistors without a constriction (device width = contact pad width = 100 μm) as plotted in Figure 2. We see that the current density as well

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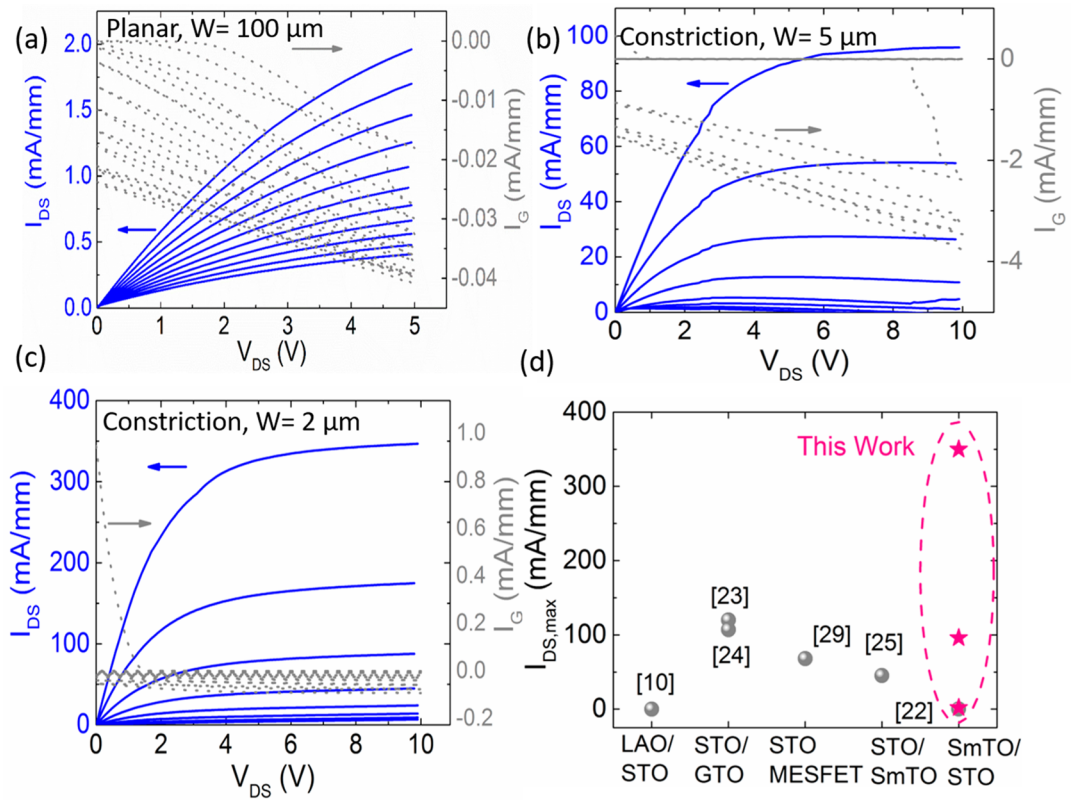

Figure 2. Transistor output characteristics, along with gate currents on the right axis, measured at room temperature for (a) planar devices for V_G ranging from −10 to 0 V in 1 V steps, and constriction devices of (b) $W = 5$ μm and (c) $W = 2$ μm, for V_G ranging from −6 to +1 V. Constriction devices show higher current densities and pinch-off behavior in contrast to the planar transistors. (d) Comparison of reported maximum current densities ($I_{DS,max}$ in mA/mm) for a range of STO-based field-effect transistors (with $LaAlO_3$, $GdTiO_3$, and $SmTiO_3$ heterointerfaces and $SrTiO_3$ MESFETs) reported in the literature with the present work.[10,22−25,29]

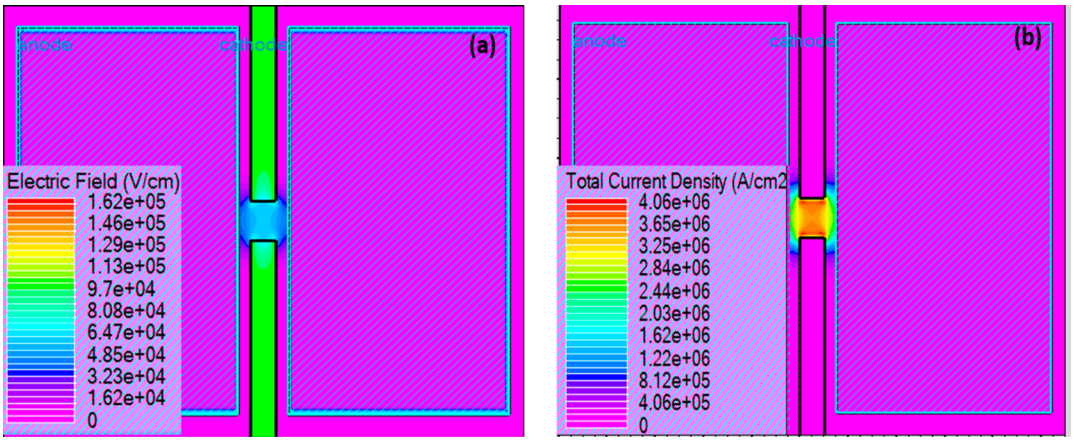

Figure 3. Device simulations showing the effect of the constriction geometry on the (a) electric fields and (b) current densities, for a uniformly doped semiconductor constriction channel of 10^{20} cm^{-3} with 10 V applied bias. The field profiles are quite uniform across the constriction structure, while current densities are confined to the narrow constriction with some current crowding observed around the edges.

as pinch-off behavior of the transistors dramatically improve for the constriction structures as compared to the planar transistor. Furthermore, the narrower (2 μm) constriction width devices show much higher current densities as compared to the wider (5 μm) devices for identical gate lengths (L_G), source−gate (L_{SG}), and gate−drain (L_{GD}) spacings as shown in Figure 1f. While planar devices showed a maximum current density of 2 mA/mm with limited current modulation and no evidence of pinch-off behavior (Figure 2a), $I_{DS,max}$ values of 96 and 350 mA/mm were observed for the 5 μm and 2 μm constriction devices respectively, along with improved current modulation and drain pinch-off (Figures 2b and 2c). In the case of transistors with low parasitic source and drain resistances, scaling the width of the device does not significantly alter the width-normalized current density. However, this is contrary to the present observations on the SmTO/STO transistors. Here, reducing the constriction width increases the contribution of the SmTO/STO channel to the total device resistance while any parasitic series resistances remain unaltered as the dimensions of the contact, and source

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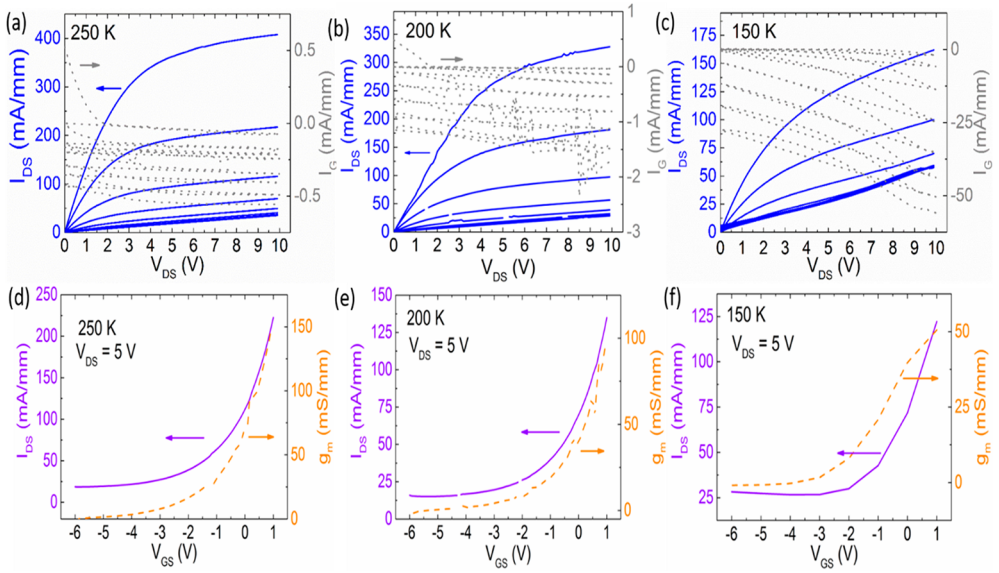

Figure 4. Temperature-dependent transistor behavior of the 2 μm constriction devices showing output characteristics and gate currents for V_G of −6 to +1 V in 1 V steps and transfer curves with transconductances at a V_{DS} of 5 V at (a, d) 250 K (b, e) 200 K, and (c, f) 150 K. Current densities and transconductances monotonically drop with temperature, indicative of insulating behavior of the SmTO/STO channels.

and drain access regions are essentially the same. Therefore, the fractional contribution of the parasitic source−drain resistances to the net device resistances reduces with decreasing constriction widths and allows us to obtain larger current densities which are more reflective of the intrinsic channel resistances. It must be mentioned that for an ideal STO transistor under the gradual channel approximation having the same dimensions, a channel mobility of 10 cm^2/V, a measured C_{ox} of 4.63 $\mu F/cm^2$, and a threshold voltage of −6 V, the saturation current density for V_G = +1 V should be 473 mA/mm (see the Supporting Information for more details).

Additionally, the geometry of the constriction structures also improves field management in these transistors by better confining the current within the constriction. This can be seen in Figure 3 where the total electric field and current density of an exemplar constriction structure surrounded by an insulator in the gap region has been plotted using 2-D device simulations. A uniformly doped n-type channel of 10^{20} cm^{-3} was assumed, analogous to the 3-D doping densities in the present SmTO/STO channels along with 10 V of applied drain bias. While some current crowding can be seen at the edges of the device from Figure 3b due to its geometry, the electric field in this device in Figure 3a is not only well-confined to the narrow channel but also relatively uniform. Such constriction channel devices have previously been used to measure velocity saturation in various semiconductors due to their well-defined electric field profiles[30,31] and have also shown superior breakdown fields on resistive AlGaN MISFETs due to their geometry as compared to planar transistors.[32] Together these two effects—reduced parasitic resistances and the superior field management—contribute to the improved device performance in terms of higher current densities and better pinch-off behavior observed here. The current densities achieved in this study are among the highest reported for any $SrTiO_3$ channel transistor as shown in Figure 2d, in comparison with the commonly used field-effect transistor architectures including $LaAlO_3$ (LAO), $GdTiO_3$ (GTO), and $SmTiO_3$ barriers. This clearly indicates that strategies to reduce parasitic series resistances and effective electric field management would play a major role in improving the performance of $SrTiO_3$ channel-based field-effect transistors.

On the other hand, the I_{ON}/I_{OFF} ratios of these devices remain modest (∼12) due to the correspondingly higher off-state currents. The gate leakages of all devices are quite low, as shown on the right axes of Figures 2a−c, indicating that the high off-state currents for these transistors are due to source−drain leakage, possibly due to a combination of incomplete channel charge modulation along with some bulk leakage from the remaining ∼10 nm etched STO layer which typically contain 10^{18} cm^{-3} of oxygen vacancies.[33] The constriction configuration can be thought of as being equivalent to a large 100 μm wide STO MESFET in parallel with the actual 2 μm wide SmTO/STO FET (see Figure 1a). This large difference between the widths could increase the contribution from the mesa-etched STO layer to the total measured currents. To ensure that this was not the case, gate fingers were also deposited between 100 μm wide contact pads directly on the etched STO layer itself, without any constriction channel between the pads. Measured currents were found to be small (<15% of total measured currents of the SmTO/STO constriction channels as shown in the Supporting Information), indicating that the resistivity of the etched STO layer was much larger than 2DEG channel resistivity. Hence, the observed current densities in these constriction devices were indeed reflective of the SmTO/STO channels and not the background doping in the STO layers. The effect of the STO isolation on the constriction transistor characteristics has been accounted for in Figures 2b and 2c by subtracting out the measured currents from the transistor output curves of an isolation FET to reveal the true current densities in these channels (see the Supporting Information). We see that despite subtracting out the conductivity of the STO layer, the OFF current in the 2 μm device, for example, was 10 mA/mm even at a V_G of −6 V, indicating incomplete channel charge modulation. Given that the channel charge density in these devices was ∼9 × 10^{13} cm^{-2}, modulating such a large amount of charge would require the use of strategies such as high-k

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layers or additional depletion using FinFET structures or some combination of both as discussed earlier in the Introduction.

Low-temperature measurements of transistor characteristics were then undertaken on the 2 μm wide constriction devices to more closely study the intrinsic carrier transport of these gated SmTO/STO channels without any parasitic resistance effects. The temperature-dependent output and transfer curves were measured down to 150 K in 50 K steps and are shown in Figure 4 for temperatures less than 300 K. Gate leakages steadily increased at lower temperatures until current modulation was limited by the high gate currents at 150 K. We see that the drain currents and transconductances steadily decrease in both the linear and saturation regimes as temperature decreases, which is characteristic of insulating behavior. $I_{DS,max}$ reduces to 162 mA/mm at 150 K while maximum g_m drops from 200 mS/mm at 300 K to 50 mS/mm for a drain voltage of 5 V. These observations are in contrast to the low-temperature characteristics of conventional semiconductor 2DEG systems, whether Si inversion layers or AlGaN/GaN high electron mobility transistors.[34,35] In these systems, the 2DEG density remains fairly constant while the mobility, however, increases with decreasing temperatures due to reduced phonon contributions to scattering, which in turn leads to an increase in current densities.

These observations are consistent with the previous report on circular transistors on such 1.2 nm SmTO/20 nm STO channels, which were also found to show insulating behavior in the 200−400 K temperature range.[22] We note that the device resistances in the present scenario are predominantly due to the SmTO/STO channel with minimal series resistance effects in the measurement and are more representative of its intrinsic behavior. Such an increase in R_{sh} with decreasing temperature is typically seen due to the hopping transport of electrons in these disordered systems where the conductivity exhibits a $\exp(-T/T_0)^{-\alpha}$ dependence as observed previously for SmTO/STO samples (also see Figure S6).[22] These results highlight the opportunities for integrating novel materials and device architectures to reduce contact and access resistances in perovskite oxide transistors. For instance, the integration of SmTO/STO channels, where the actual switching behavior takes place due to conventional charge modulation or an MIT phenomenon, with emerging perovskite oxides such as $BaSnO_3$, which have high mobilities and saturation velocities,[31,36,37] in the contact and access regions would offer an all oxide-platform for enabling high-performance electronic devices.

CONCLUSIONS

To conclude, high current density $SmTiO_3/SrTiO_3$ field-effect transistors have been realized using an I-shaped constriction structure to minimize parasitic series resistances from contact and access regions and better electric field management offered by such an architecture. An $I_{DS,max}$ of 350 mA/mm and g_m of 200 mS/mm were obtained on a 2 μm wide constriction device, which is among the highest-reported current density for any $SrTiO_3$-based transistor at room temperature. Furthermore, low-temperature measurements revealed that the SmTO/STO channels used in this study exhibit insulating behavior with a monotonic drop in resistance with decreasing temperature due to hopping transport of carriers in the channel. These results illustrate the importance of contact and access resistance reduction schemes in enabling good performance $SrTiO_3$-based transistors.

EXPERIMENTAL DETAILS

$SmTiO_3/SrTiO_3$ heterostructures were grown on $(La_{0.3}Sr_{0.7})(Al_{0.65}Ta_{0.35})O_3$ (LSAT) substrates in the (001) orientation by using molecular beam epitaxy (MBE), with a thickness of 1.2 nm (corresponding to 3 unit cells) for the $SmTiO_3$ top layer with 20 nm of $SrTiO_3$ layer beneath; details are reported elsewhere. Device fabrication was performed using i-line (365 nm) stepper lithography for all process steps (see Figure S1 for a schematic process flow). First, ohmic contacts of Ti/Au (40 nm/200 nm) were deposited by using e-beam evaporation using a lift-off process. This was followed by mesa isolation to a depth of 9−12 nm, as confirmed by AFM, in an inductively coupled plasma reactive ion etching (ICP-RIE) system using $BCl_3/Cl_2/Ar$ etch chemistry (5/50/5 sccm, 100 W RIE and 100 W ICP powers, 5 mTorr pressure). Lastly, platinum Schottky gates of 90 nm thickness were deposited by using e-beam evaporation and lift-off to complete the device fabrication flow.

The fabricated transistors include planar devices of 2 × 100 μm channel widths as well as I-shaped constriction structures consisting of large contact pads (100 μm × 60 μm) connected by a narrow SmTO/STO channel surrounded by mesa isolation (see Figure 1a). The constriction structures had designed widths of 2 and 5 μm, with constriction lengths of 3 μm covered by the gate metal with gate lengths of 2.5−2.7 μm. SEM, AFM, and optical micrographs of the fabricated devices were obtained by using a Zeiss Ultra 55 Plus FE-SEM, a Bruker Icon 3 AFM in the ScanAsyst mode, and an Olympus BX51TRF, respectively. Device characterization was performed by using an Agilent B1500A semiconductor device analyzer fitted with a capacitance measurement unit, while low-temperature measurements were performed in a Lake Shore Cryotronics CRX-6.5K cryogenic probe station.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.9b00738.

Schematic device fabrication flow, measured transistor curves on the gated $SrTiO_3$ mesa-isolation spacings, frequency-dependent $C-V$ measurements of large-area circular capacitors on the SmTO/STO 2DEG, calculated ideal transistor curves and material parameters used for generating SmTO/STO band diagrams, TLM measurements and fractional series resistance calculations for planar and constriction structures, and temperature-dependent sheet resistances at different gate voltages for the 2 μm constriction transistor (PDF)

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Notes

The authors declare no competing financial interest.

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