A Review on Switching Slew Rate Control for Silicon Carbide Devices using Active Gate Drivers

Shuang Zhao, *Member, IEEE*; Xingchen Zhao; Yuqi Wei; Yue Zhao, *Senior Member, IEEE*; Homer Alan Mantooth, *Fellow, IEEE*

***Abstract*— Driving solutions for power semiconductor devices are experiencing new challenges since the emerging wide bandgap power devices, such as silicon carbide (SiC), with superior performance become commercially available. Generally, high switching speed is desired due to the lower switching loss, yet high *dv/dt* and *di/dt* can result in elevated electromagnetic interference (EMI) emission, false-triggering, and other detrimental effects during switching transients. Active gate drivers (AGDs) have been proposed to balance the switching losses and the switching speed of each switching transient. The review of the in-existence AGD methodologies for SiC devices has not been reported yet. This review starts with the essence of the slew rate control and its significance. Then a comprehensive review categorizing the state-of-the-art AGD methodologies is presented. It is followed by a summary of the AGDs control and timing strategies. In this work, using AGD to reduce the EMI noise of a 10 kV SiC MOSFET system is reported. This work also highlights other capabilities of AGDs including reliability enhancement of power devices and rebalancing the mismatched electrical parameters of parallel- and series-connected devices. These application scenarios of AGDs are validated via simulation and experimental results.**

***Index Terms*— Active gate driver, silicon carbide, slew rate, EMI.**

I. Introduction

THE modern power industry is calling for high efficiency power converters for applications such as distributed generations, electric vehicles, energy storage systems, and more electric aircrafts with reduced volume and cost of the systems [1]-[2]. The energy loss of the power semiconductor devices usually consists of two major parts: conduction loss and switching loss [3]. The wide bandgap (WBG) semiconductor devices, e.g., gallium nitride (GaN) and silicon carbide (SiC) devices, are approaching ideal switches due to the lower intrinsic device parasitics and reduced switching transient times, thus the switching loss is significantly reduced compared to their silicon (Si) counterparts [4]. Moreover, the annually improving yield of WBG devices drives the cost down and it results in a further increased penetration into the power industry [5]. GaN devices are now replacing their silicon counterparts in the low voltage applications (<1.2 kV) while SiC devices may dominate the medium to high voltage applications (≥1.7 kV) in the near future [6].

High switching slew rate, i.e., *dv/dt* and *di/dt*, is not always desired since it introduces challenges into the power converter design, especially the electromagnetic interference (EMI) noise immunity [7][8]. Specifically, high *dv/dt* slew rate may cause high frequency noise through coupling with the heatsink or gate driver isolated power supply and finally leads to a false triggering event [9]. Another drawback is high crosstalk noise. The fast switching transient of a device in a half-bridge configuration may interact with the Miller capacitance of the complementary side switch and results in a shoot-through event [10]. Moreover, high *di/dt* interacts with parasitic inductance of the power loop, which generates voltage overshoot and ringing on the gate [11]. In the worst case scenario, the gate loop oscillation leads to switches turn on and off repeatedly, namely self-turn-on effect [12] [13].

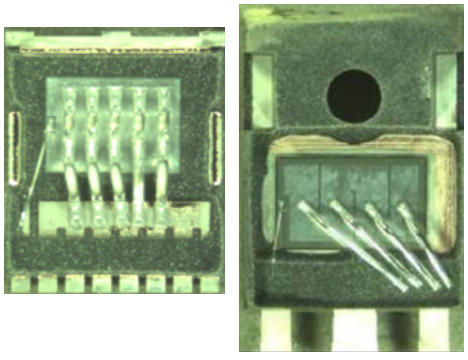

Fig. 1. A package with TO-Leadless (TOLL) package (left) compared to a TO-247 package (right).

Generally, a radical method to prevent false-triggering and shoot-through caused by high *dv/dt* is to minimize the parasitics of the power and gate loops [14]. Improving the packages of the power devices such as the Infineon CoolGaN™ devices with

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DSO package can effectively reduce the parasitics. A comparison between a surface mount TOLL package and a TO-247 package is shown in Fig. 1. The TOLL surface mountable package can reduce the parasitic inductance introduced by the leads. Also, a study investigates devices with the same bare dies in flip-chip packages and TO-247 in [15]. The flip chip packaged devices reduced the parasitic loop inductance from 15 nH in the wire bonded module to 5 nH [15]. This reduction declines the voltage overshoot and ringing by 14.2% and 8.7% respectively during turn-off [15].

The gate-loop ringing caused by common source inductance is the major reason of false triggering [16]. To suppress the voltage ringing, Kelvin connection is recommended for the gate driver connection [14]. Some new SiC discrete devices adopt TO-247-4 package which has a Kelvin pin instead of the traditionally TO-247-3 package. Nevertheless, various practical layout design constraints may hinder further reduction of parasitics on a printed circuit board (PCB) or a busbar, such as EMI immunity, insulation, and functions [17]. Also, the package of a discrete device, such as TO-247-3, inevitably introduces common source inductance close to 8 nH [18] and stray inductance in a commutation loop of a half-bridge module may be up to 20 nH [19].

High power efficiency and high EMI noise are the two edges of a sword in the power converter design. Properly slowing down of switching transient can mitigate the EMI noise and prevent false triggering yet increase power losses [14]. Through controlling the slew rate of switching, it is feasible to balance the energy loss against the EMI noise [20] and consequently optimize the switching process. A conventional slew rate adjustment method is changing the gate resistance [14]. Higher gate resistance can slow down the switching speed, thus the EMI noise is reduce. However, this method is not flexible since gate resistance cannot be changed while the converter is running. Since high gate resistance may increase the impedance of gate current route, it may increase the risk of false triggering unnecessarily in some circumstances. In addition, the slew rate of switching of the same converter can vary a lot in corresponding to the operating conditions such as load current and bus voltage [21]-[22]. As an emerging technology, active gate drivers (AGDs) can be utilized to optimize the switching transient cycle by cycle based on the feedback signals which indicates the system operation condition. Compared with the traditional methods, AGD can dynamically adjust the slew rate and provide an additional freedom for tradeoff of EMI noise against switching loss. In other words, AGD can optimize the switching process.

The AGD technology was first introduced for the IGBT turn-off protection [23]-[24]. Since then, both industry and academia have spent a significant amount of effort into the improvement of the AGD performance by dint of exploring various circuitries and control strategies. Various popular AGD methods and control strategies for IGBTs were summarized in [25]. An overview introducing various driving technologies for the SiC power devices are given in [26], with a main focus on the general driver and protection circuity for SiC devices. The extensive application of SiC devices also introduces new challenges for the AGD design. In some situations, the switching transient of SiC devices can be completed in several nanoseconds. The circuit schematics, the components bandwidth, the control strategy as well as the timing strategy should be carefully designed. For this reason, some conventional AGDs designed for silicon IGBTs are not longer suitable for the novel SiC systems. A comprehensive overview summarizing of the stat-of-the-art SiC devices AGD research is still desired because it can provide guidance to the researchers in this community and figure out the future technic path. Unfortunately, there are few publications concluding the state-of-the-art AGD methods and the slew rate control strategies for switching transient [27].

To fill this gap in the AGD research, this paper starts with the essence of the slew rate control via analyzing the fundamental mechanism with the SiC MOSFET trajectory model. Specifically, all the factors that impact the slew rate are extracted and how high slew rate of SiC devices increases EMI noise is analyzed in Section II. Based on the theoretical analysis, Section III demonstrates various slew rate control methods from gate driver side. Four types of AGDs circuits are illustrated and various on-going research of AGDs are also presented. In Section IV, three categories of in-existence control strategies and timing strategies of AGD are described in details. All AGD methodologies and control strategies are also summarized in this section. Section V points out several typical applications, i.e., on-line EMI noise suppression, reliability enhancement, current balancing of parallel-connected device and voltage balancing of series-connected device. Specifically, double pulse test (DPT) is performed to validate that AGD can alleviate the EMI noise in a 10 kV SiC MOSFET system. The switching speed rebalancing of parallel- and series-connected devices with AGD are verified with experimental and simulation study respectively. The conclusions of this review are drawn in Section VI.

II. Essence of Slew Rate Control of Power Devices

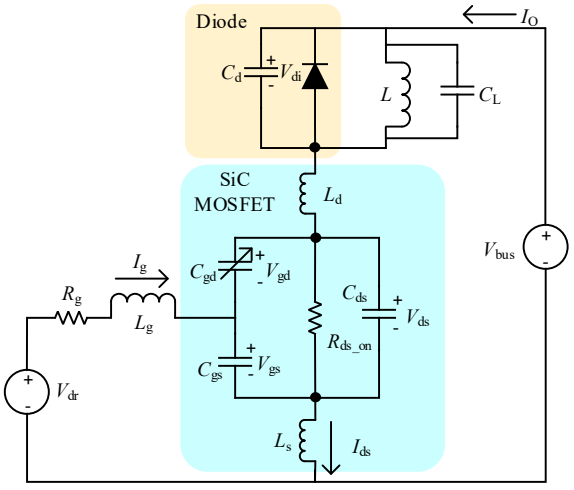

Fig. 2. The equivalent circuit of a DPT setup [1].

Fig. 2 shows an equivalent circuit of a MOSFET with the DPT setup[28]. Its gate and source terminals are connected to a

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gate driver. C_{gs} is the gate-source capacitance. C_{gd} is the Miller capacitance and C_{ds} is the drain-source capacitance. V_{gs}, V_{ds}, and V_{gd} are the gate-source, drain-source, and gate-drain voltages, respectively. L_s, L_g, and L_d represent the parasitic inductance on source, gate, and drain side. C_L is the parasitic capacitance of the load inductor.

A. *The principle of slew rate control with a gate driver*

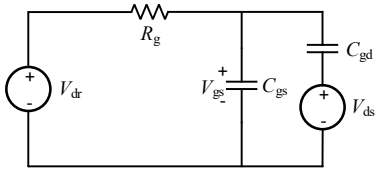

Fig. 3. The equivalent circuit of the gate driver and power device system.

From Fig. 2, the equivalent circuit of a gate driver with a power device during the switching process can be simplified as shown in Fig. 3 [29]. In Fig. 3, the intrinsic input junction capacitance of a power MOSFET, i.e., C_{iss}, is equal to C_{gs}+C_{gd}. Through charging the gate junction of the power MOSFET, the channel can be formed and the power MOSFET is conducting. During the turn-off process, C_{iss} discharges through R_g to the power supply of the gate driver.

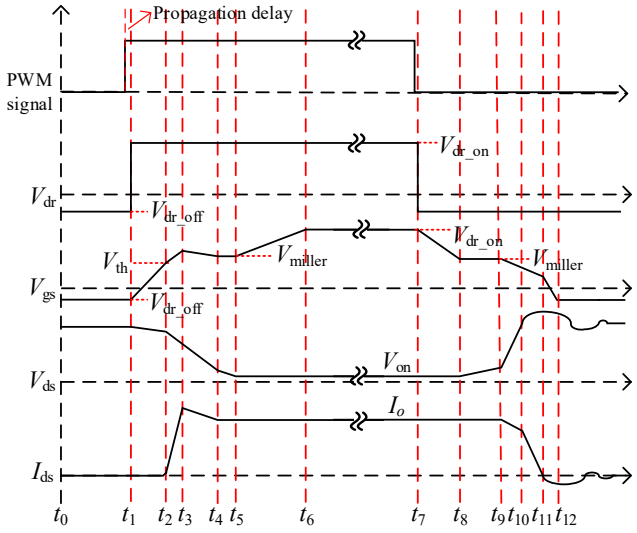

Fig. 4. The switching waveforms of a power device.

The switching transient waveforms are plotted in Fig. 4 [21]. From Fig. 4, high *dv/dt* and *di/dt* occur during the Miller plateau period when C_{gd} is charging/discharging through R_g. Correspondingly, the working principle of all slew rate control methods is to adjust the charging/discharging speed of C_{gd}. According to Fig. 3, there are several key factors affecting the gate capacitance charging/discharging speed: gate driver voltage, gate resistance, gate current, and values of C_{gs} and C_{gd} [27][30]. It should be noted that the Miller plateau of a SiC transistor is non-flat due to the low junction capacitance. The trajectory model of SiC device is slightly different from traditional model of silicon IGBT or MOSFET. The trajectory model of a SiC MOSFET can be found in [34] while silicon MOSFET model can be found in [28].

Based on the aforementioned analysis, the state-of-the-art AGD methods can be categorized into several basic types: variable gate resistance method, variable input capacitance method, variable gate voltage method, and the variable gate current method [25][30][31].

B. *Influence of different factors on the switching slew rate*

Since different AGD methodologies have different control variables, it is necessary to study how these variables affect the switching transient and quantify their effect on the switching speed. In this section, key indices that affect the performance are extracted from a mathematic model of the power devices. It should be noted that a linearized trajectory model is used in this paper to study the impact of different factors qualitatively.

a) Turn-on process

In Fig. 4, $t_1 - t_2$ is the turn-on delay. $t_2 - t_3$ is the I_{ds} rising time and $t_3 - t_4$ is the V_{ds} falling time. The *di/dt* and *dv/dt* can be approximately calculated by (1) and (2), respectively, [21] [32], [33]. The variables that may be used to control the slew rate are marked in red.

$$\frac{di}{dt}=\frac{I_{g\_t2\_t3}g_{fs}}{\left(C_{gd}+C_{gs}\right)}=\frac{\left(V_{dr\_on}-0.5V_{th}-0.5V_{miller}\right)g_{fs}}{\left(C_{gd}+C_{gs}\right)R_g+L_s g_{fs}} \tag{1}$$

$$\frac{dv}{dt}=\frac{I_{g\_t3\_t4}}{C_{gd}}=\frac{V_{dr\_on}-V_{miller}}{C_{gd}R_g+\left(C_d+C_L\right)/g_{fs}}, \tag{2}$$

where V_{miller} is the Miller plateau voltage, which is calculated as $V_{miller}=V_{th}+I_O/g_{fs}$ and g_{fs} is the transconductance. $I_{g\_t2\_t3}$ is the average gate current in the period $t_2 - t_3$ and $I_{g\_t3\_t4}$ is the average gate current in the period $t_3 - t_4$.

b) Turn-off process

In Fig. 4, $t_7 - t_8$ is the turn-off delay. $t_9 - t_{10}$ is the V_{ds} rising time and $t_{10} - t_{11}$ is the I_{ds} falling time. *dv/dt* and *di/dt* can be approximately calculated with (3)-(4) [32] [34].

$$\frac{dv}{dt}=\frac{I_{g\_t9\_t10}}{C_{gd}}=\frac{V_{miller}-V_{dr\_off}}{C_{gd}R_g+\left(C_{ds}+C_{gd}+C_d+C_L\right)/2g_{fs}} \tag{3}$$

$$\frac{di}{dt}=\frac{g_{fs}I_{g\_t10\_t11}}{C_{gd}+C_{gs}}=\frac{\left(0.5V_{miller}+0.5V_{th}-V_{dr\_off}\right)g_{fs}}{\left(C_{gd}+C_{gs}\right)R_g+L_s g_{fs}}, \tag{4}$$

$I_{g\_t9\_t10}$ is the average gate current in the period $t_9 - t_{10}$ and $I_{g\_t10\_t11}$ is the average gate current in the period $t_{10} - t_{11}$. The switching energy loss can be roughly evaluated with (5).

$$E_{on}=\frac{V_{bus}I_O^{\,2}}{2di/dt}+\frac{V_{bus}^{\,2}I_O}{2dv/dt} \tag{5}$$

TABLE I
THE SUMMARY OF THE SLEW RATE CONTROL VARIABLES

	Turn-on slew rate		Turn-off slew rate	
Variable	*dv/dt*	*di/dt*	*dv/dt*	*di/dt*
I_g↑	↑	↑	↑	↑
C_{gd}↑	↓	↓	↓	↓
C_{gs}↑	-	↓	-	↓
R_g↑	↓	↓	↓	↓
V_{dr_on}↑	↑	↑	-	-
V_{dr_off}↑	-	-	↓	↓

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In (5), V_{bus} is denoted by dc bus voltage and I_O is the load current. In (1)–(4), all the controllable variables are marked in red. It is evident to observe how these variables affect the slew rate. The deductions from the equations are concluded in Table I. It should be noted that I_g in Table I is the absolute value of the gate current. From Table I, decreasing I_g or increasing R_g can effectively reduce the slew rate while increasing C_{gd} can effectively reduce the slew rate [27][37]. This argument has been verified in [35] and [36].

C. EMI noise and other detrimental effects of high switching slew rate

The foremost application of AGD is to mitigate EMI noise. The mechanism how *dv/dt* impacts the EMI noise in the system should be analyzed in prior to designing the power converter. [38]-[40] demonstrate the mechanism of EMI noise caused by high *dv/dt* during the switching of power devices.

The analysis of a switching waveform, as shown in Fig. 5, should take the rising and falling edges into consideration. The duration of voltage rising/falling time t_{rv} and t_{fv} are critical for the noise spectrum because they determine the two corner frequencies f_{c2} and f_{c3} which are shown in Fig. 6. If the *dv/dt* during the turn on/off transient increases, t_{rv} or t_{fv} will reduce and the corner frequency f_{c2} or f_{c3} will increase. As a result, the EMI noise will rise which is depicted in Fig. 6.

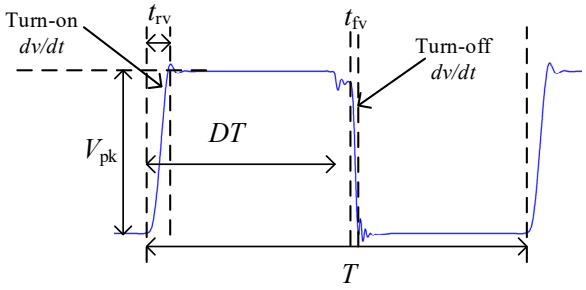


Fig. 5. A typical switching waveform with rising and falling edges.

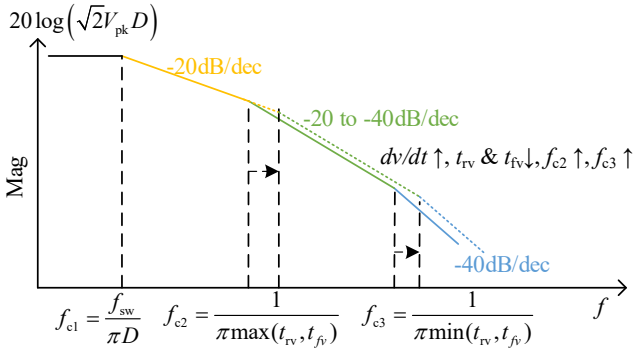
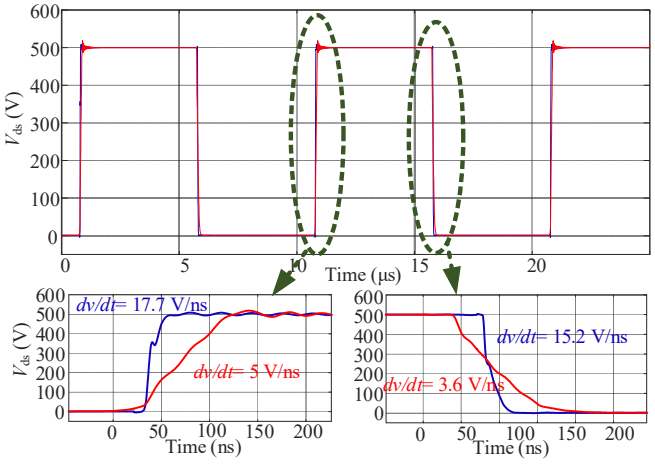
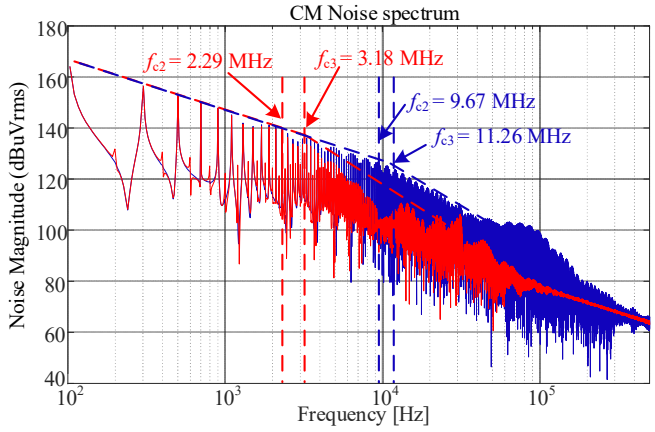


Fig. 6. Spectrums of pulse width modulation (PWM) waveforms with rising and falling edges.

Two switching waveforms with the same switching frequency f_{sw} and duty cycle D but different *dv/dt* slew rates (5V/ns increased to 50V/ns) are shown in Fig. 7 (a). *dv/dt* of turn on/off transient is assumed to be identical. The frequency domain spectrums of the waveforms are plotted in Fig. 7 (b). With a rising slew rate, the corner frequency f_{c2} increases and the spectrum magnitude increases correspondingly. More details of EMI noise model can be found in [114] and [115].



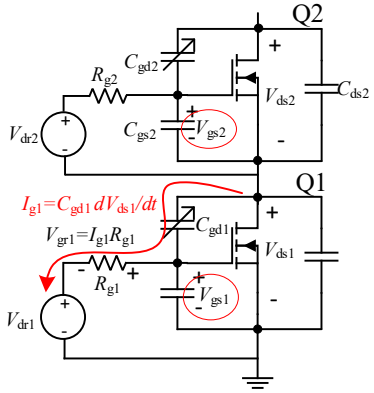
(a)



(b)

Fig. 7. The relationship between *dv/dt* and EMI noise. (a) The time domain voltage waveforms with different *dv/dt*. (b) The frequency domain spectrum of the voltage waveforms with different *dv/dt* slew rates.

Another problem of high slew rate is the rising risk of false triggering. One reason of false triggering is self-turn-on of the power switch. When the gate current flows back to the gate driver power supply, the voltage on gate resistor may cause a temporary V_{gs} rising. If this V_{gs} rising is higher than V_{th}, the power switch turns on falsely again and a shoot-through event may occur [14]. Another reason is crosstalk noise which can be explained via the propagation route in Fig. 8.



(a)

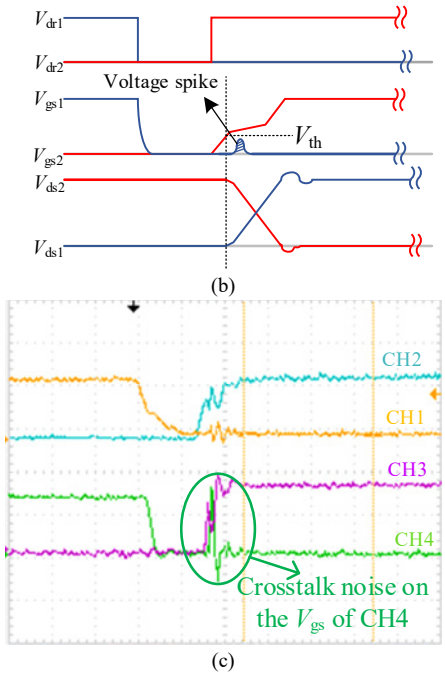


Fig. 8. Mechanism of crosstalk noise in a half-bridge. (a) The current route of crosstalk noise propagation. (b) The simplified waveform of crosstalk noise. (c) The experimental result of voltage spike on V_{gs} caused by crosstalk noise.

In Fig. 8 (a), when Q2 turns on, the slew rate of V_{ds1} triggers current across the C_{gd1} which can be denoted by $C_{gd1}V_{ds1}/dt$. When this current flows through gate resistor R_{g1}, a voltage spike $V_{gr1}=I_gR_{g1}$ is generated on the gate of Q1 [41]. An example of the crosstalk noise on a single-phase converter is captured in Fig. 8 (c). CH3 and CH4 represent V_{gs2} and V_{gs1} in a half-bridge respectively. When Q2, the *dv/dt* causes a voltage spike on the V_{gs} of CH4. For the worst case, if this voltage spike is higher than the gate threshold voltage of Q1, a shoot-through event will occur. It can be evaluated with (6) [113].

$$R_g C_{gd} \frac{dv}{dt} + V_{dr,off} < V_{th}, \tag{6}$$

where $V_{dr,off}$ is the normal turn-off driver voltage. In addition, high *di/dt* results in high overshoot voltage which may damage the device. The overshoot voltage is caused by voltage on the parasitic inductance on drain and source. The maximum drain-source voltage V_{ds_max} can be calculated with (7).

$$V_{ds\_max} = V_{bus} + (L_d + L_s)\frac{di}{dt} < V_{ds\_rating} \tag{7}$$

V_{bus} is denoted by dc bus voltage and V_{ds_rating} is the rated V_{ds} of the power device. From (7), it is evident that the maximum V_{ds} increases with *di/dt*. V_{ds_max} should be lower than V_{ds_rating} to prevent the break down of the power device.

III. Various Methodologies of AGD

The aforementioned analyses demonstrate several factors that may be utilized to control the slew rate. Based on the analyses results, in this section, various state-of-the-art AGD methods based on these factors will be introduced.

A. Variable gate resistance method

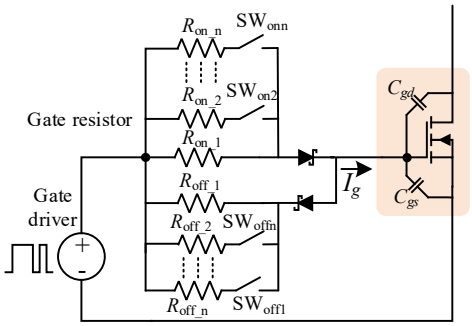


Fig. 9. A typical circuitry of variable gate resistance method.

Variable gate resistance method is the most widely used approach for slew rate control. Its attractive features, such as low cost and easy implementation, make it feasible for the EMI mitigation in some industrial applications [42]. Its working principle is straightforward [43]. Via adjusting gate resistance for different stages in a switching transient, *dv/dt* and *di/dt* can be changed. Its basic circuitry can be depicted in Fig. 9. Through controlling the switches SW_{on2} - SW_{onn} and SW_{off2} - SW_{offn}, the value of gate resistors connected in the gate loop can be changed, thus the total gate resistance is adjusted [44].

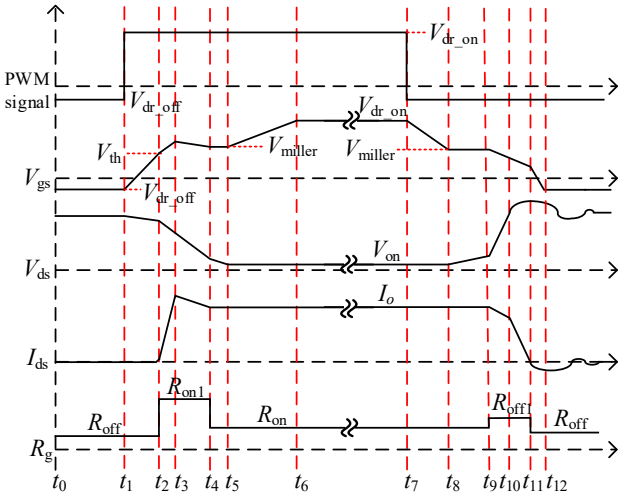


Fig. 10. The switching waveforms of a variable gate resistance AGD.

The switching waveforms of a typical variable gate resistance method are plotted in Fig. 10 [45]. Generally, high gate resistance, i.e., R_{on1} and R_{off1} in Fig. 10, is utilized during the Miller plateau period to suppress slew rate and low gate resistance is employed before/after the Miller plateau to reduce the false-triggering risk. It should be noted that the method in Fig. 9 requires additional gate resistors and BJTs to provide more adjustable steps [46]. Furthermore, if the gate charge of the power module is high, the footprint of the gate resistors should also be large to dissipate the driver loss. Therefore, a variable gate resistance AGD can hardly provide high adjustment resolution for slew rate owing to the PCB size limitation. Various AGD circuits based on this methodology have been proposed in [44]-[47].

A simple variable gate resistance AGD circuit, as shown in Fig. 11, is proposed in [46]. Three totem-pole driver ICs, i.e.,

Buffer1-3, are connected in parallel to control the gate resistance dynamically. The three turn-on/off resistors have different resistances. The driver ICs should select the ones with independent gate current source pins and sink pins such as Infineon® 1EDN751. Via controlling the conduction of the buffers in different stages of switching process, the gate resistance can be adjusted. Another state-of-art variable gate resistance AGD method is proposed in [48-50]. An optic diode is adopted to replace the conventional physical gate resistor. Through tuning the illumination to the optic diode, the conduction resistance of the diode can be changed and the switching slew rate can be controlled.

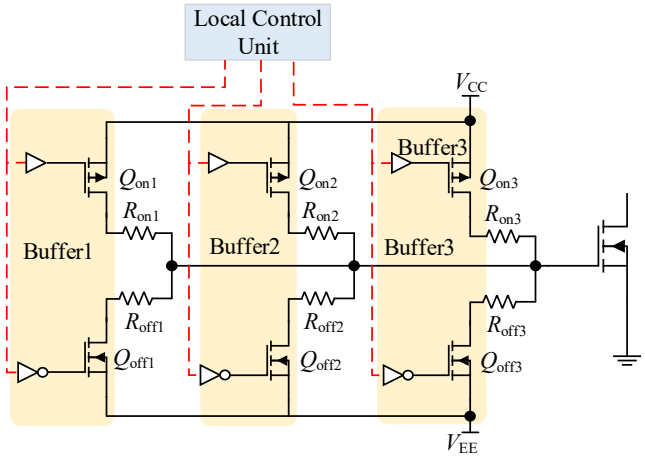


Fig. 11. The variable gate resistance AGD proposed in [46].

B. *Variable input capacitance method*

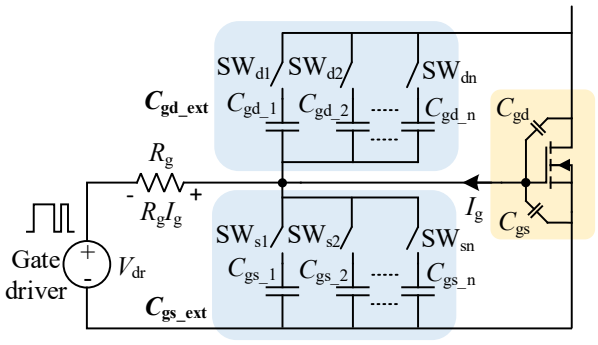


Fig. 12. Different variable input capacitance methods.

The variable input capacitance method regulates C_{iss} to control the switching slew rate as depicted in Fig. 12. In brief, via controlling the switches SW_{s1}/SW_{d1}-SW_{sn}/SW_{dn}, total capacitance of C_{gd_ext} and C_{gd_ext} which are connected in parallel with MOSFET capacitance C_{gd} and C_{gs} can be changed. Consequently, the gate input capacitance charging/discharging speed can be adjusted under different total capacitance values. The effectiveness of this type of method has been validated in [27] and [51]. However, this is a non-preferable solution due to its intrinsic defects.

Adding a capacitor C_{gs_ext} is a common solution to gate loop oscillation damping and switching transient slowing down [14]. However, since the charging time of C_{gs}+C_{gs_ext} increases dramatically, this method inevitably increases the turn-on/off delay time. Also, since peak gate current equals to $(C_{gs}+C_{gs\_ext})dV_{gs}/dt$, a large C_{gs_ext} can probably increase the peak gate current thus increase the false triggering risk reversely. Therefore, a very large C_{gs_ext} is not recommended. Apart from C_{gs_ext}, C_{gd_ext} can be another potential solution for the switching speed adjustment. Nonetheless, this is not common because C_{gd_ext} should choose a capacitor which has higher voltage rating than the V_{ds} of the device. Also, during Miller plateau of turn-off process, the gate current can be expressed with $I_g = (C_{gd}+C_{gd\_ext})dV_{ds}/dt$. Therefore, a high C_{gd_ext} increases the voltage drop on V_{gs} during turn-off. Therefore, from Eq. (6), this may not reduce the self-turn-on risk.

C. *Variable gate current method*

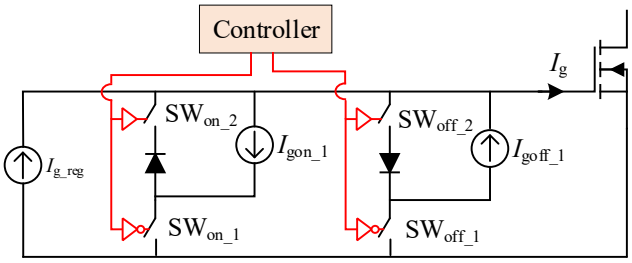


Fig. 13. The working principal of an active current source gate driver.

Variable gate current method usually utilizes a current source to change the gate current. In other words, the power device switching speed can be controlled by means of adjusting the gate current which charges/discharges C_{iss}.

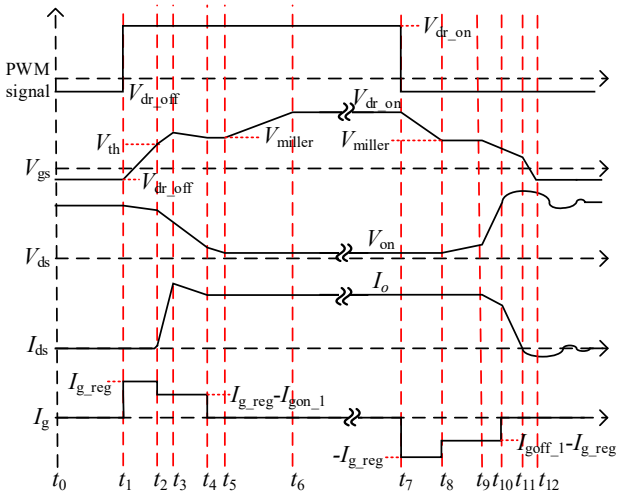


Fig. 14. The waveform of the variable gate current method AGD.

Its functionality in regard of the switching slew rate control has been validated in [35], [52]-[55]. The working principle of a variable gate current method is depicted in Fig. 13 [52]. SW_{on_1} and SW_{on_2} are complementary switches for turn-on slew rate control while SW_{off_1} and SW_{off_2} are complementary switches for turn-off. I_{g_reg} is the nominal gate current from the current source gate driver. There are two additional current sources I_{gon_1} and I_{goff_1} adjusting the gate current during the switching transient. The waveform of the latter condition is given in Fig. 14.

From Fig. 14, the gate current of AGD is I_{g_reg} for turn-on/off delay. During the Miller plateau, SW_{on_1} is on and SW_{on_2} is off. The current source I_{gon_1} will bypass a part of gate current. I_g reduces from I_{g_reg} to I_{g_reg}–I_{gon_1} and the turn-on is slowed down. The turn-off process is similar. If the switching speed is desired to be accelerated, more gate current can be injected into C_{iss} during the Miller plateau period.

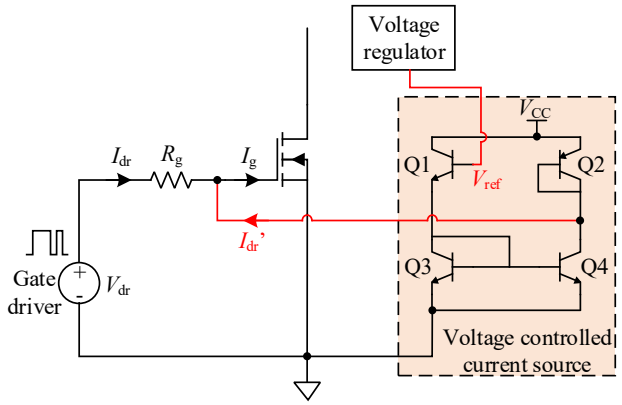


Fig. 15. The proposed circuit of variable gate current AGD in [53].

A current mirror circuit is an accessible option to realize a voltage controlled current source. [53] and [54] adopt current mirror circuits to extract the gate current during the switching transient. The circuit schematics is plotted in Fig. 15. The output current of a current mirror circuit, which incorporates BJTs Q1-Q4, can be controlled via changing the reference voltage V_{ref}. A digital-analog converter (DAC) with an local controller such as an FPGA or CPLD chip can be employed to adjust V_{ref}.

Several circuitries of current source gate drivers with inductors which can store the gate charge are introduced in [56] and [57]. The proposed resonant current source gate driver can effectively reduce the power loss caused by drivers [58]. Indeed, current source gate drivers are more complex than voltage source gate drivers. Nonetheless, they have a merit with respect to higher power efficiency since it can eliminate the power loss dissipated on the gate resistor [56]. [55] also claims that a current source gate driver can reduce the turn-on loss of an IGBT at similar dv_{CE}/dt compared to a voltage source gate driver. There are several available current source gate drivers on the market already, such as the Infineon® 1EDS20I12 gate driver.

D. Variable gate voltage method

The variable gate voltage method can adjust the gate voltage during the switching transient to control its trajectory. It attracts attention since its working principle is pertinent to the conventional gate drive methods [59]. The advantage of this method over the variable resistance method is its flexibility since an adjustable voltage regulator is always easier to be implemented. Additionally, considering that a prevailing shoot-through protection method is using multi-level turn-off to reduce the overshoot voltage when desaturation signal is detected, this AGD method is more convenient to provide the protection without sophisticated additional circuitries [60], [61]. Different topologies of the variable gate voltage AGD methods are proposed in [20] [24] [32] [34] [59-65].

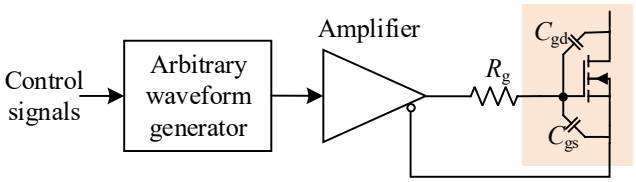


Fig. 16. The simplified block diagram of a variable gate voltage AGD.

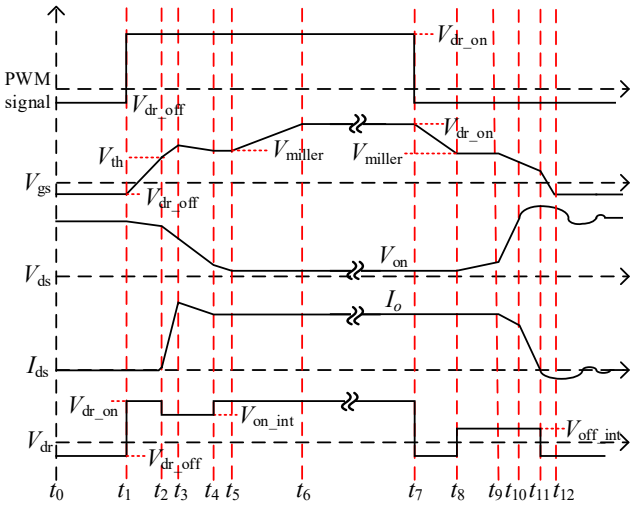


Fig. 17. The waveforms of a typical variable gate voltage method AGD.

The block diagram of the variable gate voltage AGD can be explained in Fig. 16. In general, the gate driver can be equivalent to a controlled voltage source. The desired driver voltage profile is first generated by an arbitrary waveform generator under the control of the AGD local controller and then amplified by an amplifier stage. Its working principle can be explained with Fig. 17 which shows the waveforms of a multi-level gate voltage profile. During the Miller plateau stage of the switching transient, the driver voltage are adjusted to a certain value, i.e., intermediate voltage, to regulate the switching speed to a desired level. After the switching ends, the driver voltage recovers to the normal turn on/off voltage.

In order to generate the waveforms in Fig. 17, an AGD circuit is proposed in [34] and [64]. An adjustable voltage regulator consists of a DAC which controls the intermediate voltage level one switching cycle in advance and a voltage amplifier which provides enough power to drive the power MOSFET. Then three cascaded-connected totem-pole driver buffers operates to generate the multi-level driver voltage profile in Fig. 17. To further optimize the switching slew rate, an S-shape slew rate control profile for the power devices is proposed in [20]. However, the circuitry that generates S-shape profile is complex or expensive. Another method, which is introduced in [59] and [65], can realize the same goal through changing the potential of MOSFET source to change V_{gs}.

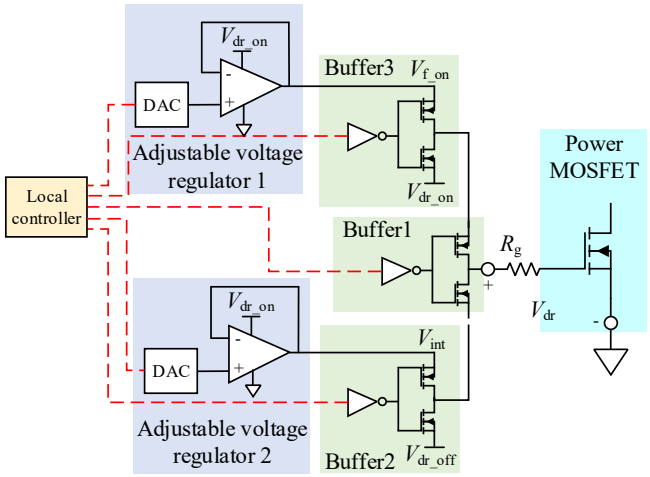


Fig. 18. A circuit of variable gate driver voltage AGD [34].

IV. Control Strategies for AGDs

The dominant challenge of AGD control strategies implementation is the short duration of each switching transient which is usually nanosecond (ns) level. For the sake of various optimization targets, there are several potential control variables: the switching slew rate, the junction temperature T_j, EMI noise, and duration of each sub-stage. The selection of the control variables is usually based on the requirements of a particular application.

A. Open-loop control

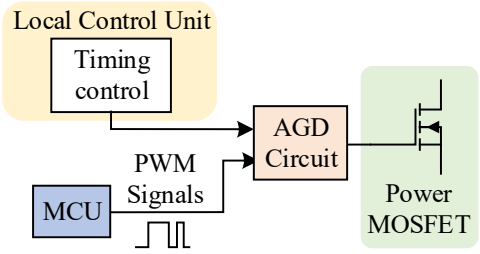


Fig. 19. A block diagram of the open-loop control.

The block diagram for a typical open-loop control is shown in Fig. 19. The main control unit (MCU) generates the PWM gate signals. A same driver voltage profile is usually applied to all scenarios. For instance, for the variable gate resistance method, the gate resistance and duration remain constant even though the operation condition changes. The open-loop method is simple and cost-friendly since no sensor for feedback signals is required [25].

A commercially available product is demonstrated in [66]. However, as analyzed in Section II, the performance indicators such as the EMI noise and power loss may be different under different operation conditions such as load current and bus voltage. Particularly, even for a same power device, the performance indicators such as the *dv/dt*, *di/dt*, and the energy losses may be different when the device is degraded [67][68]. Therefore, the open-loop method can hardly ensure that the power device always operate at the optimal condition. Much effort is dedicated into the development of open-loop AGDs. [44] and [45] introduce the variable gate resistance AGD with open-loop control strategy, while [64] introduces the variable gate voltage AGD with open-loop strategy.

B. Measurement-based control

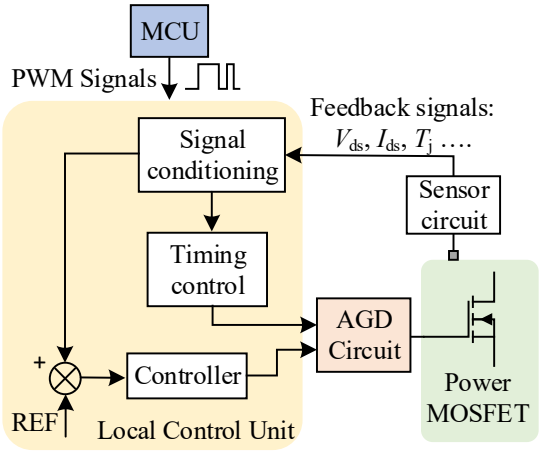


Fig. 20. A block diagram of the measurement-based control.

A block diagram of the measurement-based control is given in Fig. 20. The AGD has sensor circuits for detecting the feedback signals such as *dv/dt*, *di/dt*, energy losses, T_j etc. which will be sent to a signal conditioning circuit. A local control unit controls the output of the AGD and ensures the feedback signals track their references. A timing control circuit is used to ensure the AGD acts at the correct time point. The error between the reference and feedback signal is compensated by a controller. The timing signals and controller output will be sent to the AGD circuit to control the switching of the power devices.

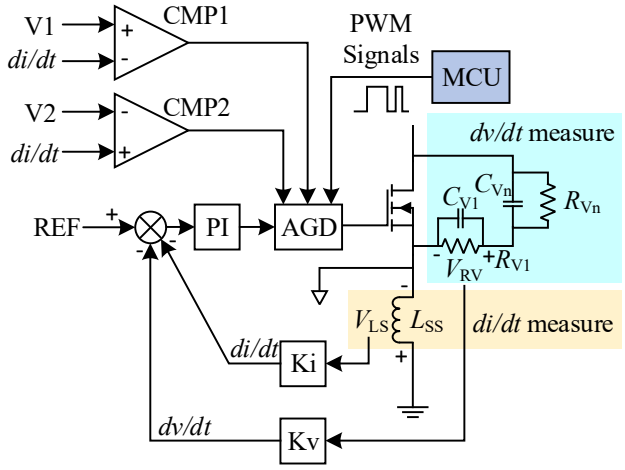


Fig. 21. The block diagram of a typical measurement base control AGD.

Since the switching process is rapid (typically nanosecond level), the slew rate feedback is hard to implement [25]. A straightforward *dv/dt* measuring method is sensing the IGBT collector- emitter voltage V_{ce} and calculating the slew rate with a digital controller [25]. In [69], *dv/dt* is sensed directly with the voltage divider circuit with a high bandwidth op-amp OPA847. The direct slew rate feedback method works well for the IGBTs

whose switching transient is longer than 1 μs [25]. The WBG devices requires very high-bandwidth sensors and analog-to-digital converters which are costly. Therefore, in [35], *dv/dt* is measured through sensing the current across capacitors which are connected between source/gate and drain. *di/dt* indicates the overshoot voltage on V_{ce} or V_{ds}. Accordingly, the *di/dt* can be measured through sensing the voltage drop on the stray inductance, which has been validated in [25] [60] [62] [70-72].

An example of a control block diagram with *dv/dt* and *di/dt* feedback is shown in Fig. 21. *di/dt* is measured through sensing the voltage on the inductance L_{ss}. *dv/dt* measurement is conducted with RC networks (R_V and C_V) since the current that flows through C_V is proportional to the *dv/dt*. The RC networks are connected in series to reduce the total parasitic inductance and increase the maximum voltage. The slew rate signals are feedback and compared with the reference signals. An analog proportional integral (PI) controller is utilized to compensate the steady-state error. Considering that the bandwidth of PI controller is determined by the opamp, it is necessary to select some high bandwidth opamps for SiC devices. Also, two threshold voltage levels V1 and V2 are used to compared with slew rate feedback signals. The outputs of comparator CMP1 and 2 indicate the start point of power MOSFET switching, thus they are utilized as the timing signals to trigger the AGD at correct time. The ultra-fast comparators with low propagation delay such as MAX9601 and ADCMP551 are recommended for WBG device.

An optimal control strategy to compensate the thermal stress on the parallel-connected switches is introduced in [73]. T_j of the two switches are measured and the switching delay time is controlled correspondingly. [53] and [74] utilize the on-state V_{ds} of MOSFETs as the feedback signals to balance the voltage on the series-connected power devices. Once the slew rate feedback is sent to the local control unit, the optimal switching speed will be calculated with the given reference signals. A comparator can be employed to limit the slew rate to a certain level. When the slew rate is higher than this threshold, the AGD will intervene to slow down the switching. This control strategy has been presented in [39]. [25] and [62] used analog PI controllers to track the slew rate reference signals. Thanks to the advancement of digital processors, the high-speed processors such as FPGA or CPLD can be applied to AGDs which are reported in [54] and [75].

C. Estimation-Based Control

When the slew rate is higher than the bandwidth of the sensors, the direct measurement is no longer possible. Moreover, junction temperature measurement is arduous if the power module does not include thermal sensors inside. To solve this problem, the feedback indices can be estimated with the mathematic model which can accurately characterize the switching trajectory or thermal curve [118].

A switching trajectory model of power devices can derive the switching performance of a power device with other accessible feedback signals. For example, instead of measuring the slew rate directly, a datasheet-driven trajectory model as well as the parasitics of the circuit, load current, and bus voltage are adopted to predict *dv/dt* and *di/dt* in [32]. Since the MOSFET parameters, load current, and bus voltage of a PWM converter can be assumed to be constant in a switching cycle, no ultra-fast sensor is required to detect the slew rate.

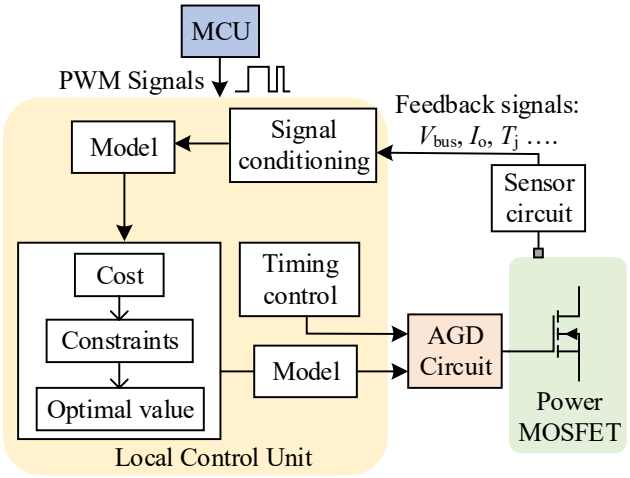


Fig. 22. A block diagram of the model-based indirect control.

Fig. 22 describes the control scheme of an estimation-based control strategy of the AGD. The AGD receives feedback signals such as dc bus voltage V_{bus}, load current I_{ds} etc. The local control unit reads feedback signals and calculates the performance indicators with the trajectory model. An example is given in [34]. The prediction of slew rate and energy loss is performed with the feedback of dc bus voltage and load current. A cost function in regard of the intermediate driver voltage considers the tradeoff of EMI noise against power loss. Once the voltage with the lowest cost is selected for next switching cycle, the timing sequence of this driver voltage can be determined with the trajectory model. Compared with the offline-tuned AGD, the adaptive method can reduce the EMI noises and energy losses of the power device.

Similarly, if junction temperature is the the feedback signal, thermo-sensitive electrical parameters (TSEP), such as peak gate current, gate charge, or turn-off delay time, can be fedback to estimate the junction temperature [116]. Miscellaneous TSEP detection circuits can be found in [117]. The drawback of TSEP method is the necessity of a data-driven thermal model of a specific SiC devices. To the best knowlege of the authors, AGD with TSEP function has not been reported, yet it is a potential and interesting solution for the thermal management of a power convertion system.

The performance of this method highly depends on the accuracy of the behavior model. However, in the real world, parasitics are not always constant during the switching and some parameters are difficult to measure. Also, the switching behavior can change dramatically due several factors such as T_j and humidity [76]. An on-line model-based control increases the computation load of the controller of the gate driver. Therefore, this method still need to be matured for real world applications.

D. Timing Strategy

As mentioned in Section II, it is necessary to adjust the AGDs output in every sub-stage of a switching process. Specifically, R_g, I_g and/or V_{gs} are adjusted during the Miller plateau. After the switching transient ends, the output AGD should be clamped at the normal turn-on or turn-off mode. Therefore, it is critical to have correct timing control. Missing the proper time instant may result in failure of switching or extended switching duration. Generally, the existing timing control approaches can be categorized into two types, i.e., feedback-based strategy and timer-based strategy. The feedback-based strategy needs certain external feedback circuits to trigger the AGD at the start of each sub-stage of the switching transient. A timer-based strategy needs a timer to count the duration of each sub-stage and control the AGD to adjust the output correspondingly.

Several typical feedback-based strategies are demonstrated in [45]. The key point of the proposed method in [45] is high-speed comparator. The V_{gs} is sensed and input to the comparator. During turn-on process, when V_{gs} increases to a level higher than gate-source threshold voltage, the power device starts conducting and the AGD changes the output control variables. It can be depicted in Fig. 21 and Fig. 22. Several typical timer-based strategies are introduced in [52] and [54].

Based on the introduction above, various state-of-the-art AGD methodologies as well as the control strategies are compared and summarized in Fig. 23. The advantages and disadvantages of various strategies are listed in Table II. It should be noted that every methodology has its own cons and pros which make it appropriate for some certain application scenarios. In general, the variable gate resistance method is relatively simple to implement and the cost-efficient while it is unsuitable Therefore, it is preferred in some scenarios when cost-reduction dominates the design consideration. The variable gate voltage method can provide high adjustment resolution and it is very similar to the desaturation protection. Thus, this method is appropriate for case when the system

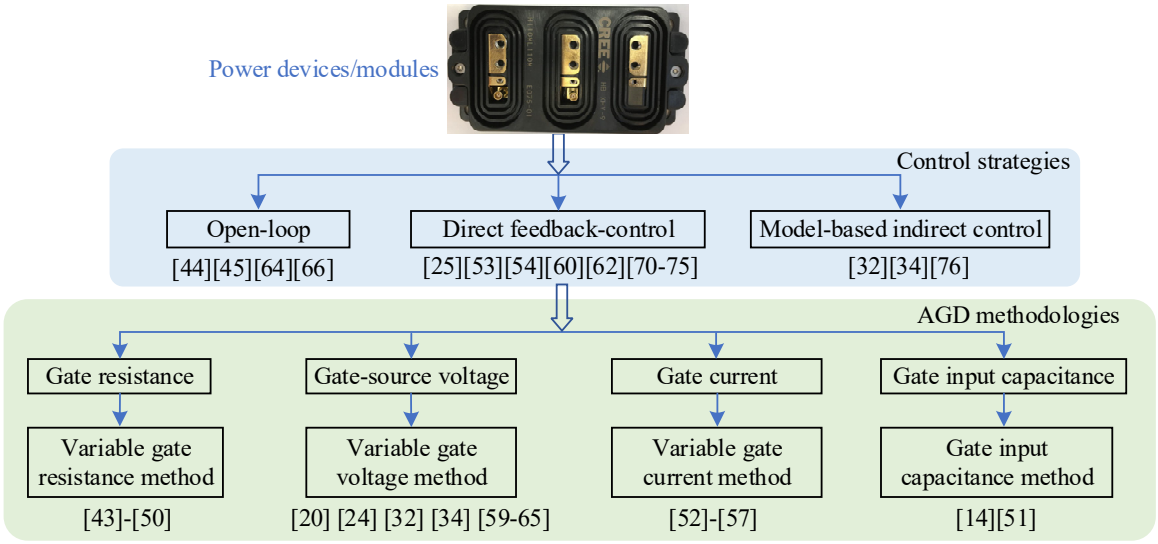


Fig. 23. A summary of the state-of-the-art AGD methodologies.

TABLE II
THE COMPARISON OF VARIOUS AGD METHODOLOGIES AND CONTROL.

	Advantages	Disadvantages	References
Variable gate resistance method	Low cost and easy implementation. Simple circuitry.	Requires additional gate resistors and BJTs to provide more adjustable steps. Hard to realize high adjustable resolution for driving speed.	[43]-[50]
Variable gate voltage method	Straightforward working principle. High adjustment resolution. Easy to provide soft turn-off for short circuit protection.	Complex circuitry and control.	[20], [24], [32], [34], [59]-[65]
Variable gate current method	Good gate loop oscillation suppression effect.	Complex circuitry and control.	[52]-[57]
Variable input capacitance method	Simple circuitry and low cost.	Increasing switching delay time. External C_{gd} requires high voltage rating.	[14], [51]
Open-loop control	Simple and low cost	Lack of flexibility. Cannot achieve the optimal performance of WBG devices.	[44], [45], [64], [66]
Direct feedback control	Straightforward control design.	Requires high speed sensors for slew rate measurement which are not economy friendly.	[25], [53], [54], [60], [62], [70]-[75]
Model-Based Indirect Control	Prevent using high speed sensors which reduces cost.	An accurate model of the circuit and the devices is required. High computation load of controller.	[32], [34], [76]

reliability has high priority. The variable gate current method is generally based on a current source gate driver. A conventional current source gate driver utilizes a resonant driver topology which can reduce driver loss. It has superior gate oscillation suppression effect and efficiency, but it is complex and expensive generally. All of these features make it suitable for the case that cost is not the top priority consideration. It should be noted that the difficulty of implementation is determined by the specific employed circuitries. In conclusion, the major challenge of the AGD development is still the feedback control design. Most commercialized products do not provide feedback control and adaptive timing strategy. Therefore, based on the insight of the future trend, exploring novel AGD circuits with feedback control for WBG devices is a thrust of this research.

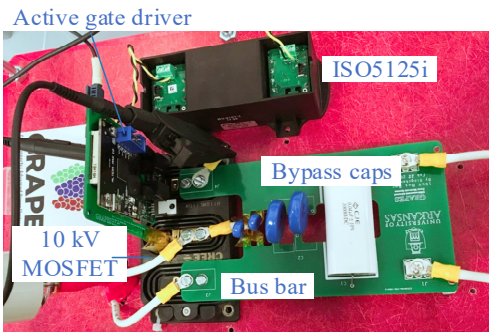
V. Conventional and Emerging Applications of AGDs

Most existing applications for AGD aim at mitigating the side effects of high switching slew rate such as EMI noise. Also, the AGDs have potentials to be applied in the following scenarios: reliability enhancement of power device, current balance of paralleled devices, and voltage balance of series connected devices. The following sections will discuss these application scenarios one by one.

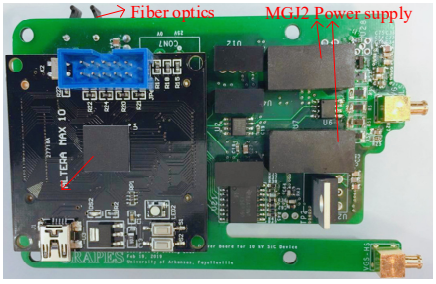
A. The conventional applications

In some cases, the switching slew rate is high while the system is vulnerable to EMI noise. For instance, the solid-state transformer with high voltage (≥10 kV) SiC power devices is an emerging technology for the distributed system [77][78]. As reported in [79], the slew rate of *dv/dt* can be even higher than 70 V/ns. This may affect the robustness of system operation. It is desired to actively adjust the slew rate to balance the EMI noise and energy loss.

A high gate resistance or external C_{gs} can reduce the slew rate, but it may dramatically increase the dead-time and affect the control of the dual active bridge converter. Therefore, in this situation, an AGD can be employed to dynamically adjust the slew rate in regard of the specific switching situations. An DPT testbed with a 10 kV SiC MOSFET module and a variable gate voltage AGD is shown in Fig. 24. The schematics of the AGD circuit can be referred to [34]. The parameters of DPT setup are listed in Table III.



(a)



(b)

Fig. 24. The experimental setup of 10 kV SiC MOSFET DPT. (a) The testbed. (b) The designed variable gate voltage AGD board.

TABLE III
THE PARAMETERS OF THE DPT EXPERIMENTAL SETUP.

Parameter	Value
DC bus voltage	4 kV
Maximum load current	20 A
Load inductor	6 mH (1.2*5)
Oscilloscope	MDO4104 (2 GHz)
V_{ds} probe	Tektronix P6015A
I_{ds} probe	PEM CWT mini
V_{gs} probe	Tektronix TPP0500
Device under test	CREE XPM3 10 kV SiC module

TABLE IV
THE INDICES OF 10 KV SIC MOSFET DPT RESULTS WITH AGD.

V_{off_int}	*dv/dt* (V/ns)	*di/dt*(A/ns)	Turn-off energy losses
Conventional (-5 V)	94.78	0.34	2302 μJ
5 V	58.8	0.158	4384 μJ
5.6 V	54.32	0.145	4629 μJ
6.3 V	52.4	0.138	4977 μJ
6.9 V	49.16	0.122	5555 μJ
7.5 V	43.56	0.109	6259 μJ
8.1 V	40.37	0.097	7410 μJ

A 300 MHz Altera 10M08SAU169C8G FPGA chip is used as the local control unit. A DSP controller is the MCU which generates the double pulse gate signals and a Broadcom AFBR1624 fiber optical transceiver is used to isolate the gate signals. The power supply is Power Integration ISO5125i which provides 18 kV galvanic isolation. Two Murata MGJ2 power supply modules are tied with the ISO5125i to provide bipolar voltage (20V/-5V) for the gate driver.

The driver voltage profile is similar with the waveforms in Fig. 17. Fig. 25 (a) shows the turn-off waveforms of the DPT under different turn-off intermediate voltage, i.e., V_{off_int} in Fig. 17. All indices of Fig. 25 (a) are extracted in Table IV.

From Fig. 25 (a) and Table IV, it is evident that with higher intermediate voltage, the slew rate is reduced while the turn-off delay time is not influenced. Fig. 25 (b) compares the spectrum analysis plot with a conventional gate driver, AGD with V_{int}=5V and 8.1V. From Fig. 25 (b), the high-frequency harmonics of conventional gate driver is the highest among the three curves while AGD with V_{int} =8.1V is the lowest. Therefore, AGD can actively adjust the slew rate of 10 kV SiC power devices switching, thus suppress high EMI noise in the system.

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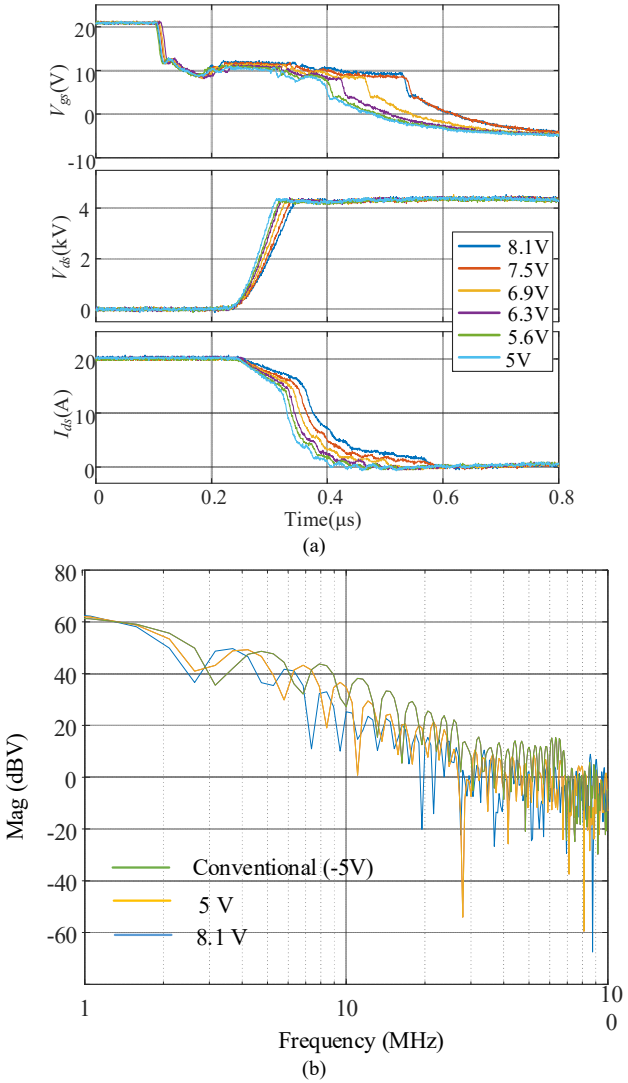


Fig. 25. DPT results of 10 kV SiC MOSFET with a variable gate voltage AGD. (a) The turn-off process waveform. (b) The frequency spectrum of the switching waveform with AGD.

Another application is motor drive. Bearing current caused by common mode current is detrimental to the motor and high switching slew rate of the power devices will deteriorate this condition [80]. AGD can be applied to alleviate this issue. Due to the multiple degrees of freedom, the current/voltage behavior, thermal performance, and lifespan can be actively controlled with AGDs.

B. The reliability enhancement of semiconductor devices

The reliability of semiconductor devices is critical to the power electronics systems. High thermal stress is one of the major reasons of the power devices failure [81]. The repetition of thermal cycles may lead to the fatigue of solder joints due to different thermal expansion coefficients of copper and ceramic materials of the substrate [82]. The classic lifetime model of power modules can be evaluated with (8) [83].

$$N_{\mathrm{f}} = a \cdot \Delta T^{-\alpha} \cdot e^{\frac{E_{\mathrm{a}}}{k_{\mathrm{B}} T_{\mathrm{j,m}}}}, \tag{8}$$

where N_{f} is the number of cycles to failure, ΔT is the amplitude of thermal fluctuation, k_{B} is the Boltzmann constant and $T_{\mathrm{j,m}}$ is the average junction temperature. Other parameters are the fitting results of the reliability experimental results. From (8), the lifetime of the power device is affected by the ΔT and $T_{\mathrm{j,m}}$. Therefore, the reliability of power devices can be improved by reducing both of them [84].

Active temperature control (ATC) can be utilized to regulate the loss and junction temperature of power devices [85]. The principle is adjusting T_{j} actively via controlling the energy loss of the power switches. The existing ATC methods can be divided into three categories: system level [86-87], modulation level [88-90], and gate driver level [91-93]. System-level ATC is usually applied to parallel-connected converters through controlling the loss distribution[86]. A modified modulation algorithms can also regulate the loss of different devices in one power converter. Nevertheless, the coupling between the energy loss on different devices may hinder ATC strategy being functional [88][89]. The adaptive switching frequency based on the T_{j} of power devices can be employed to prevent overheating [90]. It should be noted that this method cannot control the T_{j} of a specific single device independently and it may sacrifice the converter performance.

Compared with the two aforementioned methods, the AGD is more straightforward and efficient. [84] has validated that the turn-off driver voltage profile impacts on the reliability of the power devices. For this reason, the driver voltage can be regulated to control the switching and conduction loss and consequently the thermal cycling can be decreased [91]. An AGD which operates to counteract variations of the MOSFET on-state resistance based on the temperature feedback is proposed in [92]. A three-level AGD with controllable on-time is introduced in [93] to suppress the thermal cycling amount of a GaN-based dc/dc converter. Via controlling the duration of the intermediate gate voltage, the switching loss as well as the thermal fluctuation can be effectively regulated. It should be noted that all the AGDs methodologies introduced in Section III can be potentially employed to enhance the system reliability.

C. Parallel connection of power devices

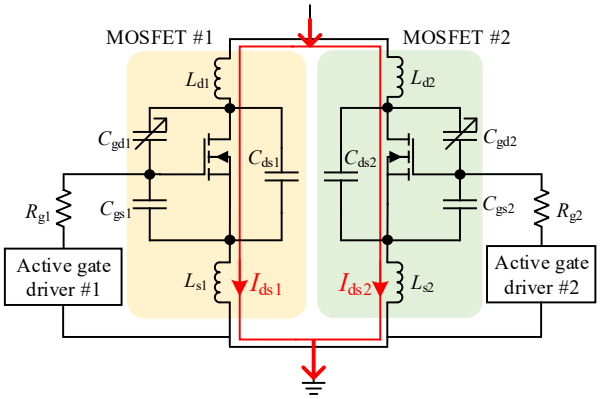


Fig. 26. The application of AGDs on parallel connected power devices.

Parallel connection of power devices, as shown in Fig. 26, is regularly used in the industry to boost the current rating of the power converters. Tesla Model S and Roadster have 2×14 parallel connected discrete IGBTs in TO-247 package for the

on-board charger and motor drive [94]. Compared with a single power device with high current rating, parallel connected devices are relatively affordable and can reduce the total power loss [95]. Additionally, hybrid power devices such as SiC MOSFET + Si IGBT are now emerging as technologies to make use of the advantages of both types of devices [73].

The thermal imbalance caused by the current imbalance is the major issue for paralleling power devices. The device suffering from higher current stress may be damaged first. The reasons leading to the current imbalance are diverse. The discrepancies of power devices electrical parameters such as the gate threshold voltage V_{th}, on-state resistance R_{ds_on}, and parasitic stray inductance are the major reasons [96]. The discrepancy of the gate driver of each device and the unequal parasitics in the power/gate loop caused by undesired PCB layout may also aggravate the current imbalance.

Even though the PCB parasitics are distributed averagely on each device, some thermo-sensitive parameters of the power devices such as V_{th} and R_{ds_on} may still intensify the current mismatching [97]. For instance, V_{th} decreases with the increasing junction temperature for most power devices, which aggregates the thermal imbalance. The forward voltage of most IGBTs shows negative temperature coefficient, so the higher temperature one shares more current stress and this feature increases its junction temperature in return. Addressing the problems above from the driver side is a favorable engineering solution since no modification needed in the power loop.

AGD is an effective method to compensate the current unbalance. A conventional method is adjusting the delay of the gate signal [96], [98], [99]. However, the delay of gate signal cannot compensate the unequal current completely in some cases. The gate signal delay and gate drive voltage are controlled in the AGD proposed in [100] to compensate the differences of turn on/off delay and slew rate of current respectively for Si IGBT. However, the active control of gate voltages of paralleled SiC MOSFETS has not been explored in previous work. DPT experimental study are conducted to validate current balancing function of variable gate voltage. The bus voltage is 400 V and total load current is 25 A. Two Wolfspeed C3M0065090D SiC MOSFETs are connected in parallel to be tested. High side is a C4D40120D SiC diode. The AGDs have multi-level turn-on voltage profile and their schematics can be found in [34]. The gate resistances of these two AGDs are both 5 Ω. The DPT experimental results are shown in Fig. 27 and the key indices of the results are listed in Table V. The right two subplots of Fig. 27 show the details of the zoom-in area of the left subplots. In Fig. 27 (a), the switching transient of the two devices is not synchronous without current balancing. Device #2 has higher slew rate than Device #1. Therefore, the energy loss of the Device #2 is higher than Device #1. To balance the transient I_{ds} of the two devices, the intermediate driver voltage levels of the two devices , i.e., V_{on_int} in Fig. 17, are changed. The Device #2 reduces to 18V while Device #1 remains at 20V. Fig. 27 (b) shows the

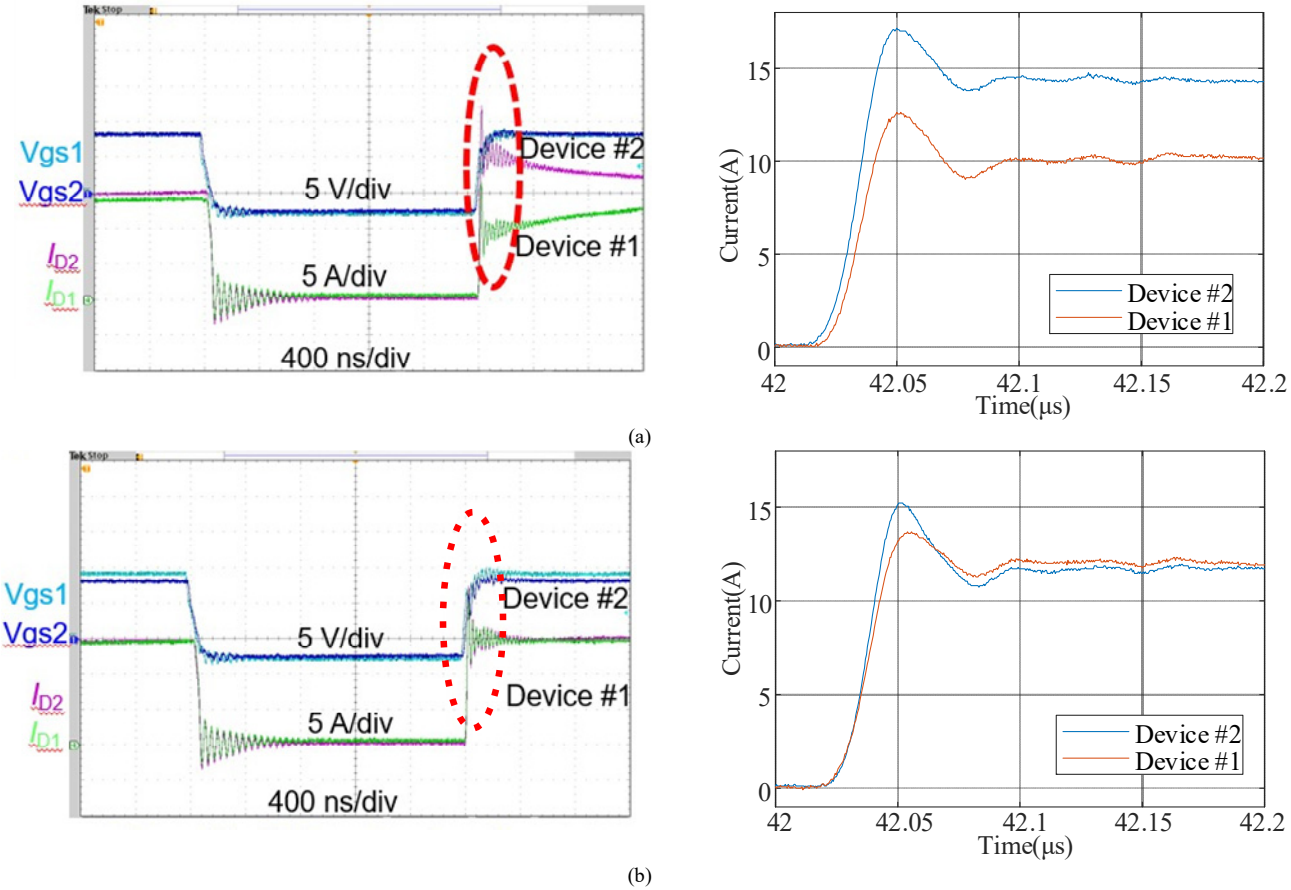


Fig. 27. Experimental results of parallel-connected device with variable gate voltage AGD. (a) Without AGD. (b) With AGD.

experimental results after current balancing with AGDs are functioning. From Fig. 27 (b), the turn-on transient current is balanced and the total energy loss is now distributed averagely on the two devices.

TABLE V
THE INDICES OF THE DPT RESULTS FOR PARALLEL-CONNECTED DEVICES.

Parameters	Without current balance		With current balance	
	Device #1	Device #2	Device #1	Device #2
Eon	78.5 μJ	55.1 μJ	61.2 μJ	62 μJ
***dv/dt* (on)**	8.9 V/ns	8.9 V/ns	8.5 V/ns	8.5 V/ns
***di/dt* (off)**	0.50 A/ns	0.61 A/ns	0.53 A/ns	0.6 A/ns

D. *Series connection of devices*

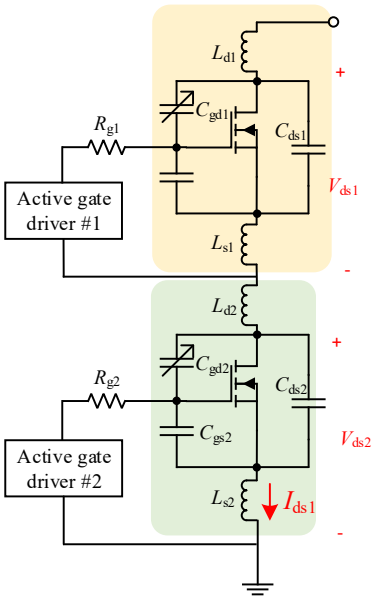


Fig. 28. The application of AGD on the series connected power devices.

Thanks to the advancement of SiC technologies, the voltage rating of power semiconductor devices increases to the level higher than 10 kV which enables power electronics converter be extensively applied in the power grid. In high voltage systems such as distributed grid, power devices are often connected in series to increase the total voltage rating, as shown in Fig. 28. Nevertheless, in some conditions, the voltage may not disperse evenly on each device for the sake of the mismatched gate drivers and the discrepancy of the electrical parameters of the devices and PCBs which has been analyzed in [53] and [101]. Especially, the dynamic voltage imbalance is difficult to eliminate due to the short switching time.

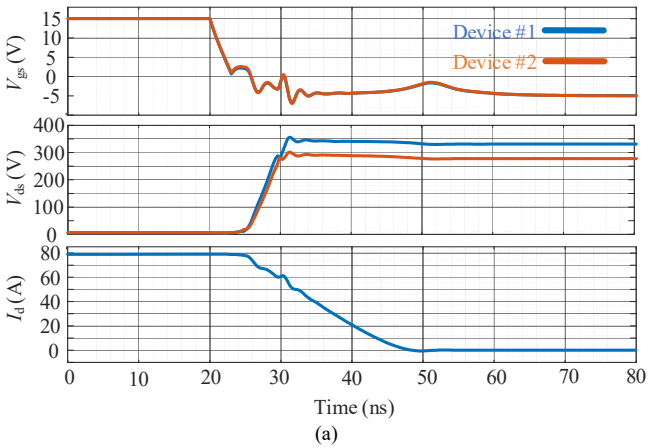
Passive snubbers are the simplest solution for voltage imbalance [101], but the snubber circuit parameters are not adaptive and the efficiency declines dramatically [102]. Master-slave switching pattern is another voltage balancing method, yet it results in large propagation delay in the system [103-106]. The active Miller clamping can also balance the voltage dynamically, but it still leads to extra energy loss [107] [108]. Additionally, the fast-switching process makes some conventional voltage balancing methods, such as adding gate chokes [109], no longer feasible for SiC systems.

AGD is a potential option for voltage balancing of series connected power devices. There are some literature reviews reporting a couple of AGD structures and algorithms to realize the voltage balance. In [110] and [111], the switching speed of series-connected devices can be controlled with an additional current source/sink. A novel AGD is proposed in [53] to eliminate the voltage imbalance caused by the discrepancy of the gate-to-ground capacitance. An auxiliary gate current is generated through the Miller capacitance to control the switching speed. A variable gate voltage technique is introduced in [112] to balance the transient voltage in virtue of controlling the *dv*/*dt*. However, the circuit schematics of the proposed variable gate voltage driver was absent in [112].

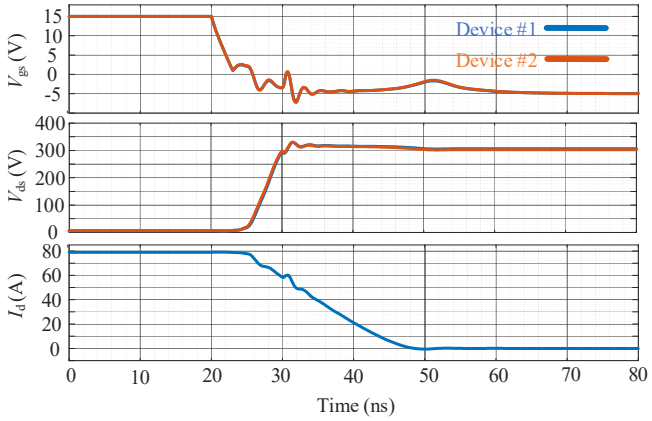
To validate that AGDs can balance the V_{ds} of series-connected SiC MOSFETs, a preliminary simulation is conducted with LTspice™. Two SiC MOSFETs C3M0065090D from Wolfspeed are connected in series and two gate drivers are connected to the gates of the two MOSFETs respectively. The high side is also a C3M0065090D. Its gate and source are shorted to prevent shoot-through. To emulate the discrepancy of electrical parameters, C_{gd} of MOSFET1 and MOSFET2 when V_{ds} =0V are 100 pF and 120 pF respectively. The dc-link voltage is 600 V and the maximum current is 79 A during the switching off transient. The gate driver is variable gate voltage AGDs which has the identical driver voltage profile in Fig. 17. The normal turn on/off voltage levels are V_{dr_on}=15V and V_{dr_off}=-5V.

Fig. 29 (a) shows the scenario without AGDs which means the gate driver is conventional two-level profile. V_{dr} of two gate drivers decreases from 15 to -5V directly. From Fig. 29 (a), without AGD, V_{ds} of two MOSFETs are unequal during the turn-off transient since the C_{gd} of the two devices is different. The maximum voltage difference is 55 V.

In contrast, another group of simulation study is conducted with the variable gate voltage AGD (V_{off_int1}= -4.5 V and V_{off_int2}= -5 V) when the other parameters remain the same. The dynamic V_{ds} curve of two MOSFETs are now matched as shown in Fig. 29 (b) and the voltage stress of MOSFET2 is effectively reduced. From Fig. 29 (b), the maximum voltage difference is reduced by ten times to 5.4 V. Table VI lists the key indices of the DPT of series-connected SiC MOSFETs. It shows that the imbalance of voltage stress and turn-off loss can be compensated with the variable gate voltage AGDs.



(a)



(b)

Fig. 29. The LTSpice simulation results of the I_d, V_{gs} and V_{ds} of two series-connected MOSFETs. (a) Without AGD. (b) With AGD.

TABLE VI
THE KEY INDICES OF THE DPT SIMULATION RESULTS FOR SERIES-CONNECTED DEVICES.

Parameters	Without voltage balance		With voltage balance	
	Device #1	Device #2	Device #1	Device #2
Eoff	1019 μJ	988 μJ	998.3 μJ	1000.6 μJ
***dv/dt* (on)**	67.4 V/ns	60.3 V/ns	62.7 V/ns	62.3 V/ns
***di/dt* (off)**	3.3 A/ns	3.3 A/ns	3.3 A/ns	3.3 A/ns
Max ΔV	55 V		5.4 V	

VI. CONCLUSION

The application of WBG devices can effectively reduce the energy loss while it also requires higher EMI noise immunity and lower circuit parasitics to avoid false triggering. In some scenarios, adjusting the slew rate is an evitable tradeoff. AGDs are invented to adjust the switching speed cycle by cycle actively to balance the power loss and side effects caused by fast switching speed.

In this paper, the fundamental mechanism of the slew rate control is demonstrated via analyzing the switching trajectory model of SiC devices. All the factors that can be utilized to adjust the switching speed are given. Based on the analysis of slew rate control mechanism, four categories of the state-of-the-art AGD methodologies are summarized. Accordingly, the available control strategies for the AGD are illustrated. Apart from EMI noise suppression, this paper also figures out three promising application scenarios of AGD technology including reliability enhancement, the current rebalancing of parallel-connected devices, and the voltage rebalancing of series-connected devices. The experimental and simulation study have validated the effectiveness of AGD in the aforementioned application scenarios.

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