A Review on Switching Slew Rate Control for Silicon Carbide Devices using Active Gate Drivers

Shuang Zhao, Member, IEEE; Xingchen Zhao; Yuqi Wei; Yue Zhao, Senior Member, IEEE; Homer Alan Mantooth, Fellow, IEEE

Abstract—Driving solutions for power semiconductor devices are experiencing new challenges since the emerging wide bandgap power devices, such as silicon carbide (SiC), with superior performance become commercially available. Generally, high switching speed is desired due to the lower switching loss, yet high $dv/dt$ and $di/dt$ can result in elevated electromagnetic interference (EMI) emission, false-triggering, and other detrimental effects during switching transients. Active gate drivers (AGDs) have been proposed to balance the switching losses and the switching speed of each switching transient. The review of the in-existence AGD methodologies for SiC devices has not been reported yet. This review starts with the essence of the slew rate control and its significance. Then a comprehensive review categorizing the state-of-the-art AGD methodologies is presented. It is followed by a summary of the AGDs control and timing strategies. In this work, using AGD to reduce the EMI noise of a 10 kV SiC MOSFET system is reported. This work also highlights other capabilities of AGDs including reliability enhancement of power devices and rebalancing the mismatched electrical parameters of parallel- and series-connected devices. These application scenarios of AGDs are validated via simulation and experimental results.

Index Terms—Active gate driver, silicon carbide, slew rate, EMI.

I. INTRODUCTION

The modern power industry is calling for high efficiency power converters for applications such as distributed generations, electric vehicles, energy storage systems, and more electric aircrafts with reduced volume and cost of the systems [1]-[2]. The energy loss of the power semiconductor devices usually consists of two major parts: conduction loss and switching loss [3]. The wide bandgap (WBG) semiconductor devices, e.g., gallium nitride (GaN) and silicon carbide (SiC) devices, are approaching ideal switches due to the lower intrinsic device parasitics and reduced switching transient times, thus the switching loss is significantly reduced compared to their silicon (Si) counterparts [4]. Moreover, the annually improving yield of WBG devices drives the cost down and it results in a further increased penetration into the power industry [5]. GaN devices are now replacing their silicon counterparts in the low voltage applications (<1.2 kV) while SiC devices may dominate the medium to high voltage applications (≥1.7 kV) in the near future [6].

High switching slew rate, i.e., $dv/dt$ and $di/dt$, is not always desired since it introduces challenges into the power converter design, especially the electromagnetic interference (EMI) noise immunity [7][8]. Specifically, high $dv/dt$ slew rate may cause high frequency noise through coupling with the heatsink or gate driver isolated power supply and finally leads to a false triggering event [9]. Another drawback is high crosstalk noise. The fast switching transient of a device in a half-bridge configuration may interact with the Miller capacitance of the complementary side switch and results in a shoot-through event [10]. Moreover, high $di/dt$ interacts with parasitic inductance of the power loop, which generates voltage overshoot and ringing on the gate [11]. In the worst case scenario, the gate loop oscillation leads to switches turn on and off repeatedly, namely self-turn-on effect [12][13].

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S. Zhao was with Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701 USA and he is now with Infineon Technologies, El Segundo, CA 90245 USA. (E-mails: shaang.zhao@infineon.com; sz009@uark.edu)

X. Zhao, Y. Wei, Y. Zhao and H. A. Mantooth are with Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701 USA. (E-mails: xczhaonuaa@gmail.com, yuqiwei@uark.edu, yuezhao@uark.edu, mantooth@uark.edu)

Fig. 1. A package with TO-Leadless (TOLL) package (left) compared to a TO-247 package (right).

Generally, a radical method to prevent false-triggering and shoot-through caused by high $dv/dt$ is to minimize the parasitics of the power and gate loops [14]. Improving the packages of the power devices such as the Infineon CoolGaN™ devices with
DSO package can effectively reduce the parasitics. A comparison between a surface mount TOLL package and a TO-247 package is shown in Fig. 1. The TOLL surface mountable package can reduce the parasitic inductance introduced by the leads. Also, a study investigates devices with the same bare dies in flip-chip packages and TO-247 in [15]. The flip chip packaged devices reduced the parasitic loop inductance from 15 nH in the wire bonded module to 5 nH [15]. This reduction declines the voltage overshoot and ringing by 14.2% and 8.7% respectively during turn-off [15].

The gate-loop ringing caused by common source inductance is the major reason of false triggering [16]. To suppress the voltage ringing, Kelvin connection is recommended for the gate driver connection [14]. Some new SiC discrete devices adopt TO-247-4 package which has a Kelvin pin instead of the traditionally TO-247-3 package. Nevertheless, various practical layout design constraints may hinder further reduction of parasitics on a printed circuit board (PCB) or a busbar, such as EMI immunity, insulation, and functions [17]. Also, the package of a discrete device, such as TO-247-3, inevitably introduces common source inductance close to 8 nH [18] and stray inductance in a commutation loop of a half-bridge module may be up to 20 nH [19].

High power efficiency and high EMI noise are the two edges of a sword in the power converter design. Properly slowing down of switching transient can mitigate the EMI noise and prevent false triggering yet increase power losses [14]. Through controlling the slew rate of switching, it is feasible to balance the energy loss against the EMI noise [20] and consequently optimize the switching process. A conventional slew rate adjustment method is changing the gate resistance [14]. Higher gate resistance can slow down the switching speed, thus the EMI noise is reduce. However, this method is not flexible since gate resistance cannot be changed while the converter is running. Since high gate resistance may increase the impedance of gate current route, it may increase the risk of false triggering unnecessarily in some circumstances. In addition, the slew rate of switching of the same converter can vary a lot in corresponding to the operating conditions such as load current and bus voltage [21]-[22]. As an emerging technology, active gate drivers (AGDs) can be utilized to optimize the switching transient cycle by cycle based on the feedback signals which indicates the system operation condition. Compared with the traditional methods, AGD can dynamically adjust the slew rate and provide an additional freedom for tradeoff of EMI noise against switching loss. In other words, AGD can optimize the switching process.

The AGD technology was first introduced for the IGBT turn-off protection [23]-[24]. Since then, both industry and academia have spent a significant amount of effort into the improvement of the AGD performance by dint of exploring various circuitries and control strategies. Various popular AGD methods and control strategies for IGBTs were summarized in [25]. An overview introducing various driving technologies for the SiC power devices are given in [26], with a main focus on the general driver and protection circuitry for SiC devices. The extensive application of SiC devices also introduces new challenges for the AGD design. In some situations, the switching transient of SiC devices can be completed in several nanoseconds. The circuit schematics, the components bandwidth, the control strategy as well as the timing strategy should be carefully designed. For this reason, some conventional AGDs designed for silicon IGBTs are not longer suitable for the novel SiC systems. A comprehensive overview summarizing of the stat-of-the-art SiC devices AGD research is still desired because it can provide guidance to the researchers in this community and figure out the future technic path. Unfortunately, there are few publications concluding the state-of-the-art AGD methods and the slew rate control strategies for switching transient [27].

To fill this gap in the AGD research, this paper starts with the essence of the slew rate control via analyzing the fundamental mechanism with the SiC MOSFET trajectory model. Specifically, all the factors that impact the slew rate are extracted and how high slew rate of SiC devices increases EMI noise is analyzed in Section II. Based on the theoretical analysis, Section III demonstrates various slew rate control methods from gate driver side. Four types of AGDs circuits is illustrated and various on-going research of AGDs are also presented. In Section IV, three categories of in-existence control strategies and timing strategies of AGD are described in details. All AGD methodologies and control strategies are also summarized in this section. Section V points out several typical applications, i.e., on-line EMI noise suppression, reliability enhancement, current balancing of parallel-connected device and voltage balancing of series-connected device. Specifically, double pulse test (DPT) is performed to validate that AGD can alleviate the EMI noise in a 10 kV SiC MOSFET system. The switching speed rebalancing of parallel- and series-connected devices with AGD are verified with experimental and simulation study respectively. The conclusions of this review are drawn in Section VI.

II. ESSENCE OF SLEW RATE CONTROL OF POWER DEVICES

Fig. 2 shows an equivalent circuit of a MOSFET with the DPT setup[28]. Its gate and source terminals are connected to a
Correspondingly, the working principle of all slew rate control methods is to adjust the charging/discharging speed of capacitance and plateau period when \( \frac{dv}{dt} \) is high shown in Fig. 3 [29]. In Fig. 3, the intrinsic input junction power device during the switching process can be simplified as traditional model of silicon IGBT or MOSFET. The trajectory model of SiC device is slightly different from transistor is non-flat due to the low junction capacitance. The trajectory model of a SiC MOSFET can be found in [34] while silicon MOSFET can be found in [28].

Based on the aforementioned analysis, the state-of-the-art AGD methods can be categorized into several basic types: variable gate resistance method, variable input capacitance method, variable gate voltage method, and the variable gate current method [25][30][31].

B. Influence of different factors on the switching slew rate

Since different AGD methodologies have different control variables, it is necessary to study how these variables affect the switching transient and quantify their effect on the switching speed. In this section, key indices that affect the performance are extracted from a mathematic model of the power devices. It should be noted that a linearized trajectory model is used in this paper to study the impact of different factors qualitatively.

a) Turn-on process

In Fig. 4, \( t_2 - t_1 \) is the turn-on delay. \( t_3 - t_2 \) is the \( I_{th} \) rising time and \( t_4 - t_3 \) is the \( V_{ds} \) falling time. The \( \frac{dv}{dt} \) and \( \frac{dv}{dt} \) can be approximately calculated by (1) and (2), respectively, [21][32][33]. The variables that may be used to control the slew rate are marked in red.

\[
\frac{dv}{dt} = \frac{I_{th}}{C_{gs} + C_{gd}} + \frac{V_{ds}}{g_m} \quad \text{(1)}
\]

\[
\frac{dv}{dt} = \frac{I_{th}}{C_{gd}} + \frac{V_{ds}}{g_m} \quad \text{(2)}
\]

where \( V_{miller} \) is the Miller plateau voltage, which is calculated as

\[
V_{miller} = V_{th} + I_{th} / g_m \quad \text{and} \quad g_m \quad \text{is the transconductance. \( I_{th,12} \)}
\]

is the average gate current in the period \( t_2 - t_1 \) and \( I_{th,13} \) is the average gate current in the period \( t_3 - t_2 \).

b) Turn-off process

In Fig. 4, \( t_6 - t_4 \) is the turn-off delay. \( t_{10} - t_{11} \) is the \( I_{th} \) rising time and \( t_{10} - t_{11} \) is the \( I_{th} \) falling time. \( \frac{dv}{dt} \) and \( \frac{dv}{dt} \) can be approximately calculated with (3)-(4) [32][34].

\[
\frac{dv}{dt} = \frac{I_{th,10}}{C_{gd} + C_{gs}} \quad \text{(3)}
\]

\[
\frac{dv}{dt} = \frac{I_{th,10} + I_{th,11}}{C_{gd} + C_{gs}} + \frac{V_{miller} - V_{off}}{2g_m} \quad \text{(4)}
\]

\( I_{th,10} \) is the average gate current in the period \( t_9 - t_{10} \) and \( I_{th,10,11} \) is the average gate current in the period \( t_{10} - t_{11} \). The switching energy loss can be roughly evaluated with (5).

\[
E_{on} = \frac{V_{bus}I_{th,10}^2 + V_{bus}I_{th,11}^2}{2dV/dt} \quad \text{(5)}
\]

### TABLE I

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<th>Variable</th>
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3
In (5), \( V_{bus} \) is denoted by dc bus voltage and \( I_0 \) is the load current. In (1)-(4), all the controllable variables are marked in red. It is evident to observe how these variables affect the slew rate. The deductions from the equations are concluded in Table I. It should be noted that \( I_g \) in Table I is the absolute value of the gate current. From Table I, decreasing \( I_g \) or increasing \( R_g \) can effectively reduce the slew rate while increasing \( C_{gd} \) can effectively reduce the slew rate [27][37]. This argument has been verified in [35] and [36].

C. EMI noise and other detrimental effects of high switching slew rate

The foremost application of AGD is to mitigate EMI noise. The mechanism how \( dv/dt \) impacts the EMI noise in the system should be analyzed in prior to designing the power converter. [38]-[40] demonstrate the mechanism of EMI noise caused by high \( dv/dt \) during the switching of power devices.

The analysis of a switching waveform, as shown in Fig. 5, should take the rising and falling edges into consideration. The duration of voltage rising/falling time \( t_{rv} \) and \( t_{ft} \) are critical for the noise spectrum because they determine the two corner frequencies \( f_{c2} \) and \( f_{c3} \) which are shown in Fig. 6. If the \( dv/dt \) during the turn on/off transient increases, \( t_{rv} \) or \( t_{ft} \) will reduce and the corner frequency \( f_{c2} \) or \( f_{c3} \) will increase. As a result, the EMI noise will rise which is depicted in Fig. 6.

Another problem of high slew rate is the rising risk of false triggering. One reason of false triggering is self-turn-on of the power switch. When the gate current flows back to the gate driver power supply, the voltage on gate resistor may cause a temporary \( V_{gs} \) rising. If this \( V_{gs} \) rising is higher than \( V_{th} \), the power switch turns on falsely again and a shoot-through event may occur [14]. Another reason is crosstalk noise which can be explained via the propagation route in Fig. 8.
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IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS 5

A. Variable gate resistance method

Variable gate resistance method is the most widely used approach for slew rate control. Its attractive features, such as low cost and easy implementation, make it feasible for the EMI mitigation in some industrial applications [42]. Its working principle is straightforward [43]. Via adjusting gate resistance for different stages in a switching transient, \(dv/dt\) and \(di/dt\) can be changed. Its basic circuitry can be depicted in Fig. 9. Through controlling the switches \(SW_{on2} - SW_{on1}\), \(SW_{off2} - SW_{off1}\), the value of gate resistors connected in the gate loop can be changed, thus the total gate resistance is adjusted [44].

The switching waveforms of a typical variable gate resistance AGD are plotted in Fig. 10 [45]. Generally, high gate resistance, i.e., \(R_{on1}\) and \(R_{off}\) in Fig. 10, is utilized during the Miller plateau period to suppress slew rate and low gate resistance is employed before/after the Miller plateau to reduce the false-triggering risk. It should be noted that the method in Fig. 9 requires additional gate resistors and BJTs to provide more adjustable steps [46]. Furthermore, if the gate charge of the power module is high, the footprint of the gate resistors should also be large to dissipate the driver loss. Therefore, a variable gate resistance AGD can hardly provide high adjustment resolution for slew rate owing to the PCB size limitation. Various AGD circuits based on this methodology have been proposed in [44]-[47].

A simple variable gate resistance AGD circuit, as shown in Fig. 11, is proposed in [46]. Three totem-pole driver ICs, i.e.,

![Diagram of A typical circuitry of variable gate resistance method.](image)

![Diagram of Variable gate resistance method.](image)

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In Fig. 8 (a), when Q2 turns on, the slew rate of \(V_{ds1}\) triggers current across the \(C_{gd1}\), which can be denoted by \(C_{gd1}V_{ds1}/dt\). When this current flows through gate resistor \(R_g\), a voltage spike \(V_{gs} = i_dR_g\) is generated on the gate of Q1 [41]. An example of the crosstalk noise on a single-phase converter is captured in Fig. 8 (c). CH3 and CH4 represent the experimental result of voltage spike on the \(V_{gs}\) caused by crosstalk noise. In Fig. 8 (a), when Q2 turns on, the slew rate of \(V_{ds1}\) triggers current across the \(C_{gd1}\), which can be denoted by \(C_{gd1}V_{ds1}/dt\). When this current flows through gate resistor \(R_g\), a voltage spike \(V_{gs} = i_dR_g\) is generated on the gate of Q1 [41]. An example of the crosstalk noise on a single-phase converter is captured in Fig. 8 (c). CH3 and CH4 represent the experimental result of voltage spike on the \(V_{gs}\) caused by crosstalk noise.

![Diagram of Voltage spike and crosstalk noise propagation.](image)

![Diagram of The simplified waveform of crosstalk noise.](image)

![Diagram of Voltage spike and crosstalk noise propagation.](image)
Buffer1-3, are connected in parallel to control the gate resistance dynamically. The three turn-on/off resistors have different resistances. The driver ICs should select the ones with independent gate current source pins and sink pins such as Infineon® 1EDN751. Via controlling the conduction of the buffers in different stages of switching process, the gate resistance can be adjusted. Another state-of-art variable gate resistance AGD method is proposed in [48-50]. An optic diode is adopted to replace the conventional physical gate resistor. Through tuning the illumination to the optic diode, the conduction resistance of the diode can be changed and the switching slew rate can be controlled.

**B. Variable input capacitance method**

The variable input capacitance method regulates $C_{iss}$ to control the switching slew rate as depicted in Fig. 12. In brief, via controlling the switches $SW_{di1}/SW_{di2}$-$SW_{dn}$, total capacitance of $C_{gd,ext}$ and $C_{gd,ext}$ which are connected in parallel with MOSFET capacitance $C_{gd}$ and $C_{gs}$ can be changed. Consequently, the gate input capacitance charging/discharging speed can be adjusted under different total capacitance values. The effectiveness of this type of method has been validated in [27] and [51]. However, this is a non-preferable solution due to its intrinsic defects.

Adding a capacitor $C_{gs,ext}$ is a common solution to gate loop oscillation damping and switching transient slowing down [14]. However, since the charging time of $C_{gs}+C_{gs,ext}$ increases dramatically, this method inevitably increases the turn-on/off delay time. Also, since peak gate current equals to $(C_{gs}+C_{gs,ext})dV_{gs}/dt$, a large $C_{gs,ext}$ can probably increase the peak gate current thus increase the false triggering risk reversely. Therefore, a very large $C_{gs,ext}$ is not recommended. Apart from $C_{gs,ext}$, $C_{gd,ext}$ can be another potential solution for the switching speed adjustment. Nonetheless, this is not common because $C_{gd,ext}$ should choose a capacitor which has higher voltage rating than the $V_{ds}$ of the device. Also, during Miller plateau of turn-off process, the gate current can be expressed with $I_g = (C_{gd}+C_{gd,ext})dV_{ds}/dt$. Therefore, a high $C_{gd,ext}$ increases the voltage drop on $V_{ds}$ during turn-off. Therefore, from Eq. (6), this may not reduce the self-turn-on risk.

**C. Variable gate current method**

Variable gate current method usually utilizes a current source to change the gate current. In other words, the power device switching speed can be controlled by means of adjusting the gate current which charges/discharges $C_{iss}$.

![Fig. 13. The working principal of an active current source gate driver.](image)

Its functionality in regard of the switching slew rate control has been validated in [35], [52]-[55]. The working principle of a variable gate current method is depicted in Fig. 13 [52]. $SW_{on,1}$ and $SW_{on,2}$ are complementary switches for turn-on slew rate control while $SW_{off,1}$ and $SW_{off,2}$ are complementary switches for turn-off. $I_{g_{reg}}$ is the nominal gate current from the current source gate driver. There are two additional current sources $I_{gon_1}$ and $I_{goff_1}$ adjusting the gate current during the switching transient. The waveform of the latter condition is given in Fig. 14.

![Fig. 14. The waveform of the variable gate current method AGD.](image)
From Fig. 14, the gate current of AGD is $I_{g_{\text{reg}}}$ for turn-on/off delay. During the Miller plateau, $SW_{\text{on,1}}$ is on and $SW_{\text{on,2}}$ is off. The current source $I_{\text{gon,1}}$ will bypass a part of gate current. $I_g$ reduces from $I_{g_{\text{reg}}}$ to $I_{g_{\text{reg}}}-I_{\text{gon,1}}$ and the turn-on is slowed down. The turn-off process is similar. If the switching speed is desired to be accelerated, more gate current can be injected into $C_{\text{gs}}$ during the Miller plateau period.

D. Variable gate voltage method

The variable gate voltage method can adjust the gate voltage during the switching transient to control its trajectory. It attracts attention since its working principle is pertinent to the conventional gate drive methods [59]. The advantage of this method over the variable resistance method is its flexibility since an adjustable voltage regulator is always easier to be implemented. Additionally, considering that a prevailing shoot-through protection method is using multi-level turn-off to reduce the overshoot voltage when desaturation signal is detected, this AGD method is more convenient to provide the protection without sophisticated additional circuitries [60], [61]. Different topologies of the variable gate voltage AGD methods are proposed in [20] [24] [32] [34] [59-65].

Fig. 15. The proposed circuit of variable gate current AGD in [53].

A current mirror circuit is an accessible option to realize a voltage controlled current source. [53] and [54] adopt current mirror circuits to extract the gate current during the switching transient. The circuit schematics is plotted in Fig. 15. The output current of a current mirror circuit, which incorporates BJTs Q1-Q4, can be controlled via changing the reference voltage $V_{\text{ref.}}$. A digital-analog converter (DAC) with an local controller such as an FPGA or CPLD chip can be employed to adjust $V_{\text{ref.}}$.

Several circuitries of current source gate drivers with inductors which can store the gate charge are introduced in [56] and [57]. The proposed resonant current source gate driver can effectively reduce the power loss caused by drivers [58]. Indeed, current source gate drivers are more complex than voltage source gate drivers. Nonetheless, they have a merit with respect to higher power efficiency since it can eliminate the power loss dissipated on the gate resistor [56], [55] also claims that a current source gate driver can reduce the turn-on loss of an IGBT at similar that a current source gate driver can reduce the turn-on loss of an IGBT. The proposed resonant current source gate driver can effectively reduce the power loss caused by drivers [58].

Fig. 16. The simplified block diagram of a variable gate voltage AGD.

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Fig. 17. The simplified block diagram of a variable gate voltage AGD.

The block diagram of the variable gate voltage AGD can be explained in Fig. 16. In general, the gate driver can be equivalent to a controlled voltage source. The desired driver voltage profile is first generated by an arbitrary waveform generator under the control of the AGD local controller and then amplified by an amplifier stage. Its working principle can be explained with Fig. 17 which shows the waveforms of a multi-level gate voltage profile. During the Miller plateau stage of the switching transient, the driver voltage are adjusted to a certain value, i.e., intermediate voltage, to regulate the switching speed to a desired level. After the switching ends, the driver voltage recovers to the normal turn on/off voltage.

In order to generate the waveforms in Fig. 17, an AGD circuit is proposed in [34] and [64]. An adjustable voltage regulator consists of a DAC which controls the intermediate voltage level one switching cycle in advance and a voltage amplifier which provides enough power to drive the power MOSFET. Then three cascaded-connected totem-pole driver buffers operates to generate the multi-level driver voltage profile in Fig. 17. To further optimize the switching slew rate, an S-shape slew rate control profile for the power devices is proposed in [20]. However, the circuitry that generates S-shape profile is complex or expensive. Another method, which is introduced in [59] and [65], can realize the same goal through changing the potential of MOSFET source to change $V_{gs}$. 

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IV. CONTROL STRATEGIES FOR AGDs

The dominant challenge of AGD control strategies implementation is the short duration of each switching transient which is usually nanosecond (ns) level. For the sake of various optimization targets, there are several potential control variables: the switching slew rate, the junction temperature \( T_j \), EMI noise, and duration of each sub-stage. The selection of the control variables is usually based on the requirements of a particular application.

A. Open-loop control

The block diagram for a typical open-loop control is shown in Fig. 19. The main control unit (MCU) generates the PWM gate signals. A same driver voltage profile is usually applied to all scenarios. For instance, for the variable gate resistance method, the gate resistance and duration remain constant even though the operation condition changes. The open-loop method is simple and cost-friendly since no sensor for feedback signals is required [25].

A commercially available product is demonstrated in [66]. However, as analyzed in Section II, the performance indicators such as the EMI noise and power loss may be different under different operation conditions such as load current and bus voltage. Particularly, even for a same power device, the performance indicators such as the \( dv/dt \), \( di/dt \), and energy losses may be different when the device is degraded [67][68]. Therefore, the open-loop method can hardly ensure that the power device always operate at the optimal condition. Much effort is dedicated into the development of open-loop AGDs.

[44] and [45] introduce the variable gate resistance AGD with open-loop control strategy, while [64] introduces the variable gate voltage AGD with open-loop strategy.

B. Measurement-based control

A block diagram of the measurement-based control is given in Fig. 20. The AGD has sensor circuits for detecting the feedback signals such as \( dv/dt \), \( di/dt \), energy losses, \( T_j \) etc. which will be sent to a signal conditioning circuit. A local control unit controls the output of the AGD and ensures the feedback signals track their references. A timing control circuit is used to ensure the AGD acts at the correct time point. The error between the reference and feedback signal is compensated by a controller. The timing signals and controller output will be sent to the AGD circuit to control the switching of the power devices.

Since the switching process is rapid (typically nanosecond level), the slew rate feedback is hard to implement [25]. A straightforward \( dv/dt \) measuring method is sensing the IGBT collector- emitter voltage \( V_{ce} \) and calculating the slew rate with a digital controller [25]. In [69], \( dv/dt \) is sensed directly with the voltage divider circuit with a high bandwidth op-amp OPA847. The direct slew rate feedback method works well for the IGBTs.
whose switching transient is longer than 1 μs [25]. The WBG devices require very high-bandwidth sensors and analog-to-digital converters which are costly. Therefore, in [35], \( \frac{dv}{dt} \) is measured through sensing the current across capacitors which are connected between source/gate and drain. \( \frac{di}{dt} \) indicates the overshoot voltage on \( V_{ce} \) or \( V_{ds} \). Accordingly, the \( \frac{di}{dt} \) can be measured through sensing the voltage drop on the stray inductance, which has been validated in [25] [60] [62] [70-72].

An example of a control block diagram with \( \frac{dv}{dt} \) and \( \frac{di}{dt} \) feedback is shown in Fig. 21. \( \frac{dv}{dt} \) is measured through sensing the voltage on the inductance \( L_{ac} \), \( \frac{dv}{dt} \) measurement is conducted with RC networks (\( R_{V} \) and \( C_{V} \)) since the current that flows through \( C_{V} \) is proportional to the \( \frac{dv}{dt} \). The RC networks are connected in series to reduce the total parasitic inductance and increase the maximum voltage. The slew rate signals are feedback and compared with the reference signals. An analog proportional integral (PI) controller is utilized to compensate the steady-state error. Considering that the bandwidth of PI controller is determined by the opamp, it is necessary to select some high bandwidth opamps for SiC devices. Also, two threshold voltage levels \( V_{1} \) and \( V_{2} \) are used to compare with slew rate feedback signals. The outputs of comparator CMP1 and 2 indicate the start point of power MOSFET switching, thus they are utilized as the timing signals to trigger the AGD at correct time. The ultra-fast comparators with low propagation delay such as MAX9601 and ADCMP551 are recommended for WBG device.

An optimal control strategy to compensate the thermal stress on the parallel-connected switches is introduced in [73]. \( T_{j} \) of the two switches are measured and the switching delay time is controlled correspondingly. [53] and [74] utilize the on-state \( V_{ds} \) of MOSFETs as the feedback signals to balance the voltage on the series-connected power devices. Once the slew rate feedback is sent to the local control unit, the optimal switching speed will be calculated with the given reference signals. A comparator can be employed to limit the slew rate to a certain level. When the slew rate is higher than this threshold, the AGD will intervene to slow down the switching. This control strategy has been presented in [39]. [25] and [62] used analog PI controllers to track the slew rate reference signals. Thanks to the advancement of digital processors, the high-speed processors such as FPGA or CPLD can be applied to AGDs which are reported in [54] and [75].

C. Estimation-Based Control

When the slew rate is higher than the bandwidth of the sensors, the direct measurement is no longer possible. Moreover, junction temperature measurement is arduous if the power module does not include thermal sensors inside. To solve this problem, the feedback indices can be estimated with the mathematical model which can accurately characterize the switching trajectory or thermal curve [118].

A switching trajectory model of power devices can derive the switching performance of a power device with other accessible feedback signals. For example, instead of measuring the slew rate directly, a datasheet-driven trajectory model as well as the parasitics of the circuit, load current, and bus voltage are adopted to predict \( \frac{dv}{dt} \) and \( \frac{di}{dt} \) in [32]. Since the MOSFET parameters, load current, and bus voltage of a PWM converter can be assumed to be constant in a switching cycle, no ultra-fast sensor is required to detect the slew rate.

Fig. 22 describes the control scheme of an estimation-based control strategy of the AGD. The AGD receives feedback signals such as dc bus voltage \( V_{bus} \), load current \( I_{load} \), etc. The local control unit reads feedback signals and calculates the performance indicators with the trajectory model. An example is given in [34]. The prediction of slew rate and energy loss is performed with the feedback of dc bus voltage and load current. A cost function in regard of the intermediate driver voltage considers the tradeoff of EMI noise against power loss. Once the voltage with the lowest cost is selected for next switching cycle, the timing sequence of this driver voltage can be determined with the trajectory model. Compared with the offline-tuned AGD, the adaptive method can reduce the EMI noises and energy losses of the power device.

Similarly, if junction temperature is the the feedback signal, thermo-sensitive electrical parameters (TSEP), such as peak gate current, gate charge, or turn-off delay time, can be feedback to estimate the junction temperature [116]. Miscellaneous TSEP detection circuits can be found in [117]. The drawback of TSEP method is the necessity of a data-driven thermal model of a specific SiC devices. To the best knowledge of the authors, AGD with TSEP function has not been reported, yet it is a potential and interesting solution for the thermal management of a power conversion system.

The performance of this method highly depends on the accuracy of the behavior model. However, in the real world, parasitics are not always constant during the switching and some parameters are difficult to measure. Also, the switching behavior can change dramatically due several factors such as \( T_{j} \) and humidity [76]. An on-line model-based control increases the computation load of the controller of the gate driver. Therefore, this method still need to be matured for real world applications.
D. Timing Strategy

As mentioned in Section II, it is necessary to adjust the AGDs output in every sub-stage of a switching process. Specifically, \( R_g \), \( I_g \) and/or \( V_{gs} \) are adjusted during the Miller plateau. After the switching transient ends, the output AGD should be clamped at the normal turn-on or turn-off mode. Therefore, it is critical to have correct timing control. Missing the proper time instant may result in failure of switching or extended switching duration. Generally, the existing timing control approaches can be categorized into two types, i.e., feedback-based strategy and timer-based strategy. The feedback-based strategy needs certain external feedback circuits to trigger the AGD at the start of each sub-stage of the switching transient. A timer-based strategy needs a timer to count the duration of each sub-stage and control the AGD to adjust the output correspondingly.

Several typical feedback-based strategies are demonstrated in [45]. The key point of the proposed method in [45] is high-speed comparator. The \( V_{gs} \) is sensed and input to the comparator. During turn-on process, when \( V_{gs} \) increases to a level higher than gate-source threshold voltage, the power device starts conducting and the AGD changes the output control variables. It can be depicted in Fig. 21 and Fig. 22.

Several typical timer-based strategies are introduced in [52] and [54].

Based on the introduction above, various state-of-the-art AGD methodologies as well as the control strategies are compared and summarized in Fig. 23. The advantages and disadvantages of various strategies are listed in Table II. It should be noted that every methodology has its own cons and pros which make it appropriate for some certain application scenarios. In general, the variable gate resistance method is relatively simple to implement and the cost-efficient while it is unsuitable Therefore, it is preferred in some scenarios when cost-reduction dominates the design consideration. The variable gate voltage method can provide high adjustment resolution and it is very similar to the desaturation protection. Thus, this method is appropriate for case when the system

![Fig. 23. A summary of the state-of-the-art AGD methodologies.](image)

**TABLE II**

<table>
<thead>
<tr>
<th>AGD methodologies</th>
<th>Control strategies</th>
<th>Advantages</th>
<th>Disadvantages</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>Variable gate resistance method</td>
<td>Open-loop</td>
<td>Low cost and easy implementation. Simple circuitry.</td>
<td>Requires additional gate resistors and BJTs to provide more adjustable steps. Hard to realize high adjustable resolution for driving speed.</td>
<td>[43]-[50]</td>
</tr>
<tr>
<td>Variable gate voltage method</td>
<td>Direct feedback-control</td>
<td>Straightforward working principle. High adjustment resolution. Easy to provide soft turn-off for short circuit protection.</td>
<td>Complex circuitry and control.</td>
<td>[20], [24], [32], [34], [59]-[65]</td>
</tr>
<tr>
<td>Variable gate current method</td>
<td>Model-based indirect control</td>
<td>Good gate loop oscillation suppression effect.</td>
<td>Complex circuitry and control.</td>
<td>[52]-[57]</td>
</tr>
<tr>
<td>Variable input capacitance method</td>
<td></td>
<td>Simple circuitry and low cost.</td>
<td>Increasing switching delay time. External ( C_{gd} ) requires high voltage rating.</td>
<td>[14], [51]</td>
</tr>
</tbody>
</table>

- **Open-loop control**: Simple and low cost.
- **Direct feedback control**: Straightforward control design.
- **Model-Based Indirect Control**: Prevent using high speed sensors which reduces cost.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
</table>

In general, the variable gate resistance method is relatively simple to implement and the cost-efficient while it is unsuitable. Therefore, it is preferred in some scenarios when cost-reduction dominates the design consideration. The variable gate voltage method can provide high adjustment resolution and it is very similar to the desaturation protection. Thus, this method is appropriate for case when the system.
reliability has high priority. The variable gate current method is generally based on a current source gate driver. A conventional current source gate driver utilizes a resonant driver topology which can reduce driver loss. It has superior gate oscillation suppression effect and efficiency, but it is complex and expensive generally. All of these features make it suitable for the case that cost is not the top priority consideration. It should be noted that the difficulty of implementation is determined by the specific employed circuits. In conclusion, the major challenge of the AGD development is still the feedback control design. Most commercialized products do not provide feedback control and adaptive timing strategy. Therefore, based on the insight of the future trend, exploring novel AGD circuits with feedback control for WBG devices is a thrust of this research.

V. CONVENTIONAL AND EMERGING APPLICATIONS OF AGDs

Most existing applications for AGD aim at mitigating the side effects of high switching slew rate such as EMI noise. Also, the AGDs have potential to be applied in the following scenarios: reliability enhancement of power device, current balance of paralleled devices, and voltage balance of series connected devices. The following sections will discuss these application scenarios one by one.

A. The conventional applications

In some cases, the switching slew rate is high while the system is vulnerable to EMI noise. For instance, the solid-state transformer with high voltage (≥10 kV) SiC power devices is an emerging technology for the distributed system [77][78]. As reported in [79], the slew rate of \( \frac{dv}{dt} \) can be even higher than 70 V/ns. This may affect the robustness of system operation. It is desired to actively adjust the slew rate to balance the EMI noise and energy loss.

A high gate resistance or external \( C_{gs} \) can reduce the slew rate, but it may dramatically increase the dead-time and affect the control of the dual active bridge converter. Therefore, in this situation, an AGD can be employed to dynamically adjust the slew rate in regard of the specific switching situations. An DPT testbed with a 10 kV SiC MOSFET module and a variable gate voltage AGD is shown in Fig. 24. The schematics of the AGD circuit can be referred to [34]. The parameters of DPT setup are listed in Table III.

---

### TABLE III

<table>
<thead>
<tr>
<th>Parameter Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC bus voltage</td>
</tr>
<tr>
<td>Maximum load current</td>
</tr>
<tr>
<td>Load inductor</td>
</tr>
<tr>
<td>Oscilloscope</td>
</tr>
<tr>
<td>( V_{in} ) probe</td>
</tr>
<tr>
<td>( I_{in} ) probe</td>
</tr>
<tr>
<td>( V_{out} ) probe</td>
</tr>
<tr>
<td>Device under test</td>
</tr>
</tbody>
</table>

---

A 300 MHz Altera 10M08SAU169C8G FPGA chip is used as the local control unit. A DSP controller is the MCU which generates the double pulse gate signals and a Broadcom AFBR1624 fiber optical transceiver is used to isolate the gate signals. The power supply is Power Integration ISO5125i which provides 18 kV galvanic isolation. Two Murata MGI2 power supply modules are tied with the ISO5125i to provide bipolar voltage (20V/-5V) for the gate driver.

The driver voltage profile is similar with the waveforms in Fig. 17. Fig. 25 (a) shows the turn-off waveforms of the DPT under different turn-off intermediate voltage, i.e., \( V_{off\_int} \) in Fig. 17. All indices of Fig. 25 (a) are extracted in Table IV.

---

### TABLE IV

<table>
<thead>
<tr>
<th>( V_{off_int} )</th>
<th>( \frac{dv}{dt} ) (V/ns)</th>
<th>( \frac{di}{dt} ) (A/ns)</th>
<th>Turn-off energy losses</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( 5 ) V</td>
<td>94.78</td>
<td>0.34</td>
<td>2302 ( \mu )J</td>
</tr>
<tr>
<td>( 5 ) V</td>
<td>58.8</td>
<td>0.158</td>
<td>4384 ( \mu )J</td>
</tr>
<tr>
<td>( 5.6 ) V</td>
<td>54.32</td>
<td>0.145</td>
<td>4629 ( \mu )J</td>
</tr>
<tr>
<td>( 6.3 ) V</td>
<td>52.4</td>
<td>0.138</td>
<td>4977 ( \mu )J</td>
</tr>
<tr>
<td>( 6.9 ) V</td>
<td>49.16</td>
<td>0.122</td>
<td>5555 ( \mu )J</td>
</tr>
<tr>
<td>( 7.5 ) V</td>
<td>43.56</td>
<td>0.109</td>
<td>6259 ( \mu )J</td>
</tr>
<tr>
<td>( 8.1 ) V</td>
<td>40.37</td>
<td>0.097</td>
<td>7410 ( \mu )J</td>
</tr>
</tbody>
</table>

---

From Fig. 25 (a) and Table IV, it is evident that with higher intermediate voltage, the slew rate is reduced while the turn-off delay time is not influenced. Fig. 25 (b) compares the spectrum analysis plot with a conventional gate driver, AGD with \( V_{int}=5 \) V and 8.1 V. From Fig. 25 (b), the high-frequency harmonics of conventional gate driver is the highest among the three curves while AGD with \( V_{int}=8.1 \) V is the lowest. Therefore, AGD can actively adjust the slew rate of 10 kV SiC power devices switching, thus suppress high EMI noise in the system.
The reliability of semiconductor devices is critical to the power electronics systems. High thermal stress is one of the major reasons of the power devices failure [81]. The repetition of thermal cycles may lead to the fatigue of solder joints due to different thermal expansion coefficients of copper and ceramic materials of the substrate [82]. The classic lifetime model of power modules can be evaluated with (8) [83].

\[ N_i = a \cdot \Delta T^n \cdot e^{\frac{E_i}{k_B T_i}} \tag{8} \]

where \( N_i \) is the number of cycles to failure, \( \Delta T \) is the amplitude of thermal fluctuation, \( k_B \) is the Boltzmann constant and \( T_i \) is the average junction temperature. Other parameters are the fitting results of the reliability experimental results. From (8), the lifetime of the power device is affected by the \( \Delta T \) and \( T_{i,m} \). Therefore, the reliability of power devices can be improved by reducing both of them [84].

Active temperature control (ATC) can be utilized to regulate the loss and junction temperature of power devices [85]. The principle is adjusting \( T_i \) actively via controlling the energy loss of the power switches. The existing ATC methods can be divided into three categories: system level [86–87], modulation level [88–90], and gate driver level [91–93]. System-level ATC is usually applied to parallel-connected converters through controlling the loss distribution [86]. A modified modulation algorithms can also regulate the loss of different devices in one power converter. Nevertheless, the coupling between the energy loss on different devices may hinder ATC strategy being functional [88][89]. The adaptive switching frequency based on the \( T_i \) of power devices can be employed to prevent overheating [90]. It should be noted that this method cannot control the \( T_i \) of a specific single device independently and it may sacrifice the converter performance.

Compared with the two aforementioned methods, the AGD is more straightforward and efficient. [84] has validated that the turn-off driver voltage profile impacts on the reliability of the power devices. For this reason, the driver voltage can be regulated to control the switching and conduction loss and consequently the thermal cycling can be decreased [91]. An AGD which operates to counteract variations of the MOSFET on-state resistance based on the temperature feedback is proposed in [92]. A three-level AGD with controllable on-time is introduced in [93] to suppress the thermal cycling amount of a GaN-based dc/dc converter. Via controlling the duration of the intermediate gate voltage, the switching loss as well as the thermal fluctuation can be effectively regulated. It should be noted that all the AGDs methodologies introduced in Section III can be potentially employed to enhance the system reliability.

C. Parallel connection of power devices

Parallel connection of power devices, as shown in Fig. 26, is regularly used in the industry to boost the current rating of the power converters. Tesla Model S and Roadster have 2 × 14 parallel connected discrete IGBTs in TO-247 package for the
on-board charger and motor drive [94]. Compared with a single power device with high current rating, parallel connected devices are relatively affordable and can reduce the total power loss [95]. Additionally, hybrid power devices such as SiC MOSFET + Si IGBT are now emerging as technologies to make use of the advantages of both types of devices [73].

The thermal imbalance caused by the current imbalance is the major issue for paralleling power devices. The device suffering from higher current stress may be damaged first. The reasons leading to the current imbalance are diverse. The discrepancies of power devices electrical parameters such as the gate threshold voltage $V_{th}$, on-state resistance $R_{ds\_on}$, and parasitic stray inductance are the major reasons [96]. The discrepancy of the gate driver of each device and the unequal parasitics in the power/gate loop caused by undesired PCB layout may also aggravate the current imbalance.

Even though the PCB parasitics are distributed averagely on each device, some thermo-sensitive parameters of the power devices such as $V_{th}$ and $R_{ds\_on}$ may still intensify the current mismatching [97]. For instance, $V_{th}$ decreases with the increasing junction temperature for most power devices, which aggravates the thermal imbalance. The forward voltage of most IGBTs shows negative temperature coefficient, so the higher temperature one shares more current stress and this feature increases its junction temperature in return. Addressing the problems above from the driver side is a favorable engineering solution since no modification needed in the power loop.

AGD is an effective method to compensate the current unbalance. A conventional method is adjusting the delay of the gate signal [96], [98], [99]. However, the delay of gate signal cannot compensate the unequal current completely in some cases. The gate signal delay and gate drive voltage are controlled in the AGD proposed in [100] to compensate the differences of turn on/off delay and slew rate of current respectively for Si IGBT. However, the active control of gate voltages of paralleled SiC MOSFETs has not been explored in previous work. DPT experimental study are conducted to validate current balancing function of variable gate voltage. The bus voltage is 400 V and total load current is 25 A. Two Wolfspeed C3M0065090D SiC MOSFETs are connected in parallel to be tested. High side is a C4D40120D SiC diode. The AGDs have multi-level turn-on voltage profile and their schematics can be found in [34]. The gate resistances of these two AGDs are both 5 Ω. The DPT experimental results are shown in Fig. 27 and the key indices of the results are listed in Table V. The right two subplots of Fig. 27 show the details of the zoom-in area of the left subplots. In Fig. 27 (a), the switching transient of the two devices is not synchronous without current balancing. Device #2 has higher slew rate than Device #1. Therefore, the energy loss of the Device #2 is higher than Device #1. To balance the transient $I_{ds}$ of the two devices, the intermediate driver voltage levels of the two devices, i.e., $V_{on\_int}$ in Fig. 17, are changed. The Device #2 reduces to 18 V while Device #1 remains at 20 V. Fig. 27 (b) shows the
experimental results after current balancing with AGDs are functioning. From Fig. 27 (b), the turn-on transient current is balanced and the total energy loss is now distributed averagely on the two devices.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Without current balance</th>
<th>With current balance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eon</td>
<td>78.5 μJ</td>
<td>55.1 μJ</td>
</tr>
<tr>
<td>dv/dt (on)</td>
<td>8.9 V/ns</td>
<td>8.9 V/ns</td>
</tr>
<tr>
<td>dv/dt (off)</td>
<td>0.50 A/ns</td>
<td>0.53 A/ns</td>
</tr>
</tbody>
</table>

Table V: The indices of the DPT results for parallel-connected devices.

D. Series connection of devices

Thanks to the advancement of SiC technologies, the voltage rating of power semiconductor devices increases to the level higher than 10 kV which enables power electronics converter be extensively applied in the power grid. In high voltage systems such as distributed grid, power devices are often connected in series to increase the total voltage rating, as shown in Fig. 28. Nevertheless, in some conditions, the voltage may not disperse evenly on each device for the sake of the mismatched gate drivers and the discrepancy of the electrical parameters of the devices and PCBs which has been analyzed in [53] and [101]. Especially, the dynamic voltage imbalance is difficult to eliminate due to the short switching time.

Passive snubbers are the simplest solution for voltage imbalance [101], but the snubber circuit parameters are not adaptive and the efficiency declines dramatically [102]. Master-slave switching pattern is another voltage balancing method, yet it results in large propagation delay in the system [103-106]. The active Miller clamping can also balance the voltage dynamically, but it still leads to extra energy loss [107] [108]. Additionally, the fast-switching process makes some conventional voltage balancing methods, such as adding gate chokes [109], no longer feasible for SiC systems.

AGD is a potential option for voltage balancing of series connected power devices. There are some literature reviews reporting a couple of AGD structures and algorithms to realize the voltage balance. In [110] and [111], the switching speed of series-connected devices can be controlled with an additional current source/sink. A novel AGD is proposed in [53] to eliminate the voltage imbalance caused by the discrepancy of the gate-to-ground capacitance. An auxiliary gate current is generated through the Miller capacitance to control the switching speed. A variable gate voltage technique is introduced in [112] to balance the transient voltage in virtue of controlling the dv/dt. However, the circuit schematics of the proposed variable gate voltage driver was absent in [112].

To validate that AGDs can balance the V_{ds} of series-connected SiC MOSFETs, a preliminary simulation is conducted with LTspice™. Two SiC MOSFETs C3M0065090D from Wolfspeed are connected in series and two gate drivers are connected to the gates of the two MOSFETs respectively. The high side is also a C3M0065090D. Its gate and source are shorted to prevent shoot-through. To emulate the discrepancy of electrical parameters, C_{gd} of MOSFET1 and MOSFET2 when V_{ds} =0V are 100 pF and 120 pF respectively. The dc-link voltage is 600 V and the maximum current is 79 A during the switching off transient. The gate driver is variable gate voltage AGDs which has the identical driver voltage profile in Fig. 17. The normal turn on/off voltage levels are V_{dr,on}=15V and V_{dr,off}=-5V.

Fig. 29 (a) shows the scenario without AGDs which means the gate driver is conventional two-level profile. V_{ds} of two gate drivers decreases from 15 to -5V directly. From Fig. 29 (a), without AGD, V_{ds} of two MOSFETs are unequal during the turn-off transient since the C_{gd} of the two devices is different. The maximum voltage difference is 55 V.

In contrast, another group of simulation study is conducted with the variable gate voltage AGD (V_{off,int} = -4.5 V and V_{off,int} = -5 V) when the other parameters remain the same. The dynamic V_{ds} curve of two MOSFETs is now matched as shown in Fig. 29 (b) and the voltage stress of MOSFET2 is effectively reduced. From Fig. 29 (b), the maximum voltage difference is reduced by ten times to 5.4 V. Table VI lists the key indices of the DPT of series-connected SiC MOSFETs. It shows that the imbalance of voltage stress and turn-off loss can be compensated with the variable gate voltage AGDs.
The key indices of the DPT simulation results for series-connected devices.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Without voltage balance</th>
<th>With voltage balance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device #1</td>
<td>Device #2</td>
<td>Device #1</td>
</tr>
<tr>
<td>Eoff 1019 μJ</td>
<td>988 μJ</td>
<td>998.3 μJ</td>
</tr>
<tr>
<td>dv/dt (on) 67.4 V/μs</td>
<td>60.3 V/μs</td>
<td>62.7 V/μs</td>
</tr>
<tr>
<td>dv/dt (off) 3.3 A/μs</td>
<td>3.3 A/μs</td>
<td>3.3 A/μs</td>
</tr>
<tr>
<td>Max AV 55 V</td>
<td>5.4 V</td>
<td></td>
</tr>
</tbody>
</table>

VI. CONCLUSION

The application of WBG devices can effectively reduce the energy loss while it also requires higher EMI noise immunity and lower circuit parasitics to avoid false triggering. In some scenarios, adjusting the slew rate is an evitable tradeoff. AGDs are invented to adjust the switching speed cycle by cycle actively to balance the power loss and side effects caused by fast switching speed.

In this paper, the fundamental mechanism of the slew rate control is demonstrated via analyzing the switching trajectory model of SiC devices. All the factors that can be utilized to adjust the switching speed are given. Based on the analysis of slew rate control mechanism, four categories of the state-of-the-art AGD methodologies are summarized. Accordingly, the available control strategies for the AGD are illustrated. Apart from EMI noise suppression, this paper also figures out three promising application scenarios of AGD technology including reliability enhancement, the current rebalancing of parallel-connected devices, and the voltage rebalancing of series-connected devices. The experimental and simulation study have validated the effectiveness of AGD in the aforementioned application scenarios.

REFERENCES


Crosstalk suppression in a 650-V GaN FET bridgeleg converter using 2012.

Electron. Motion Control Conf. (EPE/PEMC)


(ECCE)


IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS


[80] Busse, J. Erdman, R. J. Kerkman, S. D and G. Skibinski, “Beari-

[81]currents and their relationship to PWM drives,” in

[82]T. Bruckner and D. G. Holmes, “Optimal pulse width modulation for
dc link power converters,” in

[83]F. Blaabjerg, K. Ma and D. Zhou, “Power electronics and reliability in
green energy systems,” in

[84]X. Wang, Z. Zhao and L. Yuan, “Current sharing of IGBT modules in
circuit with parallel thermal balance,” in


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### Shuang Zhao
(S’13–M’20) was born in Zunyi, China. He received the B.S. and M.S. degrees in electrical engineering from Wuhan University, Wuhan, China, in 2012 and 2015, respectively. He received his Ph.D. degree in electrical engineering from University of Arkansas, Fayetteville, AR, USA, in 2019. In 2018, he was an intern at ABB US Corporate Research Center, Raleigh, NC, USA. Since 2019, he has been with Infineon Technologies, El Segundo, USA where he is currently a Sr. Application Engineer. His research interests include gate driver, electric vehicle, and distributed generation.

Dr. Zhao serves as a reviewer for multiple journals and conferences. He was a recipient of the Outstanding Presentation Award of the 2018 IEEE Applied Power Electronics Conference.

### Xingchen Zhao
(S’19) was born in Jiangsu, China, in 1993. He received the B.S. degree and M.S. degree in electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2015 and 2018, respectively. From 2018 to 2019, he was a research assistant with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR, USA.

His research interests include motor drive, multi-level inverters, and applications of wide bandgap devices.

### Yuqi Wei
(S’18) was born in Henan, China, in 1995. He received his B.S. degree in Electrical Engineering from Yunnan University, Hebei, China, in 2016, and his M.S. degree in Electrical Engineering from University of Wisconsin-Milwaukee (UWM), Wisconsin, U.S.A., in 2018. He received another M.S. degree in Electrical Engineering from Chongqing University, Chongqing, China, in 2019. He is currently working toward the Ph.D. degree at the University of Arkansas, Arkansas, U.S.A.

His current research interests include topology, modelling and control of DC/DC power converters and power factor correction AC/DC converters. He has published more than 20 peer-reviewed journal and conference papers. Mr. Wei serves as reviewer for IEEE Transactions on Industrial Electronics.

### Yue Zhao
(S’10–M’14–SM’20) received a B.S. degree in electrical engineering from University of Aeronautics and Astronautics, Beijing, China, in 2010, and a Ph.D. degree in electrical engineering from the University of Nebraska-Lincoln, Lincoln, USA, in 2014. He was an Assistant Professor in the Department of Electrical and Computer Engineering at the Virginia Commonwealth University, Richmond, USA, in 2014-2015. Since August 2015, he has been with the University of Arkansas, Fayetteville, USA, where he is currently an Assistant Professor in the Department of Electrical Engineering. His current research interests include electric machines and drives, power electronics, and renewable energy systems. He has 4 U.S. patents granted and co-authored more than 80 papers in refereed journals and international conference proceedings.

Dr. Zhao is an Associated Editor of the IEEE Transactions on Industry Applications and the IEEE Open Journal of Power Electronics. He also served as a Guest Associate Editor of IEEE Journal of Emerging and Selected Topics in Power Electronics. He is a member of Eta Kappa Nu. He was a recipient of 2018 U.S. National Science Foundation CAREER award. He was a recipient of the Best Paper Prize of the 2012 IEEE Transportation Electrification Conference and Expo (ITEC).

### H. Alan Mantooth
(S’83 – M’90 – SM’97 – F’09) received the B.S. and M.S. degrees in electrical engineering from the University of Arkansas in 1985 and 1986, respectively, and the Ph.D. degree from the Georgia Institute of Technology in 1990. He then joined Analog, a startup company in Oregon, where he focused on semiconductor device modeling and the research and development of modeling tools and techniques. In 1998, he joined the faculty of the Department of Electrical Engineering at the University of Arkansas, Fayetteville, where he currently holds the rank of Distinguished Professor. His research interests now include analog and mixed-signal IC design & CAD, semiconductor device modeling, power electronics, and power electronic packaging. Dr. Mantooth helped establish the National Center for Reliable Electric Power Transmission (NCREPT) at the UA in 2005. Professor Mantooth serves as the Executive Director for NCREPT as well as two of its centers of excellence: the NSF Industry/University Cooperative Research Center on Grid-connected Advanced Power Electronic Systems (GRAPES) and the Cybersecurity Center on Secure, Evolvable Energy Delivery Systems (SEEDS) funded by the U.S. Department of Energy. In 2015, he also helped to establish the UA’s first NSF Engineering Research Center entitled Power Optimization for Electro-Thermal Systems (POETS) that focuses on high power density systems for transportation applications. Dr. Mantooth holds the 21st Century Research Leadership Chair in Engineering. He serves as Immediate Past-President for the IEEE Power Electronics Society in 2019-20 and the Editor-in-Chief of IEEE Open Journal of Power Electronics. Dr. Mantooth is a Fellow of IEEE, a member of Tau Beta Pi and Eta Kappa Nu, and registered professional engineer in Arkansas.