Asymmetric sizing: an effective design approach for SRAM cells against BTI aging

Xuan Zuo and Sandeep K. Gupta
Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles, CA, USA
{xzuo, sandeep}@usc.edu

***Abstract*—The rate of aging of ICs is increasing with the continued reduction in feature sizes of devices. Bias temperature instability (BTI) is considered to be the major reliability hazard in nano-scale CMOS and causes stability degradation of SRAM cells. Some of the SRAM cells functioning properly at fabrication may fail during their desired lifetime due to aging. This will cause large aging quality loss. This paper addresses one key characteristic of aging, namely differential aging. This occurs due to the characteristics of data typically stored in SRAMs. After carefully studying the impact of differential aging on SRAM cells, we propose an asymmetric sizing approach for SRAM cells to maximize the probability of correct operation after m months of usage considering process variations. Our experiment results show that the asymmetric design can achieve much better aging quality loss (90x better) with optimal lifetime yield per area compared to the symmetric SRAM cell designs.**

I. Introduction

With the continued reduction in feature sizes of devices, the rate of aging of ICs is increasing [1]. Negative bias temperature instability (NBTI) is considered to be the major reliability hazard in nano-scale CMOS and causes threshold voltage (Vth) degradation for a PMOS transistor when negative bias voltage is applied at the transistor's gate. Positive bias temperature instability (PBTI), which increases Vth of NMOS transistors, is considered as a second-order effect in poly technology but is a prominent aging mechanism in high-k/metal technologies [2]–[5]. Various aging models have been proposed (e.g., [6]–[8]) and all capture the degradation of threshold voltage as a function of initial threshold voltage, supply voltage, duty cycle, and temperature. The impact of aging on logic circuits and SRAMs has been widely studied [3], [9], [10]. NBTI and PBTI cause timing degradation in logic circuit and timing as well as stability degradation in SRAM cells [3], [11]. The aging degradation will lead to failure of digital chips after being shipped to customers, resulting in quality loss of the shipped chips and reduction in the lifetime of chips. In this paper, we focus on SRAMs. Since stability is a big problem in SRAM, we primarily focus on static noise margin (SNM) degradation in this paper.

To reduce aging quality loss, a new test method is needed to detect SRAMs that will fail due to aging during the desired lifetime before the chips are shipped to customers. However, this will decrease yield as more chips will be discarded. A much more appealing solution is to design the SRAM cells against aging to increase its lifetime.

Certain SRAM design strategies have been proposed in the literature to mitigate or compensate the effects of aging. At architecture level, existing design techniques for aging mitigation include workload balancing between different cores [12], proactive use of spares in SRAMs [13], periodically flipping data bits stored in SRAMs [14], and shutting down idle cache blocks [15]. At circuit level, the adaptive body bias method is adopted in [16]. A standalone threshold voltage sensing circuit is used to estimate degradation and the required body bias voltage is generated accordingly to compensate for NBTI aging. However, it only considers NBTI aging effect and the body bias voltage is generated based on the threshold degradation of a pMOS under full stress condition. It fails to consider different duty cycles for different transistors in an SRAM cell, thus does not take into account an important characteristic of aging, namely differential aging.

Differential aging occurs due to the characteristics of data typically stored in SRAMs and has been recognized in [3], [10], but its implications on design have not been extensively studied. The classic approach for designing an SRAM cell is to maximize SNM. However, after m months of usage, due to the differential aging, one of the SNMs decreases more severely. Differential aging introduces new challenges for SRAM design. *In this paper, we will focus on the differential aging at circuit level to develop an approach for SRAM cell design that maximizes the probability of correct operation after m months of usage of SRAM cells.*

Meanwhile with the continued scaling in the feature sizes of devices, the increased density and leakage necessitate the ultra-low power supply operation for SRAMs to achieve low power consumption. After carefully studying the conventional 6T cell, 8T cell and 10T cell designs and comparing their various metrics, we found that the 10T Schmitt Trigger (ST) SRAM cells [17] have high SNMs and high tolerance to process variations. These cells can achieve the lowest failure probability for ultra-low power supply operation. Also they do not require any changes the conventional SRAM architecture used for 6T cells. Thus we choose 10T ST cell structure as our baseline design.

In this paper, we propose an effective design approach for SRAM cell to maximize the probability of correct operation after m months of usage considering process variation for operation at low power supply voltages.

The rest of the paper is organized as follows. In Section II we introduce differential aging and analyze the impact of BTI aging on SRAM cell stability. We propose our design approach for aging resistant SRAM cell in Section III. In Section IV, we demonstrate the effectiveness of our new design via extensive

978-1-5090-4482-5/17/$31.00 ©2017 IEEE

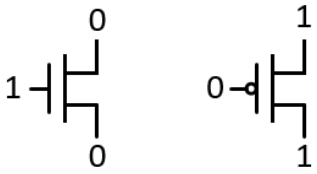


Figure 1: Stress state for NMOS transistor and PMOS transistor.

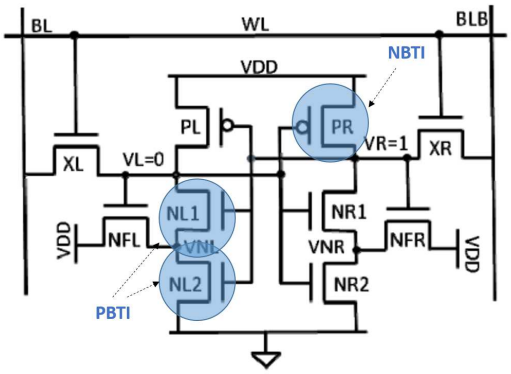


Figure 2: 10T ST SRAM cell.

simulations. Finally, we present our conclusions in Section V.

II. BTI AGING AND THE IMPACT ON SRAM CELLS

A. Differential aging

BTI is the most prominent aging effect in nano-scale CMOS. NBTI causes Vth degradation of stressed PMOS and PBTI causes Vth increase of stressed NMOS. The stress pattern for NMOS and PMOS are shown in Fig. 1. After the stress is removed, the transistor partially recovers from the degradation. Hence, in the long term, the threshold degradation caused by BTI aging is highly dependent on the percentage of time that a transistor is stressed, i.e., the duty cycle. Due to different duty cycles, different transistors in a circuit age differently. We refer to this effect as *differential aging*.

In a typical 10T ST SRAM cell as shown in Fig. 2, NL1, NL2, NR1 NR2, PL and PR, these six transistors of the cross-coupled inverters are periodically under stress depending on the value stored in the SRAM cell. When a value "0" is stored in the cell, NL1, NL2 and PR are stressed and suffer aging degradation, while NR1, NR2 and PL are stressed when a value "1" is stored in the cell. Access transistors (XL and XR) are only under stress when word line is selected. Thus the access transistors experience negligible BTI degradation because of their short stress time through SRAM's lifetime. Feedback transistors NFL and NFR are NMOS transistors and their drain terminals are always connect to VDD. Thus they do not suffer BTI degradation.

It has been widely studied that the logic values stored in SRAM array are not symmetric, i.e., the SRAM cell stores values 0 and 1 with different probabilities through its lifetime. In cache, the dominant logic bit value "0" is stored approximately 75% [15], [18] of the time. Thus various transistors in an SRAM cell undergo different stress conditions. For a cell that stores "0" most of the time as shown in Fig. 2, NL1, NL2 and PR suffer more significant aging degradation compared to its NR1, NR2 and PL.

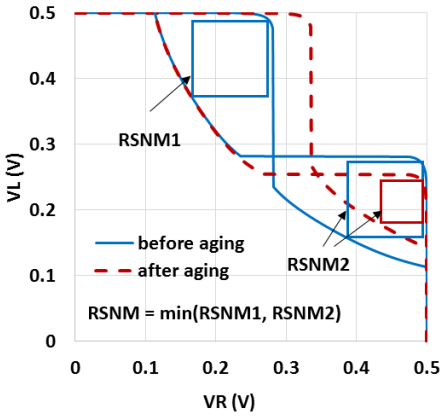


Figure 3: The butterfly curve of a 10T ST SRAM cell indicating RSNM before and after aging.

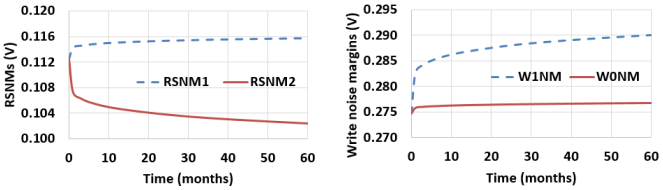
B. The impact of aging on the noise margins

SRAMs' read and write stability can be measured by the read static noise margin (RSNM) and write noise margin (WNM) respectively. The RSNM is defined as the size of the largest of the squares that can be fit into both the openings of the butterfly curve of an SRAM cell. As shown in Fig. 3, RSNM1 and RSNM2 denote the read noise margins of an SRAM cell, where RSNM1 is the side of the largest square that can be fit into the upper opening of the butterfly curve, and RSNM2 is the side of the largest square that can be fit into the lower opening of the butterfly curve. RSNM is the minimum of RSNM1 and RSNM2. The WNM is used as a metric of write stability. It is defined as the width of the smallest embedded square between two DC transmission curves of the two inverters of an SRAM cell.

To design the SRAM cell resistant to BTI aging, the impact of aging on SRAM's read and write noise margins need to be carefully studied. In this paper, all experiments are conducted using Predictive Technology Model (PTM) 32nm library [19]. The NBTI model proposed in [6] is adopted. For 32nm high-k process, as reported in [3], [4], PBTI causes the same magnitude of Vth shift to NMOS as NBTI does for PMOS.

As stated earlier, transistors in the SRAM cell undergo different stress conditions, thus they suffer different amount of Vth degradation. The differential aging is reflected on the noise margins of SRAM cells. In Fig. 3, the blue solid curves are the butterfly curve before aging and the red dashed curves are the butterfly curves after aging. Before aging, RSNM1 and RSNM2 are equal because of the symmetric strength of the cell. However, when value "0" is always stored in the cell, NL1, NL2 and PR suffer full stress condition. After differential aging, RSNM2 degrades significantly, while RSNM1 improves. Thus, RSNM decreases after aging.

Fig. 4 shows RSNM1, RSNM2, write noise margin for writing value "1" (W1NM), and write noise margin for writing value "0" (W0NM) of a 10T ST SRAM cell through its desired lifetime. The supply voltage is 0.5V and the SRAM cell is sized with the same ratio as in [20]. In this paper, we assume



(a) (b)

Figure 4: (a) Read noise margins, and (b) write noise margins through lifetime for a symmetric 10T ST SRAM cell when value "0" is stored in the cell for 75% of the time.

the desired lifetime is 5 years and value "0" is stored in the cell for 75% of its lifetime [15], [18]. We can see that after 60 months of usage, RSNM2 degrades severely while RSNM1 improves slightly. This is easy to explain since when value "0" is stored in the cell for more time than value "1", NL1, NL2 and PR suffer more degradation than NR1, NR2 and PL. Thus the pull down is weaker in the left part of the cell and the relative stresses of the pull down network and access transistor decreases more than the right part. Pull up becomes weaker in the right part of the SRAM cell.

During read operation, the voltage division between access transistor and pull down transistors decides V_{OL}. The switching threshold voltage (VM) of the inverter is determined by the relative stresses of the pull up and pull down networks. Therefore, VM of the left inverter of the cell increases, while VM of the right inverter decreases. V_{OL} of the left inverter increases more than that of the right inverter. The decrease of VM of the right inverter and increase of V_{OL} of the left inverter cause RSNM2 to decrease significantly, and make it easier to corrupt the stored value in the cell during read operation. The relative amount of shift of VM of the left inverter and V_{OL} of the right inverter decides whether RSNM1 increases or decreases. Clearly, if value "0" is stored for more time than value "1" in the SRAM cell, RSNM2 will degrade more significantly than RSNM1.

Write noise margins increase since both pull up transistors become weaker after aging. The new value is easy to write into the cell because the relative stresses between access transistor and pull up transistor increases.

III. Design Approach

The conventional design goal for SRAM cell is to increase the read and write stability to maximize the yield. The classic design approach is to optimize RSNM and WNM at the time of fabrication, i.e., at m=0 months. However, BTI aging causes stability degradation of the SRAM cell. Furthermore, according to Section II, each transistor in the SRAM cell suffers different amount of threshold degradation caused by differential aging. The noise margin degradation is not symmetric, i.e., one of the read noise margin decreases more severely after m months of usage. Differential aging introduces new challenges for SRAM design.

Before discussing our design approach, we need to define some terms.

Yield of an SRAM array: the probability that an SRAM array is able to be function correctly after fabrication.

Lifetime yield of an SRAM array: the probability that an SRAM array is able to be function correctly through its desired lifetime of m months.

Aging quality loss of an SRAM array: The probability that an SRAM array functioning properly at fabrication fails during its desired lifetime due to aging.

Failure rate of an SRAM cell (P_{fail}^{cell}): The probability that an SRAM cell fails at fabrication.

Aging failure rate of an SRAM cell ($P_{fail,aging}^{cell}$): The probability that an SRAM cell functioning properly at fabrication fails during its desired lifetime due to aging.

Then for an SRAM array consisting of N cells,

$$\text{Lifetime yield} = (1 - P_{fail}^{cell})^N (1 - P_{fail,aging}^{cell})^N$$

$$\text{Aging quality loss} = 1 - (1 - P_{fail,aging}^{cell})^N \quad (1)$$

In practice, aging quality loss is measured by defective part per million (DPPM). **DPPM** of the SRAM array = Aging quality loss $\times 10^6$. To ensure customer satisfaction, the DPPM should below a small value which we call the target DPPM. Based on these observations, the SRAM cell must be designed to maximize that noise margin which is more likely to lead to failure after m month of usage. That is determined by the initial value of the noise margin as well as the amount of degradation caused by aging. Our design goal is to optimize the lifetime yield of SRAM array under a given target DPPM instead of the yield at fabrication. Usually, the target DPPM is 50 [21], i.e., no more than 50 chips per million can fail due to aging after the chips are shipped to customers. We propose asymmetric sizing approach for the SRAM cell to achieve this design goal.

Our general approach for designing SRAM cell resistant to BTI aging is as follows: *Step 1. Identify the impact of aging on SRAM's stability. Step 2. Study the relationship between the size of each transistor and the noise margins. Step 3. Study the relationship between the size of each transistor and read access time. Step 4. Based on the layout of SRAM cell, develop a formula for cell area. Step 5. Based on the analysis of steps 1-4, find the optimal sizes of transistors to maximize the minimum noise margin after aging in the nominal case. Step 6. Analyze the impact of aging on noise margins for SRAM cells under process variations. Step 7. Carry out a comprehensive evaluation of the new design.*

We have studied the noise margins of SRAMs through the desired lifetime in the presence of differential aging in Section II. We find that write noise margins increase over the lifetime because both pull up transistors are weakened by aging. RSNM2 degrades much more severely than RSNM1 when the value "0" is stored in the SRAM cell for 75% of its lifetime. According to simulation results and literature [3], [9], SRAM read failure is more likely to occur and differential aging degrades RSNM2 more. *Thus to prevent the noise margin degradation caused by aging, we focus on maximizing RSNM2.*

A. The relationship between noise margins and the transistor sizes in the nominal case

To fully understand how to size the transistors to optimize the lifetime yield, we study the relationship of the noise margins and the size of each transistor. Fig. 5 (a) to (g) show the noise margins when only the size of a single transistor in the SRAM cell is changed. Since we focus on RSNM2, all the transistors whose sizing impact on RSNM2 of the cell, including XL, NFR, NL1, NL2, NR1, NR2 and PR, are shown. Fig. 5(h) shows the relationship between the access time and the transistor sizes in the SRAM cell to help decide the optimal size of each transistor, where TR0 indicates the access time for read 0 and TR1 indicates the access time for read 1. The access time is determined by the time required for the cell to achieve the minimum voltage drop on the bit lines required by the sense amplifier.

Our design objective is to increase RSNM2 to reduce the noise margin degradation caused by aging. In Table I, we list all the transistors whose sizing impact RSNM2 of the SRAM cell as well as how to increase RSNM2 via sizing. The reasons why RSNM2 can be improved through sizing of each transistor are also presented in the table along with the negative effects. The curves that provide the required information of the sizing are shown in the parentheses in each table entry. As shown in Table I, RSNM2 can be increased by increasing the size of NFR, NL1, NL2, PR and/or decreasing the size of XL, NR1 and NR2. However, each approach has some negative effects on stability or access time, except increasing the size of NFR. For example, write noise margins and access time are sensitive to the size of access transistor as shown in Fig. 5 (a) and (h) respectively. Decreasing the size of XL will decrease W0NM and increase access time dramatically. Increasing the size of pull down transistor NL1 and NL2 will decrease RSNM1, and thus reduce the yield at fabrication. Although decreasing the size of pull down transistors of the right inverter NR1 and NR2 will increase RSNM2, RSNM1 will decrease significantly and the access time for read 1 will increase. Sizing up pull up transistor PR will decrease W1NM dramatically. In contrast, increasing the size of NFR has no negative impact on other noise margins based on Fig. 5(b) and access time based on Fig. 5(h). *Thus we choose to increase the size of NFR.*

B. The optimal sizes of transistors in SRAM cell in the nominal case

Let us start with the nominal case, where we ignore process variations. Our design goal is to design the SRAM cell resistant to aging, i.e., no stability degradation caused by aging through the lifetime. According to the analysis in Section II and III (A), differential aging causes RSNM2 degradation and sizing up single transistor NFR can improve RSNM2 without any negative effect on other noise margin parameters and access time. We could properly size NFR transistor to ensure that RSNM does not reduce through lifetime.

Fig. 6 shows the relationship between the read noise margins and the size of NFR, for different lifetimes. The optimal sizes of NFR for different lifetimes are indicated by the dashed

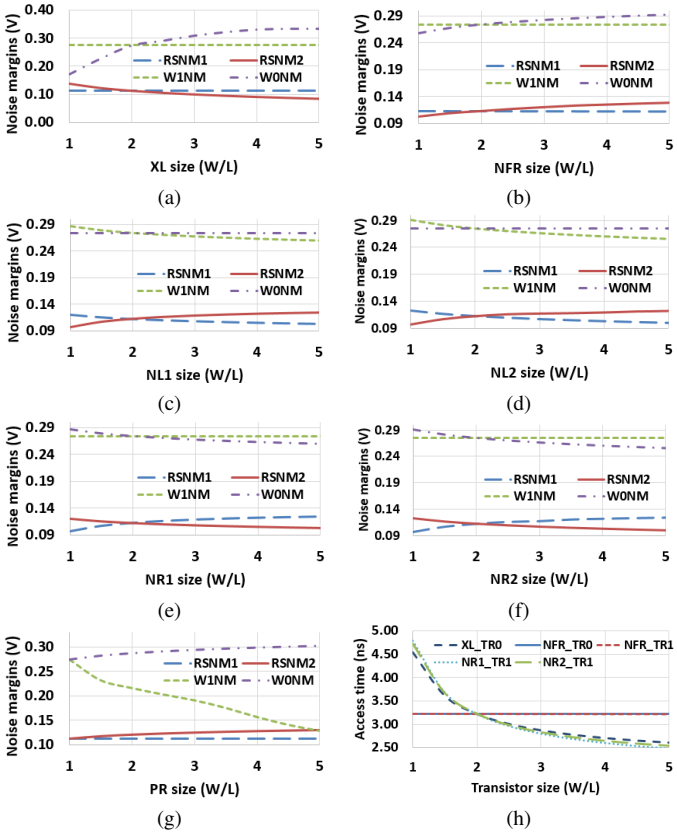


Figure 5: Noise margins of the SRAM cell versus the sizes of (a) XL (b) NFR (c) NL1 (d) NL2 (e) NR1 (f) NR2 (g) PR. (h) Access time of the SRAM cell versus the transistor sizes.

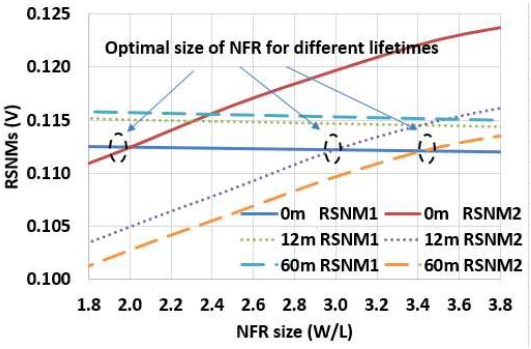


Figure 6: Optimal sizes of NFR.

circle. After the desired lifetime, the degraded RSNM2 should be no less than the minimum noise margin at fabrication, i.e., RSNM1, to prevent aging quality loss. In terms of area efficiency, NFR should not be oversized. Thus the optimal size of NFR is the size when RSNM2 after desired lifetime is equal to RSNM1 at fabrication as indicated in Fig. 6.

C. The impact of aging on SNM under process variations

In the above section, we have identified the optimal size of the transistors in SRAM cell in the nominal case. We need to study the impact of aging on noise margins for SRAM cells under process variations to find out whether the optimal size in the nominal case can achieve the optimal lifetime yield. We

Table I: All the transistors whose sizing impact RSNM2 of a 10T ST SRAM cell

Transistors having impact on RSNM2	How to increase RSNM2	Reason	Side effect except area overhead
XL	Decrease size (Fig. 5(a))	Decrease V_{OL} of the left inverter	Decrease W0NM and increase TR0 dramatically (Fig. 5 (a) and (h))
NFR	**Increase size (Fig. 5(b))**	**Increase VM of the right inverter**	**None (Fig. 5 (b) and (h))**
NL1	Increase size (Fig. 5(c))	Decrease V_{OL} of the left inverter	Decrease RSNM1 (Fig. 5(c))
NL2	Increase size (Fig. 5(d))	Decrease V_{OL} of the left inverter	Decrease RSNM1 (Fig. 5(d))
NR1	Decrease size (Fig. 5(e))	Increase VM of the right inverter	Decrease RSNM1 and increase TR1 significantly (Fig. 5 (e) and (h))
NR2	Decrease size (Fig. 5(f))	Increase VM of the right inverter	Decrease RSNM1 and increase TR1 significantly (Fig. 5 (f) and (h))
PR	Increase size (Fig. 5(g))	Increase VM of the right inverter	Decrease W1NM dramatically (Fig. 5(g))

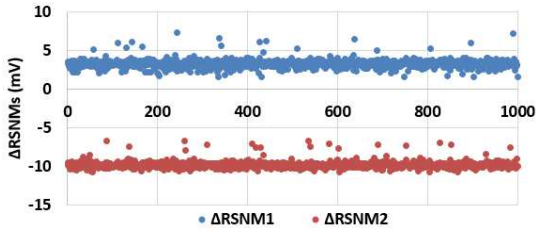


Figure 7: The read noise margin changes after 60 months usage for 1000 monte carlo SRAM cell instances with process variations.

generate 1000 Monte Carlo SRAM cell instances with process variations. The RSNMs of the 1000 instances at fabrication and after 60 months of usage are extracted, assuming that all cells store value "0" 75% of the time. Fig. 7 shows the changes of RSNM1 and RSNM2 for all 1000 instances, indicated by ΔRSNM1 and ΔRSNM2 respectively. We can see that the noise margin changes caused by aging are almost the same for different instances and are equal to those in the nominal case. Thus the optimal size for the nominal case can be used as the optimal size for all instances with process variations.

IV. Experimental evaluation

To demonstrate the effectiveness of our asymmetric sizing approach, the lifetime yield per area and DPPM of SRAM using our 10T ST asymmetric SRAM cells are compared with SRAM using symmetric 10T ST SRAM cells. For comparison, the default symmetric cell is sized in the same ratio as the cell in [20]. The lifetime yield and DPPM are calculated using Eq.1 for 2MB SRAM arrays. We use the probability collective method, a variant of the importance sampling method, proposed in [22] to estimate the failure rate and aging failure rate. In our experiments, we assume the desired lifetime for SRAM m is 60 months. 32nm high-k metal gate PTM library is used for our simulation. To model process variations, we assume that Vth of each transistor follows identical and independent Gaussian distributions with a standard deviation approximately equal to 10% of the nominal Vth value. To demonstrate that the 10T ST cell is suitable for low power operation, we set the supply voltage to 0.5V.

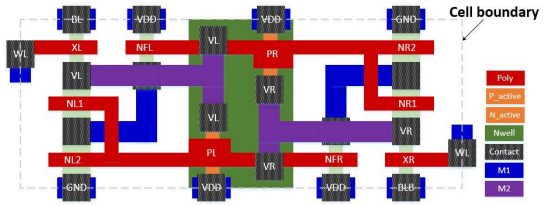


Figure 8: Layout of 10T ST SRAM cell.

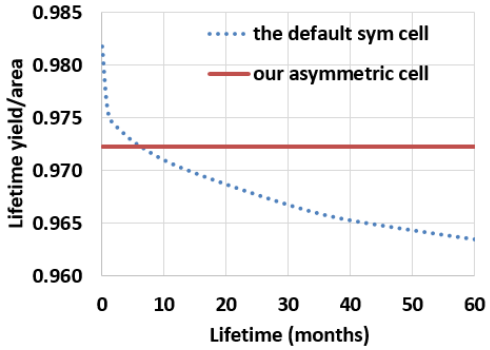


Figure 9: Lifetime yield per area comparison for 2MB SRAM arrays when value "0" is stored in all cells for 75% of the time.

A. 10T ST SRAM cell layout

To compare the lifetime yield per area of SRAM array, the area of SRAM cell must be estimated. Fig. 8 shows the layout of 10T ST SRAM cell [17]. Based on the layout and the design rule, we can derive a formula for area in terms of transistor sizes. We set the area of the default symmetric cell to 1 and then normalize the area of other cells to calculate the lifetime yield per area.

B. Lifetime yield and DPPM comparison

The lifetime yield per area of the SRAM using our new 10T ST asymmetric cell and the default symmetric cell are plotted in Fig. 9. We can see that the lifetime yield of the symmetric design decreases significantly due to the cell failures caused by aging. As shown in Fig. 10, the default design has a very large DPPM value, larger than 10000 which will cause significant customer dissatisfaction. Our proposed asymmetric design has a very low aging quality loss with a small area overhead. In particular, our design's DPPM is less than 10 for a 2MB SRAM array when "0" is stored in all cells for 75% of the time. Also the overall lifetime yield per area of the asymmetric design is significantly higher than that of the default design.

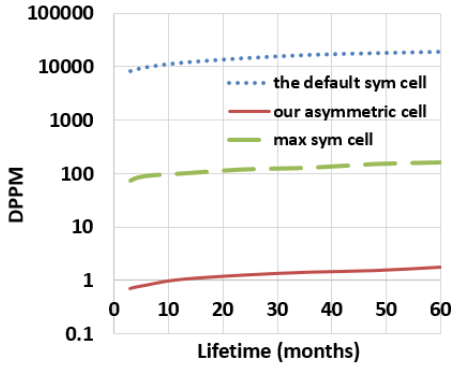


Figure 10: DPPM comparison for 2MB SRAM arrays when value "0" is stored in all cells for 75% of the time.

To demonstrate the advantage of our asymmetric sizing approach, we have studied symmetric SRAM cells with various sizes for comparison. Although the aging quality loss can be reduced by using larger transistors in symmetric cells, the area overhead is too large and the lifetime yield per area typically decreases dramatically. Thus we have simulated various symmetric cells under an area budget. The minimum DPPM of SRAM among all the symmetric cells is shown by the green dashed line in Fig. 10, which is larger than our target DPPM 50 and unacceptable. Thus, against differential aging, asymmetric sizing approach must be used to achieve the desired DPPM and optimal lifetime yield per area.

Experiment results also shows that asymmetric design has even larger advantages for SRAM cells with larger duty cycle, i.e., cells that store value "0" most of the time, since symmetric cells suffer more aging degradation in those cases.

One thing to notice is that, although in reality, the data is not always stored for 75% of the time in all the cells, sizing up NFR has no negative effect on stability and access time except with a small area overhead. The SRAM array using asymmetric cells will always lead to better DPPM under the existence of differential aging. With accurate information about data patterns, we can find optimal size for various SRAM cells against aging using our asymmetric design approach to achieve target DPPM and optimal lifetime yield per area.

V. Conclusion

In this work, we study the impact of aging on SRAM stability in combination with process variations. We have proposed a new design approach for SRAM cells to combat differential aging. We evaluate our new design along with various symmetric designs in terms of lifetime per area and DPPM. We demonstrate that our design approach provides optimal SRAM cell design. The asymmetric design is superior than the conventional symmetric designs with a very low aging quality loss and optimal lifetime yield per area.

References

[1] M. A. Alam, "A critical examination of the mechanics of dynamic nbti for pmosfets," in *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International*, pp. 14–4, IEEE, 2003.

[2] C. Liu *et al.*, "Experimental study on bti variation impacts in sram based on high-k/metal gate finfet: From transistor level vth mismatch, cell level snm to product level vmin," in *2015 IEEE International Electron Devices Meeting (IEDM)*, pp. 11–3, IEEE, 2015.

[3] A. Bansal *et al.*, "Impact of nbti and pbti in sram bit-cells: Relative sensitivities and guidelines for application-specific target stability/performance," in *Reliability Physics Symposium, 2009 IEEE International*, pp. 745–749, IEEE, 2009.

[4] S. Natarajan *et al.*, "A 32nm logic technology featuring 2 nd-generation high-k+ metal-gate transistors, enhanced channel strain and 0.171μm 2 sram cell size in a 291mb array," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, pp. 1–3, IEEE, 2008.

[5] J. Lin, A. Oates, and C. Yu, "Time dependent vccmin degradation of sram fabricated with high-k gate dielectrics," in *2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual*, pp. 439–444, IEEE, 2007.

[6] S. Bhardwaj, W. Wang, R. Vattikonda, Y. Cao, and S. Vrudhula, "Predictive modeling of the nbti effect for reliable design," in *Custom Integrated Circuits Conference, 2006. CICC'06. IEEE*, pp. 189–192, IEEE, 2006.

[7] V. B. Kleeberger *et al.*, "A compact model for nbti degradation and recovery under use-profile variations and its application to aging analysis of digital integrated circuits," *Microelectronics Reliability*, vol. 54, no. 6, pp. 1083–1089, 2014.

[8] C. Ma *et al.*, "Universal nbti compact model for circuit aging simulation under any stress conditions," *Device and Materials Reliability, IEEE Transactions on*, vol. 14, no. 3, pp. 818–825, 2014.

[9] T.-H. Kim, W. Zhang, and C. H. Kim, "An sram reliability test macro for fully-automated statistical measurements of v min degradation," in *2009 IEEE Custom Integrated Circuits Conference*, pp. 231–234, IEEE, 2009.

[10] A. Bansal *et al.*, "Impacts of nbti and pbti on sram static/dynamic noise margins and cell failure probability," *Microelectronics reliability*, vol. 49, no. 6, pp. 642–649, 2009.

[11] V. Reddy *et al.*, "Impact of negative bias temperature instability on digital circuit reliability," *Microelectronics Reliability*, vol. 45, no. 1, pp. 31–38, 2005.

[12] J. Abella, X. Vera, and A. Gonzalez, "Penelope: The nbti-aware processor," in *40th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO 2007)*, pp. 85–96, IEEE, 2007.

[13] J. Shin *et al.*, "A proactive wearout recovery approach for exploiting microarchitectural redundancy to extend cache sram lifetime," in *ACM SIGARCH Computer Architecture News*, vol. 36, pp. 353–362, IEEE Computer Society, 2008.

[14] S. V. Kumar, K. Kim, and S. S. Sapatnekar, "Impact of nbti on sram read stability and design for reliability," in *7th International Symposium on Quality Electronic Design (ISQED'06)*, pp. 6–pp, IEEE, 2006.

[15] A. Ricketts *et al.*, "Investigating the impact of nbti on different power saving cache strategies," in *Proceedings of the conference on design, automation and test in Europe*, pp. 592–597, European Design and Automation Association, 2010.

[16] H. Mostafa, M. Anis, and M. Elmasry, "Adaptive body bias for reducing the impacts of nbti and process variations on 6t sram cells," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 58, no. 12, pp. 2859–2871, 2011.

[17] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mv robust schmitt trigger based subthreshold sram," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, 2007.

[18] Y.-J. Chang and F. Lai, "Dynamic zero-sensitivity scheme for low-power cache memories," *IEEE Micro*, vol. 25, no. 4, pp. 20–32, 2005.

[19] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45 nm early design exploration," *Electron Devices, IEEE Transactions on*, vol. 53, no. 11, pp. 2816–2823, 2006.

[20] J. P. Kulkarni and K. Roy, "Ultralow-voltage process-variation-tolerant schmitt-trigger-based sram design," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 20, no. 2, pp. 319–332, 2012.

[21] F. M. Gonçalves, I. C. Teixeira, and J. Teiceira, "Realistic fault extraction for high-quality design and test of vlsi systems," in *Defect and Fault Tolerance in VLSI Systems, 1997. Proceedings., 1997 IEEE International Symposium on*, pp. 29–37, IEEE, 1997.

[22] F. Gong, S. Basir-Kazeruni, L. Dolecek, and L. He, "A fast estimation of sram failure rate using probability collectives," in *Proceedings of the 2012 ACM international symposium on International Symposium on Physical Design*, pp. 41–48, ACM, 2012.