An Energy-Efficient CMOS Dual-Mode Array Architecture for High-Density ECoG-Based Brain-Machine Interfaces

Omid Malekzadeh-Arasteh, *Student Member, IEEE*, Haoran Pu, *Student Member, IEEE*, Jeffrey Lim, *Student Member, IEEE*, Charles Yu Liu, An H. Do, Zoran Nenadic, *Senior Member, IEEE*, and Payam Heydari, *Fellow, IEEE*

***Abstract*—This article presents an energy-efficient electrocorticography (ECoG) array architecture for fully-implantable brain machine interface systems. A novel dual-mode analog signal processing method is introduced that extracts neural features from high-γ band (80–160 Hz) at the early stages of signal acquisition. Initially, brain activity across the full-spectrum is momentarily observed to compute the feature weights in the digital back-end during full-band mode operation. Subsequently, these weights are fed back to the front-end and the system reverts to base-band mode to perform feature extraction. This approach utilizes a distinct optimized signal pathway based on power envelope extraction, resulting in 1.72$\times$ power reduction in the analog blocks and up to 50$\times$ potential power savings for digitization and processing (implemented off-chip in this article). A prototype incorporating a 32-channel ultra-low power signal acquisition front-end is fabricated in 180 nm CMOS process with 0.8 V supply. This chip consumes 1.05 μW (0.205 μW for feature extraction only) power and occupies 0.245 mm^2 die area per channel. The chip measurement shows better than 76.5-dB common-mode rejection ratio (CMRR), 4.09 noise efficiency factor (NEF), and 10.04 power efficiency factor (PEF). In-vivo human tests have been carried out with electroencephalography and ECoG signals to validate the performance and dual-mode operation in comparison to commercial acquisition systems.**

***Index Terms*—Analog signal processing, brain signal acquisition, brain-machine interfaces, electrocorticography (ECoG), feature extraction, high-density array, ultra-low power.**

I. Introduction

APPROXIMATELY 330,000 people are living with chronic spinal cord injury (SCI) in the US alone, and currently there are no biomedical approaches capable of restoring motor function after SCI. Recent advances in neurophysiology and nanoscale electronics have made it possible to realize fully implantable brain-machine interfaces (BMIs) for medical applications. Large-scale miniaturized ECoG arrays are considered to be a promising signal platform for fully implantable BMIs due to their signal stability, high signal-to-noise ratio (SNR) and spatial resolution [1], [2]. However, these favorable attributes often come at the expense of excessive power consumption. Therefore, energy efficient BMI architectures inspired by prior studies of human motor control are of high interest to make such invasive BMIs a clinical reality.

It is perceived that the primary motor cortex, M1, encodes high-level kinematic parameters for upper and lower extremity movements (i.e., duration and speed), and interacts with subcortical/spinal networks that execute low-level motor control (i.e., muscle activation or movement trajectories) [3]–[7]. High spatiotemporal resolution ECoG recordings from M1 contain rich movement information related to upper and lower extremities in γ-band [8]–[11]. In particular, high-γ (80-160 Hz) band exhibits consistent changes in power levels during movement and idle states [3], and thus these patterns can be utilized as the central neural features to enable practical BMIs for prosthetic control in SCI patients.

Shown in Figs. 1(a)–(b) are general block diagrams of the analog- and digital-based multi-channel architectures, each comprised of an *N*-channel front-end, a multiplexer, and a mixed-signal and digital back-end.

The analog-based architecture utilizes analog signal processing (ASP) to form an *M*-element neural-feature vector based on spectral decomposition [12]–[14]. Although this approach reduces the signal bandwidth and lowers the sampling rate (f_s) of

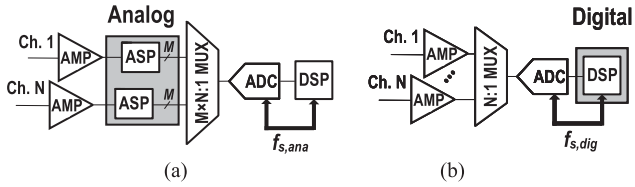


Fig. 1. Existing architectures for multi-channel feature extraction in brain-machine interfaces based on (a) analog and (b) digital signal processing.

Manuscript received June 24, 2019; revised September 1, 2019, October 29, 2019, and December 5, 2019; accepted December 19, 2019. Date of publication December 31, 2019; date of current version March 27, 2020. This work was supported by the National Science Foundation awards #1646275 and #1446908. This paper was recommended by Associate Editor Prof. Omer Oralkan. *(Corresponding author: Omid Malekzadeh-Arasteh.)*

O. Malekzadeh-Arasteh, H. Pu, and P. Heydari are with the Department of Electrical Engineering and Computer Science, University of California, Irvine, CA 92697 USA (e-mail: omalekza@uci.edu; haoranp1@uci.edu; payam@uci.edu).

J. Lim and Z. Nenadic are with the Department of Biomedical Engineering, University of California, Irvine, CA 92697 USA (e-mail: limj4@uci.edu; znenadic@uci.edu).

C. Y. Liu is with the Department of Neurosurgery, University of Southern California, Los Angeles, CA 90033 USA (e-mail: cliu@usc.edu).

A. H. Do is with the Department of Neurology, University of California, Irvine, CA 92697 USA (e-mail: and@uci.edu).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2019.2963302

the mixed-signal and digital back-ends, it has several limitations at the circuit- and architecture-level. For example, an analog neural spectral-processing integrated circuit is implemented in [12] for $M = 4$ that amplifies and processes neuronal activity with variable bandwidth and power filtering characteristics. The signal chain includes a power-hungry tunable heterodyning amplifier based on a dual-nested chopper architecture, which suffers from a limited input impedance and requires an anti-alias filter. An analog energy extractor for local field potential is introduced in [13] for $M = 6$, which allows for a compact design and low power consumption. However, this approach offers limited degree of freedom to control the selectivity and sensitivity of the transfer characteristics of the filters used as part of the energy extractor. [14] reports a single-channel neural recording prototype, capable of extracting sub-banded energy across four ($M = 4$) different frequency bands. This architecture utilizes a power-hungry variable gain amplifier to satisfy the dynamic range and settling requirements of discrete-time signal conditioning and digitization. To avoid anti-aliasing in the sampled-data system, it allows for limited tuning of each sub-band parameters which are controlled by the clock frequency. Moreover, a complex switching matrix can be employed to share the bulky energy extractors in multi-channel acquisition, which is not amenable to large-scale neural recording.

The digital-based multi-channel architecture implements the neural feature extraction entirely in the digital back-end [15], as shown in Fig. 1(b). This approach requires higher f_s compared to the analog-based architecture due to a significantly larger bandwidth of raw ECoG signal, resulting in higher dynamic power dissipation. Although power and clock gating techniques can be applied to reduce the power consumption, it is still advantageous to avoid the data-processing power bottleneck by limiting the signal bandwidth before multiplexing/digitization.

Inspired by our work in [3], this paper presents a scalable dual-mode array architecture which exploits ultra-low power (ULP) ASP to extract relevant neural features of ECoG signals to enable prosthetic control in implantable BMIs. The rest of this paper is organized as follows. Section II discusses the system-level specifications and implications of neural feature extraction. Section III presents the proposed dual-mode array architecture. Section IV describes the circuit design and analysis. Section V presents experimental results including electrical and human neurological measurements. Section VI concludes the paper.

II. System-Level Considerations and Implications

In this section, we discuss important challenges in state-of-the-art ECoG-based implantable BMIs and investigate the system-level specifications and implications.

First, the input-referred integrated RMS noise from the front-end amplifier should fall below the cortical background noise ($\sim$5–10 μV) to allow for high-fidelity signal acquisition [16]. Second, to reduce the power-line 50/60-Hz interference, the common-mode rejection ratio (CMRR) of the amplifier is desired to be larger than 70 dB [17]. Third, for multi-channel acquisition with a common-reference electrode that has comparable impedance to channel electrode's, the input impedance must be large enough ($>>1$ MΩ) to avoid any signal attenuation and CMRR degradation. Finally, to satisfy the thermal dissipation requirement in the vicinity of the brain, it is crucial to reduce the overall power consumption of the multi-channel neural recording to keep the temperature increase below 1° C.

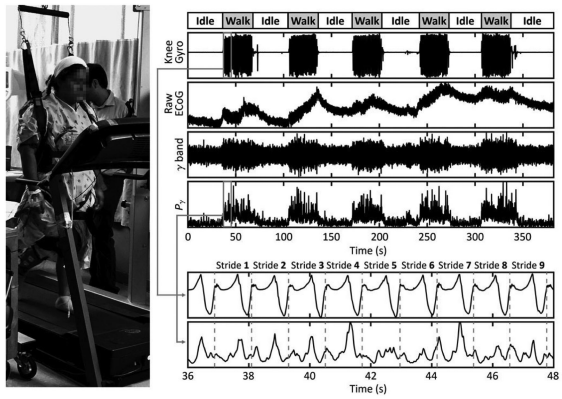


Fig. 2. Example of the experimental setup and signal processing steps used for recording of motor cortical activity with ECoG grid during a causal walking task. Data from knee gyroscope, ECoG data in its raw, γ-band filtered and power envelopes (P_γ) are shown. A close-up of P_γ and knee gyro signals is illustrated for comparison during individual gait cycles [3]. Reprinted with permission from Oxford University Press.

An effective approach to extend the longevity in battery-powered implantable BMIs is to exploit the unique characteristics of ECoG signal. It has been observed that power spectral density of ECoG signals attenuates with frequency [18], and therefore, it spans a wide dynamic range ($\sim$48 dB across 2–200 Hz). While spectral equalization helps reduce the dynamic range, relax the resolution requirement and achieve power-saving in the front-end and mixed-signal blocks, there is still a major bottleneck due to the mandated compute-intensive and power-hungry statistical data processing in the digital back-end. [3] studied the important signal characteristics of raw ECoG and power envelopes during walk and idle states. Fig. 2 shows raw ECoG, γ-band, and its power envelopes (P_γ). As can be seen, changes in P_γ exhibit distinguishable amplitude-modulated voltage variations between walk and idle states which occur in time scale of seconds, implying that both sampling rate and resolution requirements can be significantly relaxed for such signals compared to raw ECoG. These attributes suggest that extracting neural features early in the signal chain using a distinct signal pathway is highly beneficial to minimize the system power dissipation, leading to an energy-efficient neural recording architecture.

III. Proposed Dual-Mode Array Architecture

Given that power envelopes of γ-band can be used to decode movement intentions [3], it is sensible to use a single envelope detector in the analog domain to produce low-bandwidth features for clustering and classification in the digital back-end. However, based on prior work [8]–[11], a specific frequency range within γ-band needs to be identified by human training and data collection/processing of raw ECoG for decoding. Therefore, the front-end circuitry should be capable of acquiring raw ECoG signal and extracting the power envelopes

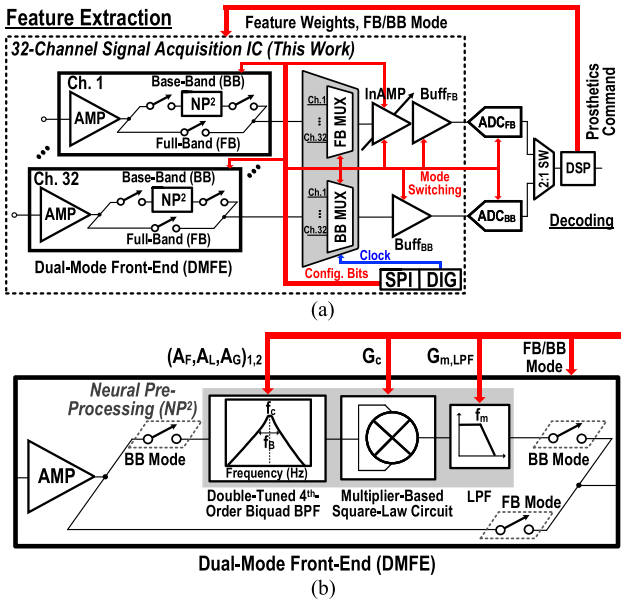


Fig. 3. Proposed dual-mode array architecture: (a) Overall system diagram (b) dual-mode front-end module.

within this identified frequency range. This notion calls for a dual-mode approach to neural recording with two distinct regimes of operation: (1) full-band (FB) mode for raw ECoG signal acquisition with moderate-resolution (8–10 bits) and high sampling rate $f_{s,FB}$ (>13 kS/s), and (2) base-band (BB) mode for power envelope extraction with low-resolution (3–4 bits) and significantly reduced sampling rate $f_{s,BB}$ (>260 S/s). Initially, brain activity across the full-spectrum is momentarily observed during FB mode operation to compute the feature weights in the digital back-end. Subsequently, these weights are fed back to the front-end and the system reverts to BB mode to perform feature extraction. While an implantable high-density ECoG-based BMI needs the FB data for training, calibration and validation purposes, it will primarily operate in BB mode for prosthetic control which accounts for majority of the time.

Fig. 3(a) shows the proposed dual-mode array architecture. The 32-channel signal acquisition system consists of a 32-element dual-mode front-end (DMFE) array, FB/BB time-multiplexers (MUXs), a programmable-gain instrumentation amplifier (InAMP), and FB/BB output buffers (Buffs), a serial peripheral interface (SPI) and a digital circuitry (DIG). The system communicates with the back-end (i.e., DSP or host PC) via SPI, which provides access to internal registers to update feature weights, and select operation mode (FB/BB) or acquisition method (either channel-specific or multiplexed). The latter option is employed to acquire signals from one specific channel or all channels during each operation mode.

To study the power-saving advantage of the proposed architecture in Fig. 3, a simple power analysis is presented. Biased to operate in subthreshold region, each DMFE includes a front-end amplifier (AMP) and neural pre-processing (NP^2) module with power consumption of P_U and P_{NP^2}, respectively. Following the FB MUX, m stages of post-multiplexing amplification/buffering are employed with N-times higher bandwidth compared to the front-end amplifier (N denotes the number of channels). Assuming unity-gain bandwidth product varies linearly with bias current in weak-inversion, each post-multiplexing gain stage approximately consumes $N \cdot P_U$ (to the first-order). Assuming a bandwidth reduction factor of η for the BB operation mode compared to the FB counterpart, the power consumption of the BB output buffer is approximately $N \cdot (\eta P_U)$. Specifically, neural signals in FB mode and extracted features in BB mode occupy a bandwidth of ~200 Hz and ~4 Hz per channel, respectively, resulting in $\eta \approx 0.02$. Moreover, the total dynamic power dissipation of MUX, ADC and DSP is represented by P_D for FB mode and ηP_D for BB mode. While FB operation requires multiplexing, post-multiplexing amplification/buffering, digitization and post-processing with an excessive bandwidth and power consumption, BB operation achieves significant power-saving in the respective blocks with minimum power overhead, P_{NP^2}, in DMFE. To deduce the power-saving advantage, the ratio of system powers $P_{sys,FB}$ and $P_{sys,BB}$ in FB and BB modes is calculated, as follows:

$$\frac{P_{sys,FB}}{P_{sys,BB}} \approx \frac{N \cdot P_U(1+m) + P_D}{N \cdot [P_U(1+\eta) + P_{NP^2}] + \eta \cdot P_D} \quad (1)$$

Given $f_{s,BB} = \eta f_{s,FB}$, BB MUX consumes proportionally less dynamic power compared to FB MUX. Furthermore, the power consumption of the BB ADC is reduced compared to that of the FB ADC due to decreased sampling rate and resolution [19]. It is expected that at low-SNR (<5-bit resolution), component matching and/or minimum realizable capacitance will impose a limit on power dissipation. However, low-bandwidth processing still continues to improve the overall system power consumption. This notion proves to be important for DSP in BB mode as dynamic powers associated with processing ($\propto f_{s,BB}^k$ where k denotes the algorithm complexity) and memory accesses ($\propto f_{s,BB}$) are reduced significantly [20]. For a quantitative comparison, ULP ADCs and DSP from literature are used to evaluate Eq. (1) for $N = 32$ and $m = 2$. Reported ULP ADCs consume as small as 2.7 nW for 1kS/s with 6-bit resolution (BB ADC) and 97nW for 40kS/s with 10-bit resolution (FB ADC) [21]. On the other hand, commercially available DSPs (e.g., C5517 by Texas Instruments) consume milliwatt-level power. Since the desired input-referred noise typically requires P_U to be greater than a few μW and P_{NP^2} introduces a small overhead, the second terms in the numerator and denominator of (1) will dominate $P_{sys,FB}$ and $P_{sys,BB}$, and the power-saving advantage will thus be significant ($\sim \frac{1}{\eta} = 50$). It is noteworthy that an activity-based mechanism realized in the digital back-end will allow for further power-cycling of BB mode during extended idling periods (i.e., night-time sleep).

To allow differential recording of neural signals with respect to a common-reference electrode from ECoG grid, each AMP employs a fully-differential topology. Considering that the differential input impedance of an AMP is approximately equal to 295 MΩ at 60 Hz (C_{in} = 18 pF) and assuming 1 kΩ electrode impedance with $N = 32$, the input interface CMRR of a common-reference scheme with similar recording and reference

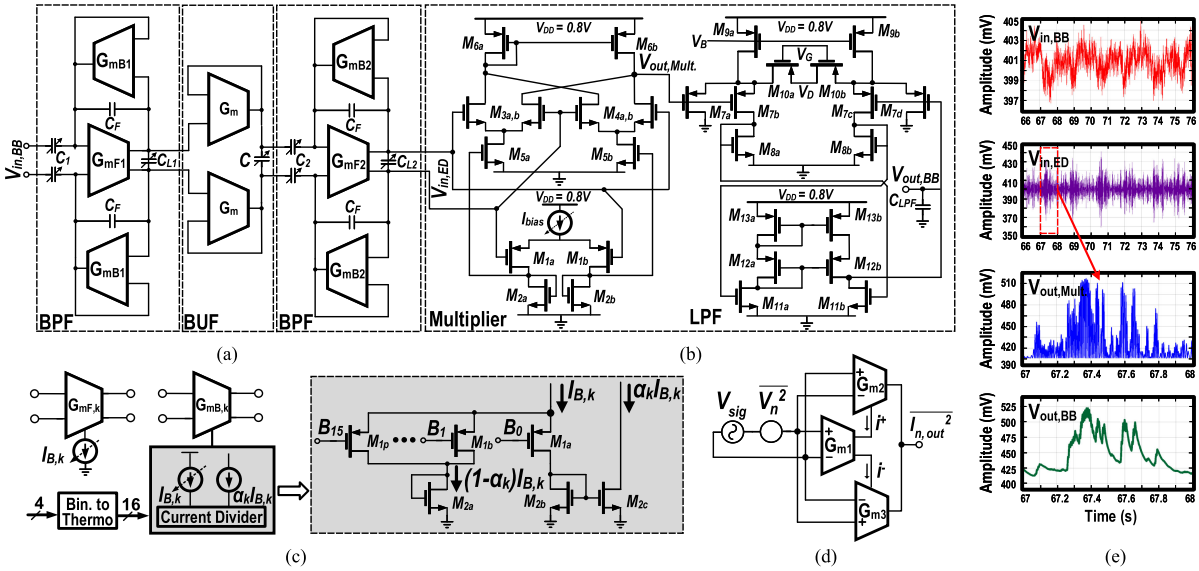


Fig. 4. Neural pre-processing module including (a) double-tuned 4th-order filter, (b) multiplier-based envelope detector, and (c) G_m bias tuning and current division circuitry. (d) Block diagram model of Gilbert cell for noise analysis. (e) Voltage waveforms from each stage of neural pre-processing.

electrode impedance reaches 79.5 dB. However, the overall CMRR is still limited by the AMP to 76.5 dB as reported in Section V-A. Two switchable pathways are incorporated for dual-mode operation. In FB mode, the amplified signals are multiplexed using the FB MUX with fast reset switches to mitigate the channel ghosting and eliminate large artifact residues (Section IV-B). The multiplexed output is further amplified, digitized by the FB ADC (off-chip in this work), and processed by the external digital back-end. In BB mode, NP^2 module performs feature extraction on amplified neural signals based on the appropriate feature weights computed in the back-end (*cf.* Fig. 3(a) and (b)). Extracted power envelopes are then multiplexed and digitized by an off-chip BB ADC prior to digital processing. Shaded in Fig. 3(b), NP^2 module carries out two main operations: band-pass filtering (BPF) and envelope detection using power extraction and averaging. A double-tuned fourth-order biquad realizes the BPF to capture high-γ-band modulations. The center frequency f_c and bandwidth f_B (hence, the quality factor Q) of the BPF are adjusted via A_F, A_L and A_G parameters to achieve better selectivity, reduced pass-band ripple and high out-of-band attenuation (Section IV-A). A multiplier-based square-law circuit performs analog multiplication to obtain signal power and its conversion gain, G_c, is optimized with respect to the input level to minimize signal-dependent noise folding and voltage offsets (Section IV-C). Lastly, a low-pass filter (LPF) with a corner frequency of f_m extracts power envelopes that modulate high-γ-band signals. To match the characteristic time scale of ECoG signals during movements, f_m is adjusted via $G_{m,LPF}$.

IV. Circuit Design and Analysis

A. Dual-Mode Front-End Design

Fig. 3(b) shows the block diagram of the proposed DMFE. Based on our earlier work in [17], the AMP is realized by an operational transconductance amplifier (OTA) within a capacitive feedback loop, which uses a differential stage with regenerative load to boost the open-loop gain. The mid-band gain is set to 40 dB and the frequency response exhibits a high-pass corner of ~2 Hz and a low-pass corner of ~200 Hz. All active and passive components within the AMP are adequately sized to minimize mismatch and process variations to attain high CMRR. To improve the common-mode output resistance of tail current source in the AMP (see Amplifier II in [17]), and hence the CMRR, supply voltage in this design is increased to 0.8 V to allow a higher drain-source voltage for a given bias current.

Figs. 4(a)–(b) depicts detailed realization of NP^2 module. The fourth-order Butterworth BPF is realized by cascading two biquad $G_m - C$ filters and an interstage LPF buffer with high corner frequency to avoid loading effect of the second biquad. The filter characteristics of each biquad section with center frequency, $f_{0,k}$, bandwidth, BW_k, and mid-band gain, $H_{mid,k}$ for $k = 1, 2$, are derived as follows:

$$f_{0,k} = \frac{1}{\sqrt{A_{G,k}A_{L,k}(A_{F,k} + 1 + \frac{A_{F,k}}{A_{L,k}})}} \frac{G_{mF,k}}{2\pi C_F} \tag{2}$$

$$BW_{\mathrm{k}} = \frac{A_{L,k} + A_{G,k}}{A_{G,k}A_{L,k}(A_{F,k} + 1 + \frac{A_{F,k}}{A_{L,k}})} \frac{G_{mF,k}}{2\pi C_F} \tag{3}$$

$$H_{\mathrm{mid,k}} \approx \frac{A_{F,k}}{1 + \frac{A_{L,k}}{A_{G,k}}} \tag{4}$$

where $A_{F,k} = C_k/C_F$, $A_{L,k} = 2C_{L,k}/C_F$ and $A_{G,k} = G_{mF,k}/G_{mB,k}$ for $k = 1, 2$. While 80–160 Hz is designated in this work to be the maximum frequency range of interest, the desired neural features may reside within a narrower range of this band. Each BPF is designed to allow for the required flexibility in frequency-range selection by tuning these parameters, which are represented by the ratios of the same physical quantity. Therefore, they are less prone to process/mismatch

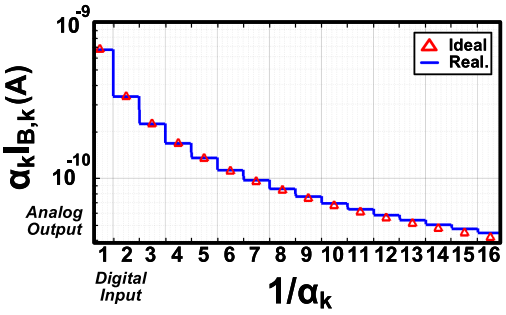


Fig. 5. Linearity of current divider (ideal versus realized).

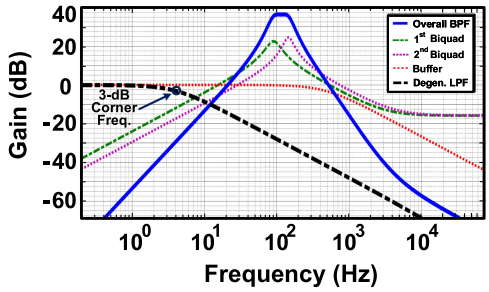


Fig. 6. Frequency response of double-tuned fourth order band-pass and degenerated low-pass filter.

variation; an essential feature required in large-scale systems. On the other hand, $G_{mF,k}/C_F$ in (2) and (3) is more susceptible to the process variation, which is calibrated in an open loop fashion by varying $G_{mF,k}$ through a tunable bias current (7-bit current bank), $I_{B,k}$ for $k = 1, 2$, as shown in Fig. 4(c). While this digital calibration incurs an area overhead that could be further addressed by sharing the same bias current locally among a cluster of channels in favor of reduced die area, it alleviates the testing time and complexity associated with off-chip current trimming in large-scale systems.

To control $A_{G,k}$, the bias current of $G_{mB,k}$ cell is obtained from a current divider that takes a reference current of $I_{B,k}$ and produces $\alpha_k I_{B,k}$, where α_k denotes the division factor for $k = 1, 2$. Bias tuning of $G_{mB,k}$ is achieved by converting a 4-bit binary code to a 16-bit thermometer code which is applied to current divider. Shaded in Fig. 4(c), a digitally controlled current division circuitry is implemented using parallel PMOS switches, M_{1a-1p}, a diode-connected transistor, M_{2a}, and a current mirror, $M_{2b,c}$. Each switch acts as a small parallel resistor when it is ON and as an open-circuit with minimal leakage current when it is OFF. All PMOS switches have an equal output resistance except for M_{1a} whose drain-source voltage may differ slightly from M_{1b-1p}. Fig. 5 shows the ideal and realized transfer characteristics of current divider. α_k is swept across every digital code from 0000 to 1111, which scales $I_{B,k}$ (∼680 pA) by α varying from 1 to 1/ 16. For a maximum division factor of 1/ 16, the output current exhibits less than 6% error at ∼42.5pA. To accommodate wide tunability of $A_{F,k}$ and $A_{L,k}$, each C_k and $C_{L,k}$ is realized by a 4-bit binary-weighted capacitor bank for $k = 1, 2$. Since independent tuning of $f_{0,k}$ and BW_k is not viable, a look-up table is generated off-line based on (2)–(4) for all possible combinations of $A_{F,k}$, $A_{L,k}$ and $A_{G,k}$ which spans the entire solution space. Thereafter, a subset of the solution space which satisfies the desired specifications for $f_{0,k}$, BW_k, and $H_{mid,k}$ for $k = 1, 2$ is found using brute-force search. Controlled by the digital back-end, this look-up table approach allows for a robust mechanism to extract neural features by reconfiguring the parameters $A_{F,k}$, $A_{L,k}$, $A_{G,k}$, G_c, and $G_{m,LPF}$. It is worth mentioning that only one lookup table is used for all channels since the same neural features are extracted from each one.

Shown in Fig. 4(b), the envelope detector consists of a four-quadrant multiplier (Gilbert cell) and a source-degenerated OTA-C filter. Both the multiplier and the OTA-C filter use current folding technique to limit transistor stacking and operate with

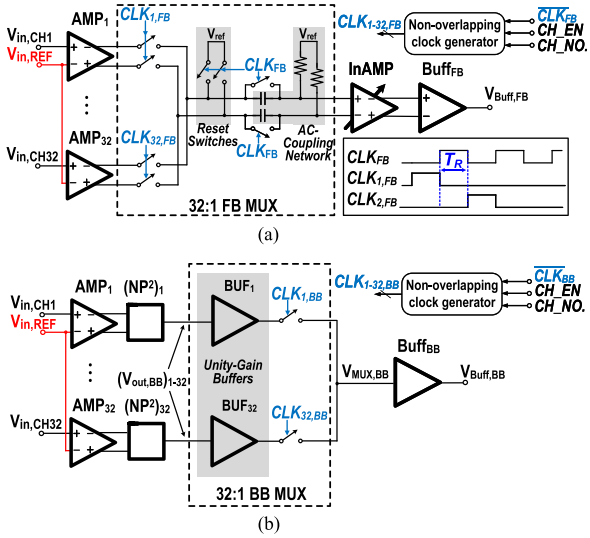


Fig. 7. Multiplexing operation: (a) Full-band (b) base-band.

low supply voltage. A 4-bit binary-weighted current source is used to vary I_{bias} and adjust the conversion gain of the multiplier. Transistors $M_{9a,b}$ mirror the current from a 4-bit binary-weighted current source to allow tunability of transconductance, $G_{m,LPF}$, in the OTA-C filter. To achieve a corner frequency of a few Hz, source-degeneration and current splitting are applied to M_{7a-d} to greatly reduce $G_{m,LPF}$. The voltage waveforms at constituent stages of neural pre-processing from a recorded ECoG signal are shown in Fig. 4(e). Fig. 6 shows the frequency response of the double-tuned 4th-order biquad filter with a center frequency of 120 Hz and bandwidth of 80 Hz and degnerated low-pass filter with a 3-dB corner frequency of 4 Hz.

B. Post-Multiplexing and Interfacing Modules Design

Similar to [17], an external clock is provided to generate non-overlapping clocks (CLK_{1-32}) with 1/ 64 duty-cycle for FB/BB channel multiplexing with an additional option to select individual channels. In FB mode, a digitally-programmable InAMP is used to accommodate 20–40 dB of additional post-multiplexing amplification with 3 dB gain steps. Shown in Fig. 7(a), the AC-coupling network with approximately 2-Hz highpass corner frequency is employed between the AMP and InAMP to filter out the voltage offset introduced by each AMP during

single-channel acquisition. For multi-channel acquisition, in order to avoid large transients during channel-multiplexing, a reset/bootstrap mechanism is introduced to the AC-coupling network in FB MUX. This is achieved by applying CLK_{FB} to reset switches during the non-overlapping intervals (T_R), which ensures that the output voltage stays at reference voltage V_{ref} after each channel switching. To mitigate the long settling time of AC-coupling network, an auxiliary pair of switches is used to bootstrap the voltages across the AC-coupling capacitors to V_{ref}. It is noteworthy that the AC-coupling network is rendered ineffective in multi-channel acquisition due to the reset/bootstrap operation. Each switch is realized by a T-network of transmission gates with dummy devices to mitigate charge-injection and clock-feedthrough effects. Fig. 7(b) indicates the multiplexing operation in BB mode. No additional gain is required after envelope detection. Nevertheless, a unity-gain buffer is placed before the BB MUX switch to buffer the high-impedance output node of envelope detector ($V_{out,BB}$) from the shared multiplexed output node ($V_{MUX,BB}$). FB/BB output buffers are used to drive an external ADC in this implementation.

C. Noise Analysis of Multiplier-Based Square-Law Circuit

In this section, noise interactions that happen in the multiplier-based envelope detector are further studied. The Gilbert-cell multiplier of Fig. 4(b) is modeled as three transconductors, G_{m1}, G_{m2} and G_{m3} in Fig. 4(d). It is evident that small-signal multiplication is achieved by applying a small AC signal (i^+/i^-) to each bias current of G_{m2} and G_{m3}. The filtered neural signal and noise contributions from the previous stages are represented by V_{sig} and $\overline{V_n^2}$, respectively. Due to the non-linear behavior of analog multiplier, signal and noise at the input undergo multiplication that results in an increased noise power. Three major sources of noise contribution are identified in a multiplier-based envelope detector [22]: (a) signal-dependent noise due to mixing between signal and noise, (b) noise self-mixing due to mixing of noise with itself, and (c) intrinsic circuit noise, which is the sum of all existing device noise (e.g., thermal and flicker noise) powers in the envelope detector. Therefore, the total current noise power at the output of envelope detector $\overline{I_{n,out}^2}$ is expressed, as follows:

$$\overline{I_{n,out}^2} = \overline{I_{n,sig}^2} + \overline{I_{n,n}^2} + \overline{I_{n,ED}^2} \tag{5}$$

where $\overline{I_{n,sig}^2}$, $\overline{I_{n,n}^2}$, $\overline{I_{n,ED}^2}$ represent the signal-dependent, self-mixing, envelope detector current noise powers. As discussed, high-γ brain signals are observed to be amplitude modulated (AM) during kinetic movements, which can be thought of as a carrier signal with an underlying modulating function. This AM signal is assumed to be a sinusoidal carrier f_c at the center of high-γ-band whose average power, $A_c^2/2$, is equivalent to the total signal power within the band modulated by a normalized baseband function, $m(t)$, whose modulation frequency and index are defined by f_m and a_m, respectively. Hence, the signal at the input of multiplier is readily expressed, as follows:

$$V_{sig,AM} = A_c[1 + a_m m(t)]\cos(2\pi f_c t) \tag{6}$$

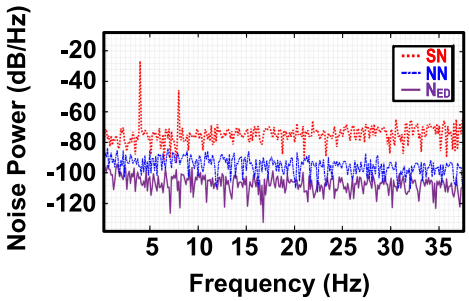


Fig. 8. Simulated noise power of each contributing sources (SN: signal-dependent noise, NN: self-mixing noise, N_{ED}: intrinsic noise of envelope detector.

It is observed that power spectral density of brain signals follows a $(\frac{1}{f})^p$ characteristic where $p = 2 \sim 4$ [18]. Thus, the total signal power $(\frac{A}{f})^p$ across the high-γ bandwidth f_B is calculated by integration, as follows:

$$\overline{V_{sig,\gamma}^2} = \int_{f_c-0.5f_B}^{f_c+0.5f_B} \left(\frac{A}{f}\right)^p df = \frac{A^p}{(-p+1)} f^{(-p+1)}\Big|_{f_c-0.5f_B}^{f_c+0.5f_B} \tag{7}$$

The average noise power from the front-end circuitry preceding the multiplier, $\overline{V_n^2}$, is obtained by integrating the overall power spectral density of all noise sources (i.e., thermal and flicker noise) over f_B. As such, the equivalent white power spectral density, $\overline{V_n^2}/f_B$, is readily used to calculate the output noise of the envelope detector across the LPF bandwidth of f_m. Assuming $m(t)$ has zero average value, $\overline{I_{n,sig}^2}$ and $\overline{I_{n,n}^2}$ are thus derived, as follows:

$$\overline{I_{n,sig}^2} = 6\,G_c^2 \overline{V_{sig,\gamma}^2}[1 + a_m^2 \overline{m^2(t)}]\frac{f_m}{f_B}\overline{V_n^2} \tag{8}$$

$$\overline{I_{n,n}^2} = 3\,G_c^2 \frac{f_m}{f_B}(\overline{V_n^2})^2 \tag{9}$$

where G_c $\left(= I_{bias}/(2nV_{th})^2\right.$, where n represents sub-threshold slope$\left.\right)$ is conversion gain of the multiplier.

The envelope detector average current noise power, $\overline{I_{n,ED}^2}$, is found by summing the thermal and flicker noise contributions of transistors (M_{1-6}), shown in Fig. 4(b), and integrating its noise power spectral density over the bandwidth f_m:

$$\overline{I_{n,ED}^2} = 8kT\gamma(g_{m1} + 2g_{m2} + 2g_{m3} + g_{m6})f_m + \frac{2K_p}{C_{ox}(WL)_1} \times \left[g_{m1}^2 + \frac{K_n(WL)_1}{K_p(WL)_2}(2g_{m2})^2 + \frac{K_n(WL)_1}{K_p(WL)_3}(2g_{m3})^2 + \frac{(WL)_1}{(WL)_6}(g_{m6})^2\right] \int_{0.1f_m}^{f_m} \left(\frac{df}{f}\right) \tag{10}$$

where K_p and K_n denote the process-dependent flicker noise constants for PMOS and NMOS devices, respectively. C_{ox} represents the gate-oxide capacitance per unit area. Shown in Fig. 8, noise power of each contributing source at the output of multiplier is plotted for an AM input signal, similar to (6), with the following parameters: $A_c = 50$ μV, $f_c = 120$ Hz,

$f_m = 4$ Hz and $a_m = 0.5$. As expected, signal-dependent noise contribution is much more significant compared to the intrinsic transistor noise of envelope detector and varies with the input signal amplitude.

To arrive at the output SNR, one needs to find the average power of the output signal ($\overline{I^2_{sig^2,out}}$) which can be found by integration, assuming $m(t)$ has zero average value:

$$\overline{I^2_{sig^2,out}} = \lim_{T\to\infty} \frac{1}{2T}\int_{-T}^{T} \left(G_c V^2_{sig,AM}\right)^2 dt$$
$$= \frac{3}{2} G_c^2 \left(\overline{V^2_{sig,\gamma}}\right)^2 [1 + 6a_m^2 \overline{m^2(t)} + a_m^4 \overline{m^4(t)}] \quad (11)$$

Omitting small noise contribution of envelope detector for simplicity and assuming 50% duty-cycled square wave for $m(t)$, output SNR (SNR_{out}) is found as a non-linear function of input SNR (SNR_{in}) :

$$SNR_{out} = \frac{\overline{I^2_{sig^2,out}}}{\overline{I^2_{n,out}}} = SNR_{in} \frac{(1+a_m^2)^2 + 4a_m^2}{4(1+a_m^2) + \frac{2}{SNR_{in}}} \frac{f_B}{f_m} \quad (12)$$

SNR_{in} in (12) is a function of high-γ bandwidth and is derived from (7), i.e.,

$$SNR_{in} = \frac{A^p}{\overline{V_n^2}} \frac{(Q-1/2)^{-(p-1)} - (Q+1/2)^{-(p-1)}}{(p-1) f_B^{p-1}} \quad (13)$$

As defined before, Q denotes the BPF quality factor. It is evident from (13) that lowering Q by reducing f_c (i.e., constant bandwidth) to contain only the neural features of interest provides the highest SNR_{in}. As predicted in [18], SNR_{in} is expected to degrade with the sharper roll-off (i.e., higher p value), particularly above 80 Hz. However, the premise of high-γ AM modulations implies that with higher a_m, which may further improve over time with co-adaptation of an implanted BMI, it is advantageous to perform low-noise analog power envelope extraction to achieve higher SNR as derived in (12), while attaining significant power-saving at the system-level. Two special cases of (12) are considered: (a) low and (b) high input SNR. For (a), it can be seen that the output SNR becomes proportional to SNR_{in}^2. However, for (b), it is understood that with increasing the signal amplitude, the signal-dependent noise term also increases and therefore, the output SNR is proportional to SNR_{in}.

D. Transient Analysis of Post-Multiplexing Modules

Since FB MUX operates at significantly higher frequency compared to BB MUX, subsequent amplification stages in FB mode must satisfy more stringent settling time and bandwidth requirements. Given n_{FB}-bit resolution for the FB ADC, the amplified output voltage is required to reach its full-scale level within $0.69(n_{FB}+\varepsilon)\tau_{FB}$ for the conventionally adopted error margin of $1/2^{\varepsilon}$ LSB ($2 \le \varepsilon \le 4$). τ_{FB} is defined as the time constant of an equivalent RC circuit modeling the output load of the post-multiplexing amplification stage in FB mode. Similarly, for n_{BB}-bit resolution of BB ADC, the amplified output voltage is required to settle within $0.69(n_{BB}+\varepsilon)\tau_{BB}$, where τ_{BB} is the equivalent time constant in BB mode. The output voltage settling required in each mode of operation should be succeeded within a half sampling period, i.e., $0.69(n_{FB}+\varepsilon)\tau_{FB} \le \frac{0.5}{f_{s,FB}}$ and $0.69(n_{BB}+\varepsilon)\tau_{BB} \le \frac{0.5}{f_{s,BB}}$. Hence, the ratio of the minimum required bandwidths for FB/BB post-multiplexing stages is expressed as follows:

$$\left(\frac{\tau_{BB}}{\tau_{FB}}\right)_{min} = \frac{(n_{FB}+\varepsilon) f_{s,FB}}{(n_{BB}+\varepsilon) f_{s,BB}} \approx \frac{n_{FB}}{n_{BB}} \frac{1}{\eta} \quad (14)$$

(14) signifies that the minimum required bandwidth for post-multiplexing stages is approximately two orders of magnitude higher in FB compared to BB mode for $\varepsilon = 2$ and $\eta = 0.02$, given the different settling requirements. This is to be expected, as time-multiplexed FB operation requires signifcantly higher sampling rate and resolution than BB operation.

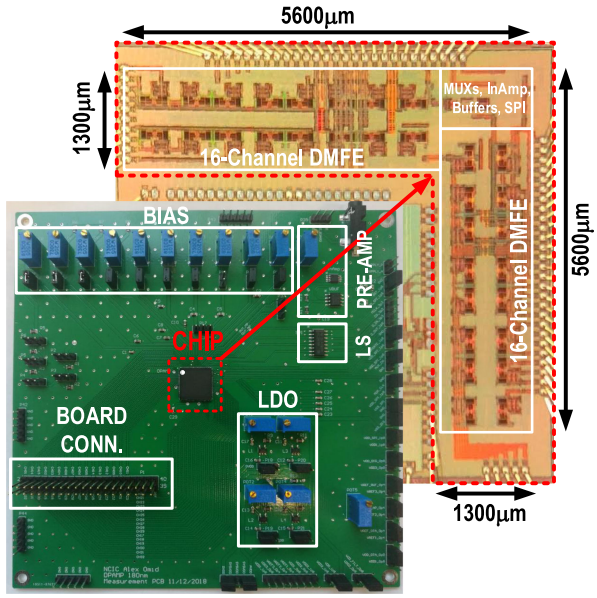


Fig. 9. Chip micrograph and custom-designed printed circuit board.

V. Experimental Results

In this section, electrical and biomedical measurements are presented. Electrical characterization was done prior to any biomedical testing to ensure proper functionality and reliable recording of the system. In-vivo human tests involved EEG and ECoG measurements. The DMFE array recorded reliably in all testings and showed on-par performance with commercial systems while consuming significantly less power.

A. Electrical Measurements

The prototype was fabricated in 180 nm CMOS process. Fig. 9 shows the chip micrograph along with the custom-designed printed circuit board (PCB). An L-shaped geometry was employed to accommodate the DMFE array, placing each channel in the proximity of the pad ring. The pads are located around the perimeter and incorporates a 2 kV HBM ESD protection circuitry with a few pA of leakage current. Following a modular

TABLE I
PERFORMANCE COMPARISON

Reference	TBCAS 2018 [23]	TBCAS 2016 [24]	TBCAS 2015 [25]	CICC 2017 [26]	ISSCC 2014 [27]	This Work
Process (nm)	180	180	180	65	130	180
Architecture	AMP	ASP	DSP	DSP	ASP	DM-ASP
No. of channels	1	16	8	1	1	32
Supply Voltage (V)	1.8	0.9	1.8(A)/1(D)	0.8	1.3-1.8	0.8
Gain (dB)	35.04	40	40	22-43	20-44	60-81.47(FB)/57-76(BB)
Bandwidth (Hz)	9.3k	0.3-7k	0.5-100	250	130	2-200
IR-Noise (μV_{rms})	3.2	4.57	0.81	1.90-2.91	4.9	1.49
NEF	1.94	4.77	4.0	4.17-4.47[a]	6.46[a]	4.09
PEF	6.77	15.45	12.96	13.88-15.97[a]	54.27-75.14[a]	10.04-13.38[b]
CMRR (dB)	76	81	100	82	>90	>76.5
Feature Extraction/Total Power per channel (μW)	NA/4.5	7/15	7/34	0.307-0.769	0.33/0.9	0.205/1.05
Area per channel (mm^2)	0.072	0.116	3.125	2	8.6	0.245

[a] Estimated from reported results.
[b] For operation with 0.6 to 0.8 V supply.

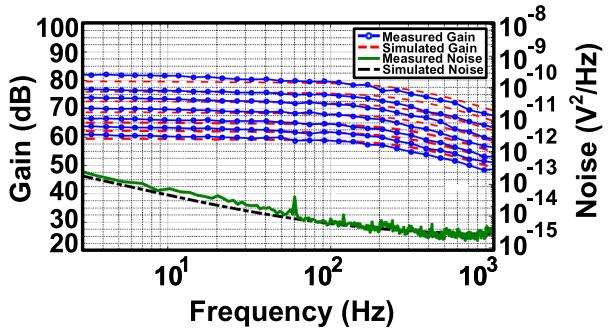


Fig. 10. Measured and simulated results of total gain in different settings and input-referred noise for a single channel (i.e., AMP and InAMP) in FB mode.

TABLE II
FRONT-END POWER CONSUMPTION BREAKDOWN

Block	BB	FB
AMP	798 nW	798 nW
Biquads	2.4 nW	-
Int. Buffer	4 nW	-
Multiplier	160 nW	-
Degen. LPF	9.36 nW	-
Buffer	80 nW	-
InAMP*	-	920 nW
FB Buffer*	-	137 nW
BB Buffer*	25 nW	-
Total	1.08 μW	1.86 μW

* Power consumption of shared blocks is divided by channel count.

design, two 16-channel DMFE arrays were constructed perpendicular to each other with shared building blocks, including InAMP, output buffers, digital circuitry and SPI placed at the intersection. This approach is pursued to allow seamless integration of more channels with less routing overhead and inclusion of other common blocks such as low-dropout (LDO) regulators, ADCs and reference buffers in the finalized design. Global bias is provided externally and local bias is generated internally within each module and is tuned via current banks. The custom-designed PCB includes bias, SPI level shifters (LS), LDO regulators for chip supply, and pre-amplifier (TI-INA826, not shown in Fig. 3(a)) before external ADC to meet the dynamic range requirements. The chip operates at 0.8 V supply voltage and consumes 59.4 μW in FB and 34.6 μW in BB mode (excluding bias). Each DMFE consumes 1.05 μW power and 0.245 mm^2 area, allocating 0.205 μW power and 0.145 mm^2 area for feature extraction only.

To characterize the overall amplification and input-referred noise in FB mode, an Agilent 33250A waveform generator with external attenuators and an Agilent E4448A spectrum analyzer were used. The nominal gain setting of the InAmp provides an additional 20 dB of gain, with 3 dB steps up to $\sim$40 dB. Shown in Fig. 10, the total measured gain in different settings and input-referred noise are compared with simulation results. For an InAMP gain setting of 23 dB, an overall gain of 63 dB and an RMS input-referred noise of 1.49 μV were achieved across a 2-200-Hz bandwidth. While the lower corner frequency realized by pseudo-resistor is expected to vary across the process corner, it is simulated and measured to be below 2 Hz, which helps acquire low-frequency activity of the brain in θ-band (4–8 Hz). For an input common-mode signal of 100 mV$_{pp}$, the measured CMRR and PSRR are better than 76.5 dB and 79 dB, respectively. The calculated dynamic range of AMP for $\sim$1% total harmonic distortion is 60.2 dB. Table I provides a performance summary of the DMFE and comparison with similar prior works. Based on a dual-mode ASP architecture, the DMFE consumes 1.05 μW of power and occupies 0.245 mm^2 of die area per channel while achieving an NEF of 4.09 and a PEF of 10.04. The DMFE achieves the lowest feature-extraction power dissipation with superior NEF and PEF compared to prior works. The power consumption of each block in the front-end is summarized in Table II. The power dissipation of the AMP is represented by P_U in (1), while the InAMP and FB buffer constitute the post-amplification stages. The power dissipated by biquads, interstage buffers, multiplier, degenerated LPF and buffer sum up to represent P_{NP^2}. Lastly, BB buffer is used to approximate ηP_U in (1). As indicated, AMP takes a significant portion of the total power consumption in both BB and FB mode given that the first-stage amplification requires more power dissipation to minimize the input-referred noise. In NP^2 module, the multiplier introduces voltage offset that can be minimized by increasing the bias current, and hence raising the power consumption. Nevertheless, the BB-mode, compared to FB-mode operation, still achieves approximately twice less power dissipation in the

TABLE III
SUB-BAND CORRELATION COEFFICIENTS

Signal/Mode/Acq. Method	θ (4-8 Hz)	α (9-12 Hz)	β (13-30 Hz)	low-γ (30-70 Hz)	high-γ (80-160 Hz)	γ (80-100 Hz)	Raw
EEG/FB/Single	0.982	0.989	0.984	0.952	-	0.907	0.946
EEG/FB/Multiplexed	0.899	0.914	0.729	0.686	-	0.407	0.871
ECoG/FB/Single	0.998	0.989	0.961	0.948	-	0.889	0.924
ECoG/FB/Multiplexed	0.992	0.987	0.979	0.842	0.584	-	0.964
ECoG/BB/Single	-	-	-	-	-	-	0.769
ECoG/BB/Multiplexed	-	-	-	-	-	-	0.60-0.84

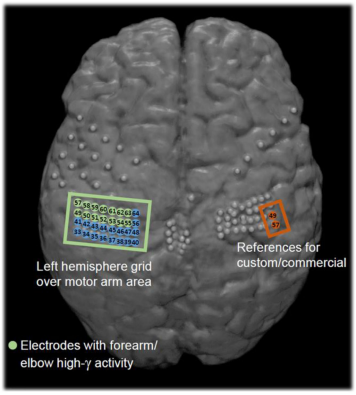


Fig. 11. MR-CT fused image from Subject B, showing implanted ECoG grid over arm motor area of the brain.

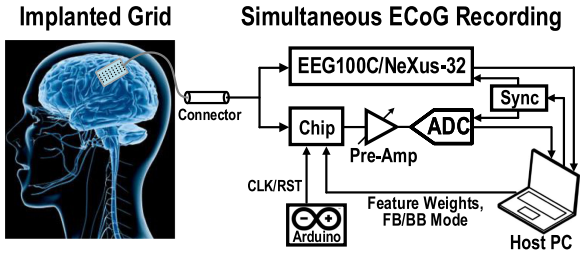


Fig. 12. Hospital setup.

front-end with the premise that the mixed-signal and digital back-end would require significantly less power, achieving 50× power-saving as discussed in Section III.

B. Human Neurological Measurements

The experiments carried out in this study were approved by the Institutional Review Boards of the University of California, Irvine and the Rancho Los Amigos National Rehabilitation Center, and are considered non-significant risk. Two human subjects (A and B) provided informed consent to participate in EEG and ECoG recordings, respectively. Single-channel and multi-channel acquisition in FB were done for EEG, in conjunction with commercial systems to validate the performance on Subject A. Similarly, single-channel and multi-channel ECoG recording in FB and BB were done at the bedside with Subject B, who was undergoing epilepsy treatment. A summary of correlation coefficients from all recordings in each frequency sub-band is presented in Table III. For brevity, methods and results from in-vivo ECoG recordings are described in the following sections.

Methods: One male patient undergoing ECoG implantation for epilepsy surgery evaluation was recruited (Subject B). The subject had a 4 × 8 mini-grid (Integra LifeSciences, Plainsboro NJ). Fig. 11 shows the location of implanted electrodes (derived by co-registering CT and MR brain images). The ECoG grid placed over the left hemispheric (LH) motor arm area was used to record brain activity during sleep (baseline) and a flexion task in FB and BB modes, respectively. Fig. 12 shows the hospital setup for in-vivo ECoG recording. 32 electrodes from LH grid were used to record ECoG signals by custom (chip) and commercial (Biopac EEG100C, NeXus-32) systems, simultaneously. The chip was battery-powered and Biopac MP150 data acquisition was used to digitize the analog output. An Arduino provided the clock (CLK) and reset (RST) signals for the chip. A host PC was responsible for chip configuration, synchronization between custom and commercial system outputs, de-multiplexing and post-processing of ECoG recordings. For FB single-channel and multi-channel recording, EEG100C and NeXus-32 were used in parallel with the chip to capture baseline activity, respectively. The subject was asleep during these experiments. For both BB single-channel and multi-channel recording, NeXus-32 was used in parallel with the chip. The subject was verbally instructed to perform elbow flexion for two 15-second periods with an idling period of 15 (single-channel) and 10 (multi-channel) seconds in between. Since NeXus-32 did not natively extract envelopes, chip-equivalent processing (i.e., band-pass filtering, power extraction and low-pass filtering) were applied in order to draw a comparison between the two acquisition systems. As depicted in Fig. 11, a subset of LH electrodes, which was determined by clinical cortical mapping procedures to correspond to forearm/elbow flexion, was used to collect brain activity for analysis during sleep (baseline) and an elbow flexion task. Given separate reference electrodes for custom chip and NeXus-32, the split reference was compensated for by common-mode averaging in post-processing [28]. The Pearson correlation was calculated between the outputs of custom and commercial systems for comparison. Additionally, correlations were calculated for physiological sub-bands to further ascertain the accuracy of the chip in comparison with the commercial system.

Results: FB single-channel and multi-channel recordings from custom and commercial systems are shown in Fig. 13(a)–(b). For BB single-channel, the extracted envelope is shown in Fig. 14, along with a spectrogram of raw ECoG from NeXus-32 which exhibits power increase across high-γ-band during movement. For BB multi-channel recording, a few extracted envelopes are shown in Fig. 15. Unlike the FB-mode data, which can be seamlessly compared between the commercial and custom systems, the comparison of the BB-mode data requires

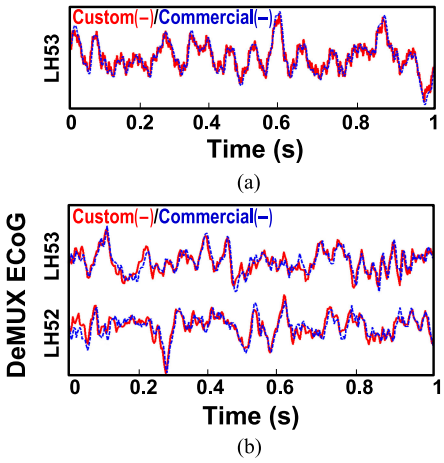


Fig. 13. Normalized ECoG time-series data from (a) single-channel recording and (b) de-multiplexed recording in FB mode.

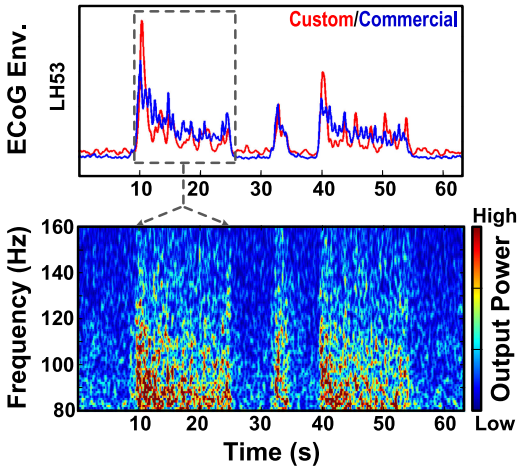


Fig. 14. Normalized ECoG power envelope time-series data from single-channel recording in BB mode (top) and spectrogram of raw ECoG from commercial system (bottom).

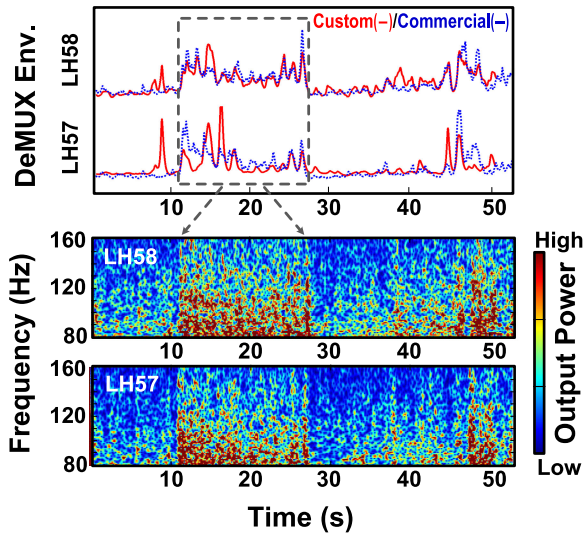


Fig. 15. Normalized ECoG power envelope time-series data from de-multiplexed recording in BB mode (top) and spectrogram of raw ECoG from commercial system (bottom).

extensive signal processing, as discussed earlier. Considering that the analog implementation introduces a number of noise sources (Section IV-C), the digital chip-equivalent operators suffer mainly from insignificant quantization and rounding errors, giving rise to lower correlations reported for the BB-mode data as compared to the FB counterpart.

VI. Conclusion

A dual-mode array architecture for high-density ECoG implantable BMIs was presented. The 180 nm CMOS chip includes a 32-channel signal acquisition front-end capable of acquiring and pre-processing of ECoG signals. Each channel employs a DMFE which consumes 1.05 μW and 0.245 mm^2 area, allocating 0.205 μW and 0.145 mm^2 area for feature extraction only. In-vivo ECoG recordings have demonstrated the feasibility of extracting power envelopes during movements using our ULP dual-mode prototype. Compared to commercial systems, our chip is capable of acquiring power envelopes with significantly less power consumption.

Acknowledgment

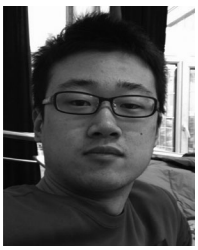
The authors would like to thank Dr. Alireza Karimi-Bidhendi for helpful technical discussions, TowerJazz Semiconductor for chip fabrication and D. Huh of Keysight Technologies for providing measurement equipment.

References

[1] M. J. Vansteensel *et al.*, "Fully implanted brain–computer interface in a locked-in patient with als," *New England J. Med.*, vol. 375, no. 21, pp. 2060–2066, 2016.
[2] A. L. Benabid *et al.*, "An exoskeleton controlled by an epidural wireless brain–machine interface in a tetraplegic patient: a proof-of-concept demonstration," *Lancet Neurol.*, 2019.
[3] C. M. McCrimmon *et al.*, "Electrocorticographic encoding of human gait in the leg primary motor cortex," *Cerebral Cortex*, vol. 28, no. 8, pp. 2752–2762, 2017.
[4] G. Schalk *et al.*, "Two-dimensional movement control using electrocorticographic signals in humans," *J. Neural Eng.*, vol. 5, no. 1, p. 75, 2008.
[5] J. Kubanek, K. Miller, J. Ojemann, J. Wolpaw, and G. Schalk, "Decoding flexion of individual fingers using electrocorticographic signals in humans," *J. Neural Eng.*, vol. 6, no. 6, p. 066001, 2009.
[6] K. Miller, S. Zanos, E. Fetz, M. Den Nijs, and J. Ojemann, "Decoupling the cortical power spectrum reveals real-time representation of individual finger movements in humans," *J. Neurosci.*, vol. 29, no. 10, pp. 3132–3137, 2009.
[7] P. T. Wang *et al.*, "Characterization of electrocorticogram high-gamma signal in response to varying upper extremity movement velocity," *Brain Struct. Function*, vol. 222, no. 8, pp. 3705–3748, 2017.
[8] N. E. Crone *et al.*, "Functional mapping of human sensorimotor cortex with electrocorticographic spectral analysis. i. alpha and beta event-related desynchronization," *Brain*, vol. 121, no. 12, pp. 2271–2299, 1998.
[9] N. E. Crone, D. L. Miglioretti, B. Gordon, and R. P. Lesser, "Functional mapping of human sensorimotor cortex with electrocorticographic spectral analysis. ii. event-related synchronization in the gamma band," *Brain*, vol. 121, no. 12, pp. 2301–2315, 1998.
[10] K. J. Miller *et al.*, "Spectral changes in cortical surface potentials during motor movement," *J. Neurosci.*, vol. 27, no. 9, pp. 2424–2432, 2007.
[11] J. Ruescher, O. Iljina, D.-M. Altenmüller, A. Aertsen, A. Schulze-Bonhage, and T. Ball, "Somatotopic mapping of natural upper-and lower-extremity movements and speech production with high gamma electrocorticography," *Neuroimage*, vol. 81, pp. 164–177, 2013.
[12] A. Avestruz *et al.*, "A 5 μ w/channel spectral analysis IC for chronic bidirectional brain–machine interfaces," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3006–3024, 2008.

[13] R. R. Harrison, "The design of integrated circuits to observe brain activity," *Proc. IEEE*, vol. 96, no. 7, pp. 1203–1216, Jul. 2008.
[14] F. Zhang, A. Mishra, A. G. Richardson, and B. Otis, "A low-power ECoG/EEG processing ic with integrated multiband energy extractor," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 58, no. 9, pp. 2069–2082, Sep. 2011.
[15] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A. P. Chandrakasan, "A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 804–816, Apr. 2010.
[16] W. J. Freeman, L. J. Rogers, M. D. Holmes, and D. L. Silbergeld, "Spatial spectral analysis of human electrocorticograms including the alpha and gamma bands," *J. Neurosci. Methods*, vol. 95, no. 2, pp. 111–121, 2000.
[17] A. Karimi-Bidhendi *et al.*, "CMOS ultralow power brain signal acquisition front-ends: design and human testing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 5, pp. 1111–1122, Oct. 2017.
[18] K. J. Miller *et al.*, "Power-law scaling in the brain surface electric potential," *PLoS Comput. Biol.*, vol. 5, no. 12, p. e1000609, 2009.
[19] B. Murmann, "A/D converter trends: Power dissipation, scaling and digitally assisted architectures," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2008, pp. 105–112.
[20] V. R. Pamula, C. Van Hoof, and M. Verhelst, *Adaptive Sampling for Ultra-Low-Power Electrocardiogram (ECG) Readouts*. Cham: Springer International Publishing, 2019, pp. 11–31.
[21] B. Murmann *et al.*, "ADC performance survey 1997–2019," 2019. [Online]. Available: http://www.stanford.edu/murmann/adcsurvey.html
[22] X. Huang, G. Dolmans, H. de Groot, and J. R. Long, "Noise and sensitivity in RF envelope detection receivers," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 60, no. 10, pp. 637–641, Oct. 2013.
[23] M. Rezaei, E. Maghsoudloo, C. Bories, Y. De Koninck, and B. Gosselin, "A low-power current-reuse analog front-end for high-density neural recording implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 2, pp. 271–280, Apr. 2018.
[24] X. Liu, M. Zhang, A. G. Richardson, T. H. Lucas, and J. Van der Spiegel, "Design of a closed-loop, bidirectional brain machine interface system with energy efficient neural feature extraction and PID control," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 4, pp. 729–742, Aug. 2017.
[25] M. A. B. Altaf and J. Yoo, "A 1.83 μ J/classification, 8-channel, patient-specific epileptic seizure classification soc using a non-linear support vector machine," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 1, pp. 49–60, Feb. 2015.
[26] S. Mondal, C.-L. Hsu, R. Jafari, and D. Hall, "A dynamically reconfigurable ECG analog front-end with a 2.5× data-dependent power reduction," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2017, pp. 1–4.
[27] L. Yan *et al.*, "A 680 nA fully integrated implantable ECG-acquisition IC with analog feature extraction," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 418–419.
[28] J. Dien, "Issues in the application of the average reference: Review, critiques, and recommendations," *Behav. Res. Methods, Instrum. Comput.*, vol. 30, no. 1, pp. 34–43, 1998.

Omid Malekzadeh-Arasteh (Student Member, IEEE) received the B.S. degree in electrical engineering from Northwestern University, Evanston, IL, USA, in 2015. He is currently working toward the Ph.D. degree in electrical engineering with the University of California, Irvine, Irvine, CA, USA. His research interests include analog and digital circuit design, low-power IC design, and biomedical circuits for brain-computer interface applications.



Haoran Pu (Student Member, IEEE) received the B.S. degree (Hons.) in electrical and computer engineering from the Ohio State University, Columbus, OH, USA, in 2015, and the M.S. degree in electrical engineering from the University of California, San Diego, La Jolla, CA, USA, in 2017. He is currently working toward the Ph.D. degree in electrical engineering with the University of California, Irvine, Irvine, CA, USA. His current research focuses on biomedical integrated circuits for brain-computer interfaces.

Jeffrey Lim (Student Member, IEEE) received the B.S. degree in biomedical engineering from the University of California, San Diego, La Jolla, CA, USA, in 2015. He is currently working toward the Ph.D. degree in biomedical engineering with the University of California, Irvine, Irvine, CA, USA. His current research focuses on artifact characterization and suppression in bi-directional brain-computer interfaces.

Charles Yu Liu is currently a Professor of neurosurgery, neurology, urology, biomedical engineering, and biokinesiology and physical therapy with the University of Southern California, Los Angeles, CA, USA, where he also serves as the Director of the USC Neurorestoration Center. He is also the Chair of Neurosurgery and Orthopedics at Rancho Los Amigos National Rehabilitation Center.

An H. Do is currently an Assistant Professor with the Department of Neurology, University of California, Irvine, CA, USA. He completed his residency and fellowship training in neurology and spinal cord injury medicine, respectively. His area of research is in developing and applying brain-computer interfaces to help people with paralysis due to neurological injuries to improve or regain motor function.

Zoran Nenadic (Senior Member, IEEE) is currently William J. Link Chair and a Professor of biomedical engineering with the University of California, Irvine, Irvine, CA, USA, where he is also the Director of Center for BioMedical Signal Processing and Computation (CBMSPC). He was the recipient of several research awards, including the Faculty Early Career Development (CAREER) Award from the NSF and the Hiruma-Wagner Award from the Japanese Research Foundation for Opto-Science and Technology.

Payam Heydari (M'01–SM'09–F'17) is currently a Professor of electrical engineering with the University of California, Irvine, Irvine, CA, USA where he is also the Director of Nanoscale Communication IC Labs. A recipient of numerous awards, he is the main principal investigator of an eight-million dollars National Science Foundation Award on the development of a bi-directional brain-machine interface.