

# Performance Analysis of Impinging Chip-Attached Micro Pin Fin Direct Liquid Cooling Package for Hotspot Targeted Applications

Vahideh Radmard  
*Department of Mechanical Engineering*  
State University of New York  
Binghamton, USA  
Vradmar1@binghamton.edu

Arad Azizi  
*Department of Mechanical Engineering*  
State University of New York  
Binghamton, USA  
aazizil@binghamton.edu

Srikanth Rangarajan  
*Department of Mechanical Engineering*  
State University of New York  
Binghamton, USA  
srangar@binghamton.edu

Najmeh Fallahtafi  
*Department of Mechanical Engineering*  
State University of New York  
Binghamton, USA  
nfallah@binghamton.edu

Cong H Hoang  
*Department of Mechanical Engineering*  
State University of New York  
Binghamton, USA  
hhoang2@binghamton.edu

Ghazal Mohsenian  
*Department of Mechanical Engineering*  
State University of New York  
Binghamton, USA  
gmohsen1@binghamton.edu

Kourosh Nemati  
*Future Facilities*  
NYC, USA  
kourosh.nemati@futurefacilities.com

Scott N Schiffres  
*Department of Mechanical Engineering*  
State University of New York  
Binghamton, USA  
sschiffrr@binghamton.edu

Bahgat Sammakia  
*Department of Mechanical Engineering*  
State University of New York  
Binghamton, USA  
bahgat@binghamton.edu

**Abstract**— As heterogeneous integration evolves, the diversity and density of devices that combine multiple functionalities has significantly increased. The subsequent increase in power usage and reduced size of components, specifically of Central Processing Units (CPUs), underlines the limitations of traditional cooling and reveals the need for significant improvements in thermal management. In this study, an innovative fluid-thermal cooling solution that addresses high density and non-uniform heat dissipation in a CPU package will be presented. The solution design includes jet impingement, which is used to directly cool four electronic chips simultaneously, as well as chip-attached micro pin fins. The copper micro pin fins have been additively manufactured onto the surface of the silicon chip using Selective Laser Melting (SLM), thus eliminating the need for thermal interface materials (TIMs). The effects of jet nozzle size and jet-to-chip distance on heat transfer and fluid flow are numerically investigated. The presented solution shows the potential to improve thermal performance with a lower level of system complexity and lower overhead for coolant and fabrication. To the author's knowledge, the thermal resistance results are the lowest reported (0.015 K/W) in the area of single-phase cooling research.

**Keywords**— *Non-uniform heat flux, Hotspot, Jet Impingement, SLM, Direct cooling, Micro pin fin.*

## Nomenclature

|            |                                          |
|------------|------------------------------------------|
| $A$        | Area ratio ( $A_{jet}/A_{HS}$ )          |
| $c_p$      | Specific heat capacity ( $J/kg.K$ )      |
| $D_h$      | Hydraulic diameter ( $m$ )               |
| $K$        | Thermal conductivity ( $J/m.K$ )         |
| $\dot{m}$  | Mass flow rate ( $kg/s$ )                |
| $P$        | Pressure ( $Pa$ )                        |
| $Q$        | Coolant volumetric flow rate ( $m^3/s$ ) |
| $\dot{q}$  | Chip power ( $W$ )                       |
| $R_{th}$   | Thermal resistance ( $K.m^2/W$ )         |
| $Re$       | Reynolds number                          |
| $T$        | Temperature ( $K$ )                      |
| $u$        | Velocity ( $m/s$ )                       |
| $k$        | Turbulent kinetic energy ( $m^2/s^2$ )   |
| $\sigma_k$ | Diffusion Prandtl number for $k$         |
| $C_1$      | Turbulent model constant                 |
| $C_2$      | Turbulent model constant                 |
| $x$        | Coordinate ( $m$ )                       |
| $H$        | jet nozzle-to-chip spacing ( $mm$ )      |
| $V$        | Volume ( $mm^3$ )                        |

## Greek symbols

|               |                                                 |
|---------------|-------------------------------------------------|
| $\varepsilon$ | Rate of dissipation of turbulent kinetic energy |
| $\mu$         | Absolute viscosity ( $kg/m.s$ )                 |
| $\rho$        | Density ( $kg/m^3$ )                            |
| $\psi$        | Chip temperature non-uniformity                 |
| $\xi$         | Pin fin effectiveness                           |

## Subscripts

|            |                            |
|------------|----------------------------|
| <i>TIM</i> | Thermal interface material |
| <i>in</i>  | Inlet                      |
| <i>S</i>   | Solid                      |
| <i>th</i>  | Thermal                    |
| <i>ch</i>  | Chip                       |

## I. INTRODUCTION

Ever shrinking electronic chips play a critical role in the launch of innovative new products of the modern world. Thermal management of these electronic chips is a primary challenge given the exponentially increasing heat fluxes. Numerous articles have been written detailing the limits of cooling techniques for electronic systems including [1]–[5] among others. Single-phase liquid cooling, either using a microchannel or pin fins, is one of the most widely explored liquid solutions due to its excellent cooling performance and relatively uncomplicated manufacturing [6]–[9]. However, most thermal solutions only consider uniform thermal power maps, which will not be relevant for the future generation of microprocessors. Since 2004, processor designers have increased core counts to exploit Moore's Law scaling, rather than focusing on single-core microprocessors [4, 5]. Invariably, cores generate multiple times the heat flux of the rest of the chip, resulting in a highly non-uniform chip power map. The extreme concentration of heat flux in cores can induce higher temperatures and thermal gradients at the surface of the chip, which is undesirable for many reasons. First, a higher temperature can reduce the efficient functional life of a chip and compromise reliability by accelerating temperature dependent failure mechanisms [12]–[15]. Heterogeneous chip and package architectures are more likely to be affected by large thermal gradients, particularly 3-dimensional chip stacks. Second, higher temperatures at a high heat flux area can induce the thermal management problem by increasing overall power consumption. In this article, the term "hotspot" refers to the chip areas with an elevated power dissipation. A hotspot's heat flux reaches up to eight times the average background heat flux [10, 11]. The ability to alleviate hotspots has recently been the focus of much research, since it is critical for emerging designs to achieve solutions can control both the average chip temperature and specific hotspot cooling. To ensure efficient performance of a microprocessor, the temperature at the chip surface must be maintained below 100 °C [18]. To tackle this problem, different approaches to non-uniform cooling, which is also known as hotspot-targeted cooling, must be explored. Thermal management of heat fluxes of up to 790 W/cm<sup>2</sup> was demonstrated over 25 years ago in Tuckerman and Pease's pioneering work on microchannel heat sinks [6]. Further studies involving passive hotspot targeted single-phase liquid cooling have also been reported [19]–[21]. C. S. Sharma et al.

experimentally studied the thermo-hydraulic performance of a hotspot-targeted liquid cooled device for multicore microprocessors with an average heat flux of 300 W/cm<sup>2</sup> in hotspot areas (hotspots) and 24.2W/cm<sup>2</sup> over the background chip area. To regulate the distribution of flow in different regions of the chip, the authors used the concept of channel granularity (fine and coarse) and a flow throttling zone. Their design showed better thermal and energy efficient results [22]. Y. Hadad et al. [23] numerically demonstrated how a novel microchannel cold plate remotely cooled a single hotspot using an optimized flow distribution under constrained geometric parameters. The authors showed that concentrating the flow on small areas of hotspot resulted in a more uniform chip temperature. D. Ansari and K.Y. Kim [24] designed a microchannel-pin fin hybrid heat sink to cool a microprocessor with a single hotspot at its center. The authors accomplished a thermal study based on the calculated temperature at the base of the heat sink. Their hybrid design indicated a lower temperature rise at the hotspot and a lower thermal resistance at an acceptable expense of the pumping power when compared to a microchannel non-hybrid heat sink. Ravi S. Prasher et al. [25] experimentally studied a microchannel heat sink using two-phase convective boiling to alleviate a 400  $\mu$ m  $\times$  400  $\mu$ m hotspot. The authors showed that fluctuation in the wall temperature was different with non-uniform heating conditions than with uniform heat flux. Unfortunately, the difficulty of modeling and fabricating two-phase cooling systems limits their implementation in the electronics industry.

Thermo-electric (Peltier) coolers (TEC) is one of the hotspot cooling approaches that focuses on the use of the Peltier effect to develop a hotspot-targeted solid-state thermoelectric cooling system [26]–[30]. Sahu et al. [31] successfully applied a hybrid cooling scheme that combined a microfluidic and solid state to remove a localized hotspot with a heat flux close to 250 W/cm<sup>2</sup>. In another study, Sahu et al. [32] showed that a liquid thermoelectric hybrid cooling method had the potential to dissipate hotspot with heat fluxes of more than 600 W/cm<sup>2</sup>. Yet, the TEC approach has its own drawbacks, such as complexity of design, higher cost, low coefficient of performance, and the limitations related to contact parasitic resistance [33].

Recently, new solutions for hotspot alleviation was proposed using separated coolants for hotspot and background area. Craig Green et al. proposed a fluid-to-fluid spot to spreader (F2S2) hybrid heat sink. Their proposed design coupled two thermal fluids to remove hotspots with heat fluxes of 1 kW/cm<sup>2</sup> and background heat fluxes up to 100 W/cm<sup>2</sup> in one compact and efficient package [34]. Reza Abbaspour et al. [35] fabricated a microfluidic two stream heat sink embedded in a silicon substrate to address hotspot high heat removal. However, their combined two-phase flow strategy required complex microfabrication approaches and a higher pressure drop.

Having spreaders or thermal interface materials (TIM) can laterally transfer heat from the hotspots toward colder areas of the chip that are subjected to lower heat flux [36], [37]. C. Bachmann and A. Bar-Cohen studied the potential of a hybrid approach that used a TIM or spreader with anisotropic thermal conductivity to remedy the effect of a single hotspot [38]. Hongtao A. Guo et al. [39] studied the impact of hotspot size on the conductive heat spreading. The authors developed an

approximate solution that accounted for the variable center hotspot size for both isotropic and orthotropic spreaders. However, even well-designed chip scale heat removal systems must consider and reduce the deleterious interfacial contact resistance that arises upon physical attachment of an anisotropic spreader to the silicon chip.

A hot spot can also be cooled using a jet impingement scheme, utilizing either a single jet or an array of multiple jets located directly above the hotspot. For efficient thermal management of a chip with hotspots, one of the promising solutions is to define multiple zones, with low cooling capacity for the background area and high cooling capacity for hotspots. This solution takes advantage of the increased heat transfer coefficient in the impingement zone by making it so that the hotspot can lay directly under the impinging jet inlet [40]–[42].

In this work, a novel single-phase cooling technology, which is hot spot targeted and compact, is presented for use in current and future high heat flux non-uniform electronic chips. The study explores the thermo-hydraulic performance of a design with chip attached micro pin fins and liquid jet impingement that directly cools four electronic chips simultaneously. This cooling concept eliminates the need for TIMs and delivers the coolant directly onto the chip's surface [43]. The theoretical capabilities of the cooling device are explored through computational fluid dynamics (CFD) simulations.

## II. PROBLEM DESCRIPTION

Figure 1 shows the non-uniform heat power map of a multicore chip with eight cores. The red regions represent hotspots dissipating  $800 \text{ W/cm}^2$  heat flux, while the orange region represents the chip background with a heat flux of  $150 \text{ W/cm}^2$ . As shown in the figure, the chip consists of eight hotspots that occupy almost 17% of the total chip area. The heat flux dissipating from the hotspots (HS) is approximately 5.3 times that of the background region (BG). The schematic of solution design is shown in Figure 2. Note that the schematic figures depicted in this study are not drawn to scale, since the dimensions have been exaggerated to make them easier to see. Starting at the bottom, a square PCB layer provides a foundation for four separate chips. Next, silicon chips with printed micro pin fins are attached on top of PCB layer. Micro pin fins with square cross section are uniformly distributed onto every chip. Printing micro pin fins on the chip eliminates the contact and sequential conduction resistances induced by a thermal interface material, base, or spreader. A plastic sidewall is used as a pillar to hold the top layer, which includes inlets and outlets. The inlet nozzles sit above the HS zones to take advantage of impingement jet cooling over the cores (Figure 3). To maintain a uniform temperature on the chip surface and keep the heat transfer coefficient as homogeneous as possible, each inlet includes an array of several micro jets. It is worth noting that there is no gap between the tip of the pin fins and the plastic cover. One of the potential obstacles of a single jet design is the high flow rate needed to remove the high heat fluxes. In a multiple micro jet design, this constraint is potentially removed, given that each jet is smaller and requires a lower flow rate than that of a single large jet. Limitations of the design are categorized in Table 1. This single package concept makes it possible to cool four high heat flux chips in a smaller constrained

area, potentially eliminating the geometrical limitation of the traditional cold plate designs.

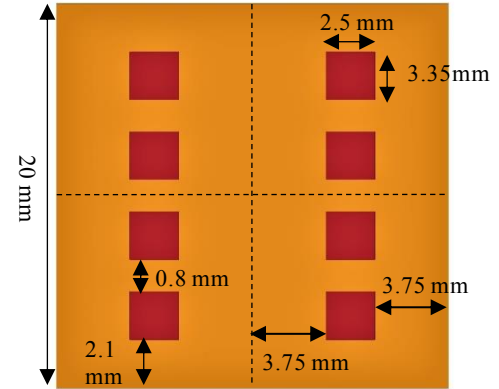


Fig. 1. The schematic view of the non-uniform heat power map of a multicore chip with 8 cores.

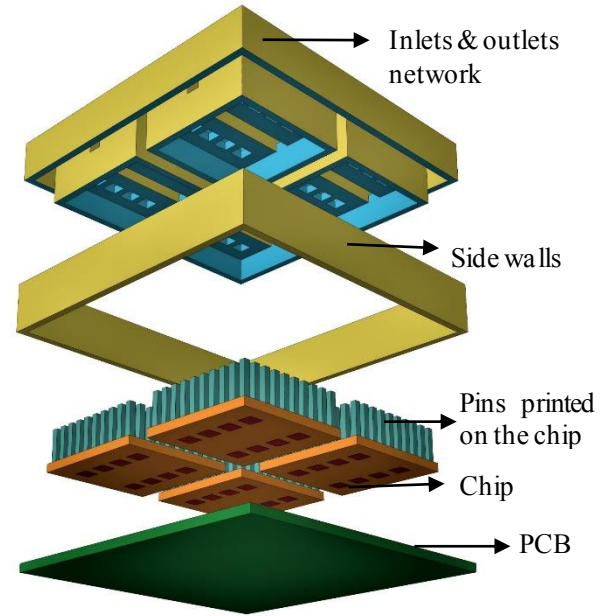


Fig. 2. The schematic view of the hotspot targeted impinging chip-attached micro pin fin cooling package.

## III. NUMERICAL ANALYSIS

The governing equations of mass, momentum, and energy are applied with the following basic assumptions:

- Three dimensional, incompressible, and steady state single-phase flow.
- The gravity forces are considered.

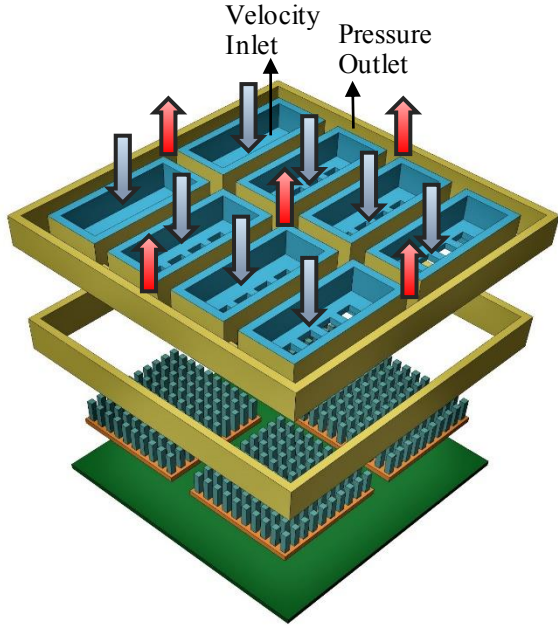


Fig. 3. The schematic view of inlets and outlet of the hotspot targeted impinging chip-attached micro pin fin cooling package.

- Temperature dependent thermo-physical properties of the coolant is applied to the model.
- Viscous heat generation is negligible.
- Negligible contract resistance at the interfaces between the coolant and solid wall.

TABLE I. GEOMETRIC PARAMETERS OF THE PREDEFINED DESIGN

| Symbol           | Definition                | Value      |
|------------------|---------------------------|------------|
| $t_{chip}$       | Chip thickness            | 0.5 (mm)   |
| $W_{chip}$       | Chip width                | 20 (mm)    |
| $W_{PCB}$        | PCB width                 | 48 (mm)    |
| $t_{wall}$       | Walls thickness           | 0.5 (mm)   |
| $P_p$            | Pin fin pitch             | 0.6 (mm)   |
| $t_p$            | Thickness of pin fin      | 0.4 (mm)   |
| $w_{ch}$         | Inter-fin spacing         | 0.2 (mm)   |
| $T_{in}$         | Coolant inlet temperature | 295 (K)    |
| $\dot{q}_{chip}$ | Chip total power          | 1035.5 (W) |

#### A. Governing equations

Due to high Reynold number at jet inlet ( $>2300$ ), the  $k-\epsilon$  model and the standard wall function are used to describe the turbulent effects of the jets. Governing equations of a numerical solution for a 3D, incompressible, steady turbulent flow regime and single-phase model are as follows:

Continuity equation:  $\frac{\partial \rho_f \bar{u}_i}{\partial x_i} = 0$  (1)

Fluid momentum:

$$\rho_f \bar{u}_j \frac{\partial \bar{u}_i}{\partial x_j} = -\frac{\partial p}{\partial x_i} + \frac{\partial}{\partial x_j} \left[ (\mu + \mu_t) \left( \frac{\partial \bar{u}_i}{\partial x_j} + \frac{\partial \bar{u}_j}{\partial x_i} \right) \right] \quad (2)$$

$$\text{Energy equation for fluid: } \rho_f \bar{u}_j \frac{\partial T}{\partial x_j} = \frac{\partial}{\partial x_j} \left[ \left( \frac{\mu_t}{\sigma_t} + \frac{\mu_t}{\sigma_r} \right) \frac{\partial T}{\partial x_j} \right] \quad (3)$$

$$\text{Energy equation for solid: } \frac{\partial}{\partial x_i} \left[ k_s \frac{\partial T}{\partial x_i} \right] = 0 \quad (4)$$

Transport equation for turbulence kinetic energy:

$$\rho \bar{u}_j \frac{\partial k}{\partial x_j} = \frac{\partial}{\partial x_j} \left[ \left( \mu + \frac{\mu_t}{\sigma_k} \right) \frac{\partial k}{\partial x_j} \right] + \mu_t \left[ \frac{\partial \bar{u}_i}{\partial x_j} + \frac{\partial \bar{u}_j}{\partial x_i} \right] \frac{\partial \bar{u}_i}{\partial x_j} - \rho \epsilon \quad (5)$$

Transport equations for turbulence kinetic energy dissipation:

$$\rho \bar{u}_j \frac{\partial \epsilon}{\partial x_j} = \frac{\partial}{\partial x_j} \left[ \left( \mu + \frac{\mu_t}{\sigma_\epsilon} \right) \frac{\partial \epsilon}{\partial x_j} \right] + C_1 \mu_t \frac{\epsilon}{k} \left[ \frac{\partial \bar{u}_i}{\partial x_j} + \frac{\partial \bar{u}_j}{\partial x_i} \right] \frac{\partial \bar{u}_i}{\partial x_j} - C_2 \rho \frac{\epsilon^2}{k} \quad (6)$$

#### B. Boundary conditions

Due to symmetry boundary conditions in both the physical geometry of interest and the expected pattern of the flow/thermal solution, the 1/4 of a unit cell of the cooling assemblage is simulated and solved. Surrounding wall surfaces are adiabatic. Coolant-solid interfaces are no-slip boundary and:

$$-k_l \frac{\partial T_l}{\partial x} = -k_s \frac{\partial T_s}{\partial x} \quad (7)$$

At the velocity inlet, the inlet temperature coolant and flow rate are defined. The pressure at the outlet is defined to be zero.

#### C. Numerical approach

The discretization of the equations of motion and energy are performed using the finite volume method in the domain analysis on a staggered grid. The stop residual for the function of temperature is set to 0.0002 as a convergence criterion. The residual of the other functions,  $k$ ,  $\epsilon$ , velocity and pressure are 0.0005. To assess the accuracy of these computations based on the computational grids, the grid independence of the solution is tested. A grid study analysis (Figure 4) shows that the pressure drop and thermal resistance of 30M vary from those of 25M within 1.2% and 0.6%, respectively. This indicates that grid number 25M will ensure a satisfactory numerical solution. The commercial program 6Sigma ET is employed as the numerical solver.

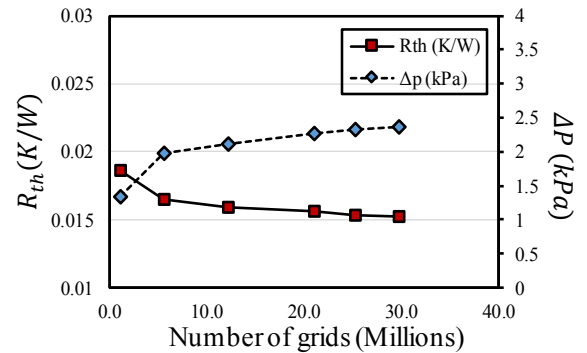


Fig. 4. The results of grid resolution based on thermal resistance and pressure drop.

#### D. Material properties

The coolant used in this study is water with an inlet temperature of 295 K. Micro pin fins made of copper are printed

onto the surface of the silicon chip. Note, this study's trends and general geometry also apply to aluminum. For the PCB material, FR4 is selected because of its versatility and affordability in manufacturing.

#### IV. RESULTS AND DISCUSSION

In the first step of assessing the thermal performance of the cooling device, it is important to determine the thermal resistance required to satisfy the thermal criteria of its components. The thermal resistance of the cooling device can be defined by:

$$R_{th} = \frac{T_{Max}^{ch} - T_{in}}{\dot{q}_{chip}} \quad (8)$$

Where,  $T_{Max}^{ch}$  and  $T_{in}$  are the maximum temperature of a chip and inlet temperature of coolant, respectively. The second parameter is the pressure differences between the inlet and outlet of the cooling device ( $\Delta P$ ).

$$\Delta P = P_{out} - P_{in} \quad (9)$$

In this study, the pressure at the outlet is assumed to be zero. In addition to the thermal resistance and pressure drop, the chip temperature non-uniformity is evaluated. High temperature non-uniformities can cause large thermal expansion gradients and induce thermal stresses to the chip and other substrates, thus reducing the chip's efficient functional life, and creating differential aging and circuit imbalances. The temperature non-uniformity ( $\psi$ ) is defined as:

$$\psi = \frac{T_{Max}^{ch} - T_{Min}^{ch}}{T_{in}} \quad (10)$$

Pin fin effectiveness is defined as the ratio of the temperature gradient with pin fins to that of the same surface without pin fins.

$$\epsilon_p = \frac{\Delta T_{pins}}{\Delta T_{without pins}} = \frac{T_{max}^{chip with pins} - T_{in}}{T_{max}^{chip without pins} - T_{in}} \leq 1 \quad (11)$$

The value of  $\epsilon_p$  is always in the range of variation [0, 1]. The lower  $\epsilon_p$  the more effective the pin fins are. Pin fin effectiveness for the design with a jet-to-chip spacing of 4mm, jet nozzle size of 3.35 mm x 2.5 mm, pin cross section of 0.4 mm x 0.4 mm, and pin pitch of 0.6 mm, is calculated as 0.31.

In the results that follow, it is presumed that each water jet exits its nozzle with a 3.35mm x 2.5 mm cross section, uniform flow rate of 0.4 LPM, temperature  $T_{in}$  and is perpendicular to the flat silicon chip. Figures 5 and 6 illustrate the effect of jet-to-chip spacing ( $H$ ) on the thermal and hydraulic performance of the cooling package. For a fixed Reynolds number of 2336 at each individual HS jet, the thermal resistance deteriorates monotonically as the jet-to-chip spacing increases. For smaller  $H$  values, a stronger dependence of the thermal performance and pressure drop on jet-to-chip spacing is observed. Figure 6 shows that both chip temperature non-uniformity and thermal resistance follow the same trend with decreasing  $H$  values. Reducing the  $H$  value from 5 to 1 mm results in a 48 % improvement in temperature non-uniformity. The temperature profile of Figure 7 shows that optimizing the  $H$  value can

eliminate the effects of HS. The fact that small jet-to-chip spacing can ensure that the jets reach the HS surface before mixing with the pin fin's crossflow can explain why thermal resistance decreases while the  $H$  value increases. A higher  $H$  value allows the jet to mix with the recirculation flow before reaches the hotspot surface. Another important factor that needs to be considered is the crossflow velocity. For smaller  $H$  values, heat transfer is enhanced for part of the pin fin flow because the crossflow velocity is higher. Since there is no gap between the tip of the pin fins and the plastic cover, pin fins height changes occur simultaneously with  $H$  variation. The heat transfer surface area competes with the flow. Both these factors contribute to the heat transfer coefficient. In this study, based on the results, flow is the more influential than surface area.

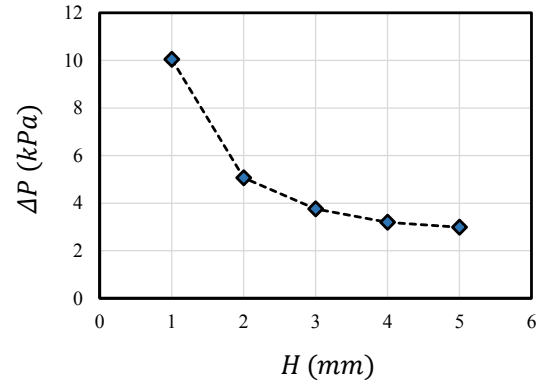


Fig. 5. The effect of jet-to-chip spacing on the pressure drop of cooling package.

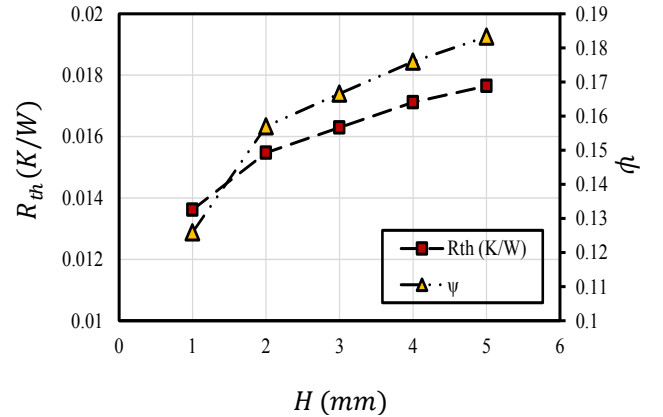


Fig. 6. The effect of jet-to-chip spacing on the thermal resistance and temperature non-uniformity of the cooling package.

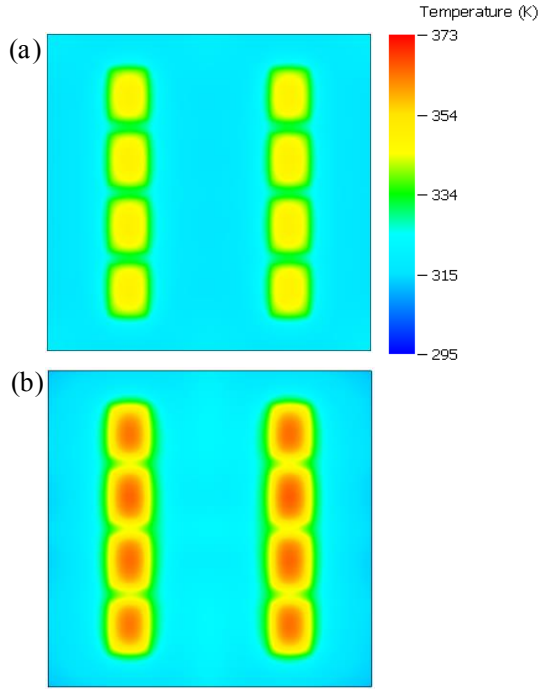


Fig. 7. a) Temperature profile of design case with  $H=1\text{ mm}$ , b) Temperature profile of design case with  $H=5\text{ mm}$  at the back surface of chip.  $H=5\text{ mm}$  at the back surface of chip.

Figure 8 shows the effect of a non-dimensionalized jet inlet size  $A = \frac{A_{jet}}{A_{HS}}$  on the pressure drop in a cooling package with  $H = 3\text{ mm}$ . Decreasing the non-dimensionalized inlet jet size from 1.29 to 0.33 results in a 4 K reduction in the chip's maximum temperature. The effect of  $A$  on the thermal performance is more evident in figure 9. This is attributed to the fact that smaller inlets produce a higher mean velocity and higher heat transfer coefficient. However, a jet inlet with an  $A$  of less than 0.5 unexpectedly pressure drop increases, which conflicts with the hydraulic performance and efficiency of the system.

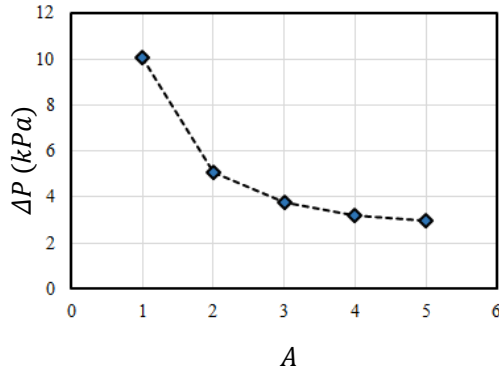


Fig. 8. The effect of inlet size on the chip's maximum temperature and pressure drop of cooling package with  $H=3\text{ mm}$ .

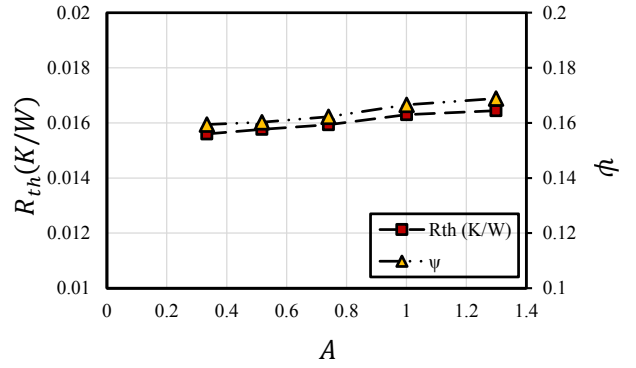


Fig. 9. The effect of jet inlet size on the thermal resistance and temperature non-uniformity of the cooling package with  $H=3\text{ mm}$ .

## V. FABRICATION PROCESS

An experiment is designed to demonstrate direct fabrication of pin fins onto chip by additive laser metal deposition. The fundamentals of this process were previously explained by the authors [44]–[48]. A mock package was used for this study, which consists of a  $1\times 1$ -inch silicon die in a flip chip configuration. The experiment was performed in a EOS M290 laser powder bed fusion system at The State University of New York At Binghamton. To accommodate the mock chip, a Computer Numerical Control (CNC) machine was used to create a custom aluminum alloy build platform and electronic package holder (Figure 10a, b, c). The chip was secured in the sample holder by Kapton® polyimide tape (Figure 10d). The print process consisted of two main stages. In the first stage,  $20\mu\text{m}$  of Sn3Ag4Ti powder was deposited onto the silicon die by a carbon fiber brush recoater blade (Figure 11a). The powder consisted of pure tin, silver, and titanium powders, which were mechanically mixed. After deposition, the build chamber was

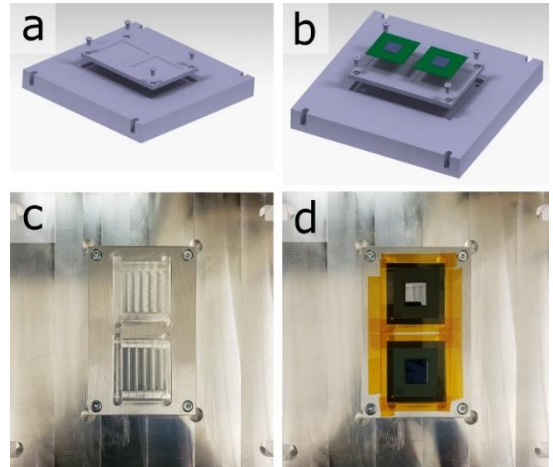


Fig. 10 a,b) Computer aided design (CAD) of the custom-made build platform and sample holder c) computer numerical controlled (CNC) machined build platform and sample holder d) mock chip secured on the sample holder by the Kapton® polyimide tape

purged with argon to reach an oxygen concentration of less than 0.1%. Finally, the deposited powder was scanned by the laser beam in a pattern defined earlier in the EOSPRINT software [49]. The pattern consisted of circles with a diameter of 500  $\mu\text{m}$  and center-to-center distance of 800  $\mu\text{m}$  in both the X and Y directions across the die (Figure 11b). The hatch distance, laser power, and scanning speed used for this process were 0.09 mm, 120 W, and 1700 mm/s with a double exposure strategy [44]. A second layer of Sn3Ag4Ti powder was deposited and exposed to the laser with the same process. In the second stage, the pin fins were fabricated via SLM. An aluminum alloy (AlSi10Mg) was used for this process, since it has a relatively high thermal conductivity the common alloys used in the SLM process [50]. Through the SLM process, 400  $\mu\text{m}$  diameter AlSi10Mg pins were fabricated onto the Sn3Ag4Ti circular interlayers that were

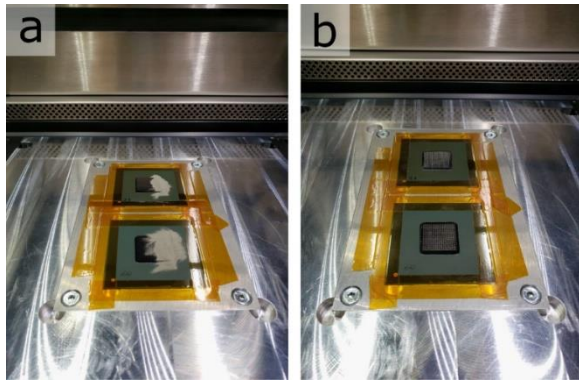


Fig. 11 a) Sn3Ag4Ti powder before deposition by the brush blade recoater b) selective laser melted Sn3Ag4Ti circular patterns with diameter of 500  $\mu\text{m}$  and center-to-center distance of 800  $\mu\text{m}$

made in the first stage. A combination of skin and post contour exposures (EOS terminology) were used for this stage. Finally, an aluminum alloy fins with a height of 8 mm (aspect ratio of 1:20) were fabricated onto the mock package (Figure 12a & b). It should be noted that such an aspect ratio is extreme, and the purpose of this experiment was to demonstrate the capability of this process. However, in liquid cooling application, such tall fins are not required as the effective length of the fin is much shorter based on our numerical simulations [43]. Adoption of this method for large scale production requires some iterations in the module level and system level production and assembly processes. By this method, the heat removal device (i.e., heat sink or cold plate) is manufactured directly onto the chip as opposed to conventional thermal management configurations, in which the cooling device is attached to the die or heat spreader with the TIM. The main required integration includes adding a SLM system capable of handling electronic packages. The cost of an industrial SLM printer currently varies approximately between \$300k-\$2M based on manufacturer and capabilities. Printers are currently being used primarily for part production for the medical and aerospace industries. Some modifications to such systems including package handling in addition to mounting on a special build platform is necessary for semiconductor processing in bulk. The print time is a function of the powder layer height, powder deposition speed, 3d printed

part's total height and the total part volume. The typical volumetric print rates are between 20-100  $\text{cm}^3/\text{hr}$  of solidified material and can handle features down to 100  $\mu\text{m}$ , though in theory can be reduced down to 1  $\mu\text{m}$ . The economics of this process depends on the machine cost, machine volumetric print rate, the metal powder costs, maintenance, and operation labor. Unlike conventional machining, complicated geometries such as lattice structures are achievable in the same time as simpler structures of the same print volume. As a result, this process would initially be of greatest interest towards high-end applications that require chips with high heat fluxes where

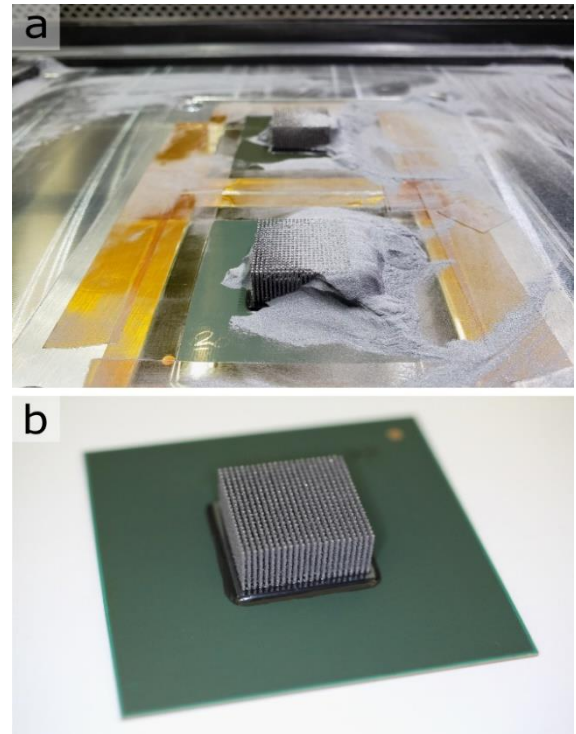


Fig. 12 a) AlSi10Mg fins fabricated by selective laser melting with powder has not been fully removed from the build platform and sample b) mock chip with 8 mm tall aluminum alloy fins with the diameter of 400  $\mu\text{m}$  (aspect ratio 1:20)

conventional methods of cooling with TIMs, both single phase and two-phase, are either too high thermal resistance or too bulky compared to conventionally machined or skived heat sinks.

## CONCLUSION

This study provides the framework for a promising new design concept of a fluid-thermal cooling solution for the next generation of electronics thermal management. The solution design combines chip-level and hotspot-level cooling to address high density and non-uniform heat dissipation in a CPU package. The effects of nozzle cross section and jet-to-chip spacing on heat transfer and fluid flow are investigated for multiple turbulent jets impinging on a flat surface at a non-uniform heat flux boundary condition. The results show that:

- For a fixed Reynolds number of 2336 at each individual HS jet, the thermal resistance deteriorates monotonically as the jet-to-chip spacing increases.
- Reducing the H value from 5 to 1 mm results in a 48% improvement in temperature non-uniformity.
- Flow is the more influential than surface area.
- Decreasing the non-dimensionalized inlet jet size from 1.29 to 0.33 results in a 4 K reduction of the chip maximum temperature.
- For the proposed case, jet-to-chip spacing is more prominent parameter than jet diameter.

However, a jet inlet with an A of less than 0.5 unexpectedly increases pressure drop value, which conflicts with the hydraulic performance and efficiency of the system

Furthermore, the presented solution shows a highly improved thermal performance with a lower level of system complexity and less overhead from the cost of coolant and fabrication. For further research, the mechanical reliability of printed pin fins and experimental validation of the CFD results from this study will be performed.

#### AUTHORS AND AFFILIATIONS

B.G. and S.N.S conceived the initial idea of this research and guided the work. V.R. developed the numerical model and performed all simulations and analysis. S.R., N.F., C.H.H., G.M., K.N. contributed towards numerical analysis and discussion. A.A. designed and developed the SLM process, fabricated the samples, and provided the technology adoption overview. All authors contributed to the writing of this paper.

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