$SrSnO_3$ Metal-Semiconductor Field-Effect Transistor with GHz Operation

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***Abstract*—A $SrSnO_3$ high-frequency field-effect transistor (FET) is demonstrated. The device structure consists of a recessed Schottky-gate FET with a heavily doped cap layer. DC measurements on devices with 0.5-μm gate length and 4-μm source/drain spacing show a maximum drain current of 53 mA/mm and a maximum transconductance of 43.2 mS/mm. Radio frequency (RF) characterization reveals a cut-off frequency, f_T, of 1.31 GHz (0.97 GHz) and a maximum oscillation frequency, f_{max}, of 3.25 (3.25) GHz, after (before) de-embedding. These results represent an important advancement in developing perovskite materials for RF applications.**

***Index Terms* – MESFET, Perovskite, Stannate, $SrSnO_3$, RF**

I. INTRODUCTION

Perovskite-structured ABO_3 oxides are promising multi-functional materials with interesting physical properties such as thermoelectricity, superconductivity, and ferromagnetism, among others [1-4]. Using perovskites as channel materials for electronic devices makes use of their relatively wide bandgap and at the same time opens up the possibility of integration with other functional perovskite oxides with interesting properties. $SrSnO_3$ (SSO) has emerged recently as a particularly interesting perovskite material for use in field-effect transistors (FETs) due to its combination of large bandgap of 4-5 eV [5-7] and high room-temperature electron mobility up to 70 cm^2/Vs [8-12], which is roughly 10× higher than d-band perovskites such as $SrTiO_3$ (< 10 cm^2/Vs) [13].

An early demonstration of an SSO FET was reported in 2018 [14]. This device, configured in a metal-semiconductor FET (MESFET) geometry, achieved a drive current of 36 mA/mm and a peak extrinsic transconductance, g_{mext}, of 17 mS/mm with a gate length of 3 μm and a source/drain (S/D) spacing of 9 μm. Subsequent optimization of the device geometry using a recessed-gate structure to decrease access resistance resulted in a peak transconductance of 73 mS/mm in a 0.5-μm gate-length device [15]. This performance is comparable to the best FETs made from $BaSnO_3$ [16], another high-mobility perovskite with a lower bandgap, and roughly 15× higher transconductance than comparable FETs made from $SrTiO_3$ [17]. This performance suggests that SSO devices might be suitable for operation at RF frequencies, yet the high-frequency performance of SSO FETs has yet to be studied. In fact, to our knowledge, only one study of RF performance on perovskite-based FETs has been reported in the literature to date. In that work [18], the frequency performance of all-oxide FETs on $LaAlO_3/SrTiO_3$ channels was reported. Those devices had extrinsic cut-off frequency, f_T, and maximum oscillation frequency, f_{max}, of 13.5 MHz and 28.8 MHz, respectively. These modest values are a result of the low mobility in $SrTiO_3$, as well as the relatively long gate length of 4 μm.

In this work, we fabricate and demonstrate RF SSO MESFETs with bi-layer SSO films grown by radical-based hybrid molecular beam epitaxy (MBE) with GHz-level performance. We utilize the same recessed-gate structure

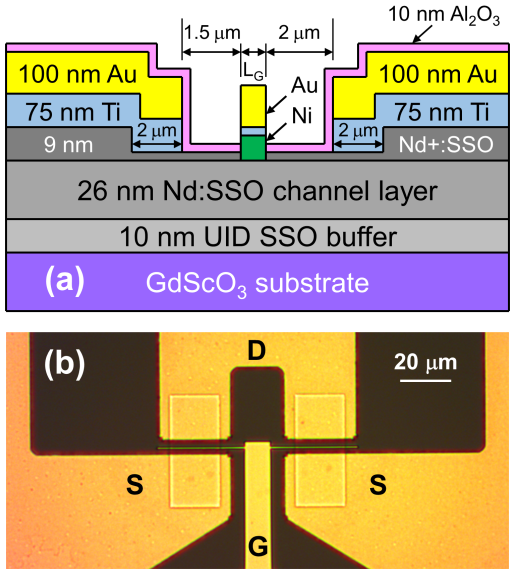

FIG 1. (a) Cross-sectional schematic of the SSO MESFET after fabrication. The relevant lateral dimensions are depicted, where the source (drain) is on the left (right) side. (b) Optical image of the RF SSO MESFET with L_G = 0.5 μm, L_{DS} = 4 μm and W_G = 2 × 20 μm in a GSG configuration.

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described in [15], but utilize devices configured in a ground-signal-ground (GSG) geometry for the purpose of RF characterization. These devices, with gate length, L_G, of 0.5 µm and a S/D spacing of 4 µm, have f_T = 1.31 GHz and f_{max} = 3.25 GHz after de-embedding.

II. DEVICE FABRICATION

The thin-film growth process is the same as that used in [15]. The epitaxial SSO films used in this work consisted of a 10 nm unintentionally-doped (UID) SSO, a 26 nm Nd:SSO channel layer and a 9 nm Nd^+:SSO cap layer grown on the top of a highly insulating $GdScO_3$ substrate by radical-based hybrid MBE technique [9],[19]. The channel layer has an effective doping concentration of 2.3 × 10^{19} cm^{-3} and mobility of 28 cm^2/Vs according to separate van der Pauw measurements performed on a 26 nm single layer SSO sample grown under the same Nd source temperature. The same measurement was not directly performed on the heavily doped cap layer, however, the doping concentration is expected to be > 10^{20} cm^{-3}.

The MESFETs fabrication also followed the procedure in [15]. After mesa isolation, the devices underwent an initial recess process, where a portion of the heavily doped cap layer, 2 µm larger than the source and drain spacing on each side, was partially etched by reactive ion etching (RIE). Ti (75 nm) / Au (100 nm) metallization was then evaporated and lifted off to form source and drain contacts. Next, a 10-nm Al_2O_3 passivation layer was deposited using atomic layer deposition, followed by the gate lithography, a wet-etch to remove the Al_2O_3, and a second RIE to remove the remaining ~3 nm heavily doped layer under the gate. Finally, the gate metal consisting of Ni (65 nm) / Ti (10 nm) / Au (80 nm) was evaporated and lifted off. The separation of the S/D Ohmic contacts, L_{DS}, was 4 µm, and L_G was 0.5 µm, where the gate was offset by 0.25 µm closer to the source, to decrease the parasitic source resistance. The device was arranged in a GSG configuration for RF characterization and had a total gate width 40 µm (2 × 20 µm). A schematic cross-sectional diagram and top-view micrograph of the completed device are shown in Figs. 1(a) and 1(b), respectively.

III. RESULTS

The DC measurements were performed in vacuum at room temperature using a Keysight B1500A semiconductor parameter analyzer. Two sets of DC measurements, one right before and one immediately after RF measurement, were performed and the results are shown in Fig. 2. Prior to RF characterization, the SSO MESFET showed good saturation in its output characteristic with peak drive current of 53 mA/mm and a low output conductance, g_o, of 4.2 mS/mm. The transfer characteristic showed slightly depletion-mode behavior, with a threshold voltage of –0.9 V. While a peak in g_{mext} is not obtained, g_{mext} reached a maximum value of 43.2 mS/mm at V_{GS} = +1 V and V_{DS} = +3 V. Compared to the results above, the DC measurements performed after the RF measurements had a more negative threshold of –2.7 V, along with a softer turn-off behavior. The maximum drive current was 87 mA/mm, with the peak g_{mext} 32.6 mS/mm.

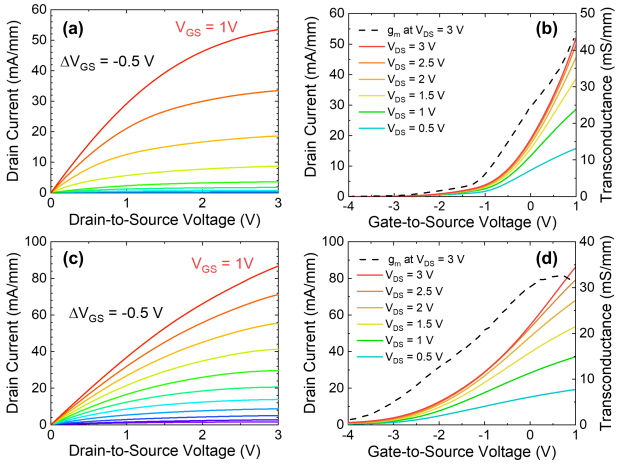

FIG 2. (a) Output characteristic and (b) transfer characteristic for the SSO MESFET with L_G = 0.5 µm and L_{DS} = 4 µm before RF measurements; (c) Output characteristic and (d) transfer characteristic for the same device after RF measurements.

While the results in Fig. 2 show that the device has some degree of threshold instability, they provide a general guide for understanding the RF measurement results. We believe the DC measurements performed prior to the RF characterization shown in Figs. 2 (a)-(b) are more reflective of the device state during RF characterization, as we will show later. While previous devices with Ni gates showed good threshold stability when measured at relatively low V_{DS} values [15], the devices reported here showed a higher degree of drift, similar to the Pt-gate devices reported in [15]. While the origin of this phenomenon requires further study, we do note that the devices in Fig. 2 had been exposed to air for an extended period between fabrication and measurement.

Two-port RF characterization was performed in air at room temperature using a Keysight E5063A vector network analyzer (VNA) with frequency ranging from 100 kHz to 18 GHz. The two ports on the VNA were to the gate and drain terminals. A bias tee was employed to mix the DC bias and RF input on each port. The VNA was calibrated using on-wafer open-short-load-thru structures on an impedance-standard substrate. In order to deembed extrinsic elements, s-parameter measurements on dummy open and short pad structures was performed. The short-circuit current gain (h_{21}) and Mason's unilateral gain (U) vs. frequency at V_{DS} = +3 V and two different V_{GS} values are

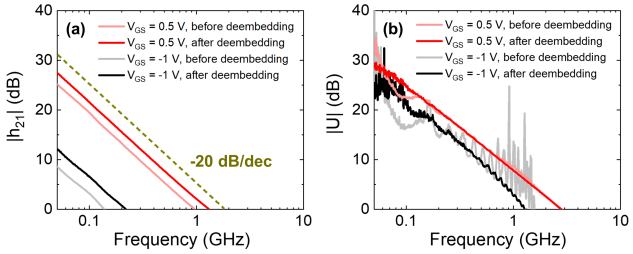

FIG 3. (a) $|h_{21}|$ and (b) $|U|$ vs. frequency before and after deembedding at V_{DS} = +3 V and two different V_{GS}. Note that at V_{DS} = +3 V and V_{GS} = +0.5 V the device shows maximum intrinsic f_T of 1.31 GHz. Deembedding minimizes the reflections in the $|U|$ plot, especially for lower V_{GS}.

shown in Fig. 3 as an example. Results before and after deembedding are shown. The low-frequency reflections on the $|U|$ vs. f plot are minimized after deembedding. We note that the extracted f_{max} does not change much after deembedding, while f_T has a slight increase, a phenomenon that happens for all bias conditions. The relatively small change in f_T and f_{max} is expected considering the relatively large device dimensions and the insulating nature of the $GdScO_3$ substrate.

The deembedded $|h_{21}|$ and $|U|$ values at $V_{DS} = +3$ V are plotted vs. frequency in Figs. 4(a) and 4(b), respectively. The current gain rolls off close to −20 dB/decade, as expected. The extracted f_T and f_{max} under different values of V_{DS}, before and after deembedding, are plotted vs. V_{GS} in Figs. 4(c) and 4(d), respectively. The degradation of f_T with decreasing V_{GS} is consistent with the g_{mext} trend from the pre-RF DC data (Fig. 2(b)), supporting our earlier statement that the DC measurements taken prior to RF characterization more closely reflect the device state during the RF measurements.

We also extracted the total gate capacitance, C_{gg}, and the high-frequency intrinsic g_m, using the (deembedded) s-parameter data. These results, shown in Table I below, provide a clearer explanation for trends in Fig. 4. The degradation of f_T at strong forward bias results from C_{gg} increasing faster than g_m, while the decrease in f_T at negative V_{GS}, is due to the rapid decrease in g_m, which cannot be offset by the lower gate capacitance.

Table I. Extracted intrinsic transconductance, g_m, and total gate capacitance, C_{gg}, from s-parameters at $V_{DS} = +3$ V.

V_{GS} (V)	g_m (mS)	C_{gg} (fF)
+1.0	1.60	169
+0.5	1.31	124
0.0	0.94	105
–0.5	0.44	85.0
–1.0	0.11	47.9
–1.5	0.038	34.1

Both f_T and f_{max} increase with increasing V_{DS} which is likely due to the higher electron velocity under larger electric field. f_T and f_{max} generally increase with increasing V_{GS}, except at more positive values, where the increased gate capacitance causes f_T and f_{max} to decrease. At $V_{DS} = +3$ V, the device shows maximum f_T of 1.31 GHz (0.97 GHz) at $V_{GS} = +0.5$ V, while the maximum f_{max} of 3.25 GHz occurs at $V_{GS} = 0$ V. The lower V_{GS} value for the peak f_{max} compared to f_T can be attribute to the V_{GS} dependence of g_o and is consistent with the increased g_m/g_o ratio of 19 at $V_{GS} = 0$ V compared to $g_m/g_0 = 17$ at $V_{GS} = +0.5$ V (taken from first DC measurement). Similarly, f_{max} also shows a V_{DS} dependence that is stronger than f_T, a trend that can be linked to the improved g_m/g_o ratio at higher V_{DS}.

While these results far exceed the best reported values for perovskites FETs in the literature, they still are lower than state-of-the-art β-Ga_2O_3 [20],[21] and GaN [22] FETs. However, several design improvements are possible. These include reducing the gate length, utilizing a T-gate structure to minimize gate resistance, and improving the recessed gate design to improve robustness to degradation. This later point will enable operation at high values of V_{DS}, which is limited in our current device design.

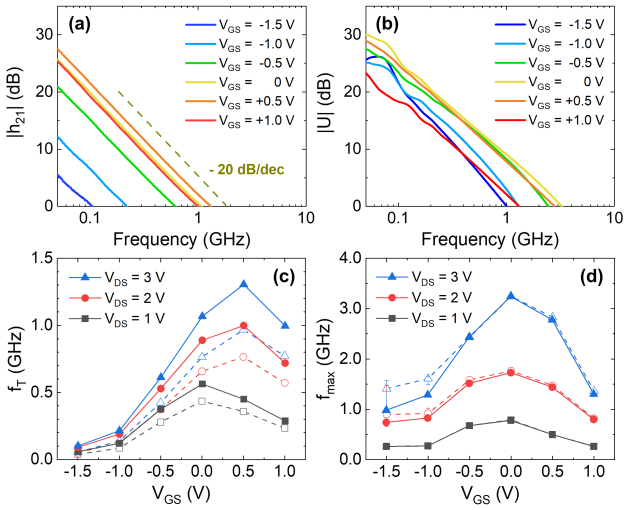

FIG 4. (a)-(b) Deembedded (a) short circuit current gain and (b) Mason's unilateral power gain vs. frequency at $V_{DS} = +3$ V and various V_{GS}. (c)-(d) Extracted (c) cut-off frequency and (d) maximum oscillation frequency vs. V_{GS} at various V_{DS} values before (dashed line) and after (solid line) deembedding.

IV. CONCLUSION

In conclusion, we have performed RF measurements on high-mobility SSO MESFET demonstrating GHz performance. Devices with 0.5-µm gate length achieve f_T of 1.31 GHz and f_{max} of 3.25 GHz after de-embedding. This work provides insight into the potential of high-mobility perovskites for use in RF applications. Several design improvements should be possible to push the performance to even higher frequencies. In the future, the high-frequency ability can be integrated with other attractive properties of SSO such as its optical transparency and integration capability with ferroelectrics to realize novel high-speed device applications.

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