A Differential Digital 4-Way Doherty Power Amplifier with 48% Peak Drain Efficiency for Low Power Applications

Jay Sheth and Steven M. Bowers
University of Virginia, Charlottesville, VA, USA
js4hb@virginia.edu

***Abstract*— This paper presents a differential digital 4-way Doherty power amplifier (PA) for low-power applications that achieves high efficiency in deep power back-off (PBO) without supply switching. The PA uses compact input and output matching networks through consolidation of various elements. A proof-of-concept PA was implemented in a 65 nm general purpose CMOS process, and it achieves a peak output stage drain efficiency (DE) of 48% at 4.75 GHz with 7.3 dBm output power (P_{out}). Also, it achieves peak PBO enhancements at 5.25 GHz with a DE of 42% at 0 dB PBO and 20% at 12.8 dB PBO. This corresponds to 2.2× improvement compared to normalized class B PA. The PA achieves an error vector magnitude (EVM) of -20 dB for a 1 Msym/s 16 QAM baseband signal with an average P_{out} of 2.9 dBm and DE of 34% at 5.25 GHz.**

***Keywords*— Differential power amplifier, CMOS, digital Doherty, compact matching network, EVM, IoT, low-power.**

I. Introduction

The need for high-efficiency transmitters for low-power applications (< 10 dBm) is growing due to advancements in the internet of things (IoT) ad-hoc sensor networks used in areas such as agriculture monitoring, inventory tracking, and smart home connectivity. In such low-power networks, the distance between two nodes can vary by an order of magnitude, necessitating efficient power amplifiers (PAs) with large (∼10 dB) output power back-off (PBO). Currently, state-of-the-art low-power transmitters (TX) use digital PAs, as this facilitates the integration of the PAs in the transmitters by allowing these PAs to be driven directly by an oscillator with a constant envelope signal, while the amplitude is controlled through digital words. Typically, these PAs employ advanced topologies such as class D [1] and class E/F_2 [2] to obtain high efficiencies, but their performance deteriorates in PBO. Limited work has been done in scaling traditional efficiency enhancement techniques such as Doherty PAs to low-power applications, but it offers low efficiency enhancements in deep PBO [3]. Although techniques such as digital class G Doherty [4] and multilevel outphasing [5] have been demonstrated in the literature for high power applications (> 25 dBm) to offer enhanced efficiencies in deep PBO, they rely on switching the V_{DD} to a lower value to maintain high efficiency. V_{DD} switching is challenging to implement in low-power regimes where the PAs operate at < 1 V (typically ∼0.5 V) to generate low output power efficiently. Scaling V_{DD} down further in back-off deteriorates the amplifier's transconductance severely.

Nested Doherty PAs have been shown in the literature [6] to offer improved efficiency in deep power back-off. In this paper, we propose a 4-way Doherty power amplifier (Fig. 1(a)) that can theoretically maintain optimal output matching for enhanced efficiency up to 9 dB PBO as shown in Fig. 1(b). The PA is implemented for low power applications, where it outputs 7.3 dBm and 6.5 dBm at 4.75 GHz and 5.25 GHz with 48% and 42% output stage drain efficiency (DE), respectively. It also achieves a 2.2× improvement compared to normalized class B PA at 12.8 dB PBO at 5.25 GHz. For ease of integration in the TX, the amplitude control of the PA has been implemented digitally, called digital 4-way Doherty power amplifier (D4DPA). This makes it a well suited candidate for IoT applications requiring digital PAs with low output power with high efficiency in power back-off.

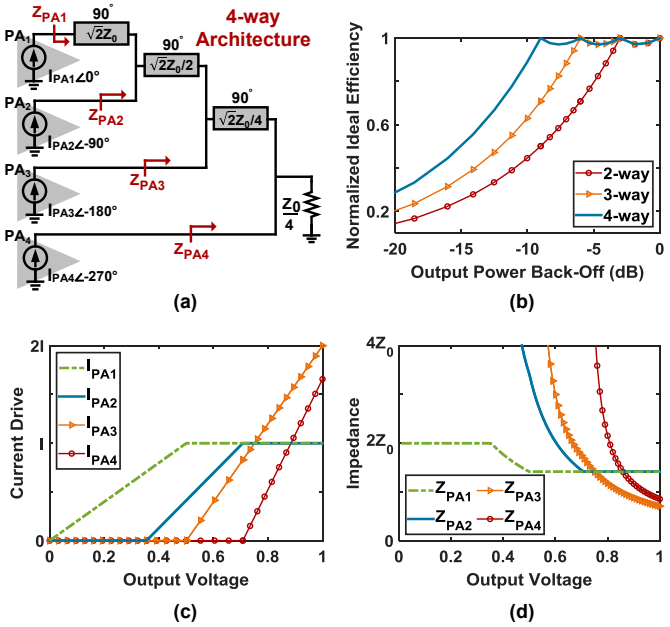

Fig. 1. (a) Proposed 4-way Doherty power amplifier (PA) architecture to maintain optimal matching through 9 dB power back-off (PBO), yielding (b) efficiency enhancements by (c) scaling RF current drives to (d) produce the desired optimal output impedances.

II. Design

Loading the PA with an optimal impedance is necessary to achieve maximum voltage swing and thus maximum efficiency. For a class B PA, the voltage swing reduces in PBO, leading to significant efficiency degradation. The traditional Doherty PA overcomes this challenge through load impedance manipulation by using a main and a peaking amplifier along with an impedance inverter. The two amplifiers work collectively to present the optimal impedances at the maximum

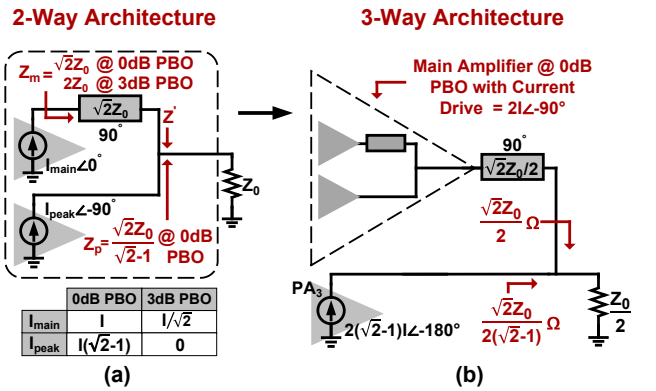

Fig. 2. Modified 2-way Doherty PA that enhances efficiency through 3 dB PBO, which extends to (b) a 3-way architecture to achieve efficiency enhancements at 3 dB and 6 dB PBO.

output power level. At 6 dB PBO, the peaking amplifier turns off and the impedance seen by the main amplifier doubles due to the impedance inverter, thus maximizing the voltage swing and leading to efficiency enhancement.

The proposed D4DPA overcomes efficiency degradation in deep PBO through four amplifiers and three impedance inverters, leading to efficiency enhancement in 3 dB increments. The design of the D4DPA can be explained through its simplified 2-way architecture. As mentioned in Fig. 2(a), through the use of asymmetric currents for the main and peaking amplifiers along with the impedance inverter network, the design can be manipulated to present optimal impedances at 0 dB and 3 dB PBO. This results in achieving two efficiency enhancement peaks, as shown in Fig. 1(b).

This concept can be extended to a 3-way architecture, where PA_1 and PA_2 can be combined and considered as the main PA with current drive $2I\angle$-90° at 0 dB PBO, and the current drive of PA_3 can be designed to obtain optimal impedances, as presented in Fig. 2(b). From 3 dB PBO onward, PA_3 turns off, leading to the same design as that of a 2-way architecture. Overall, the 3-way architecture obtains 3 efficiency peaks as illustrated in Fig. 1(b).

In this work, a 4-way architecture is implemented, as presented in Fig. 1(a), where $Z_0/4$ corresponds to 50 Ω and each amplifier is biased individually to generate the RF current drives, as shown in Fig. 1(c). These values for the current drives are obtained by extension from the 3-way architecture. The impedance seen by the amplifiers during back-off, shown in Fig. 1(d), leads to 4 efficiency enhancement peaks as depicted in Fig. 1(b).

III. Implementation

A proof-of-concept PA was implemented in a general purpose 65 nm CMOS process. The matching network's capability of presenting the expected impedances to the transistors, as described in Section II, is critical to achieve high efficiency, especially in deep PBO. To ensure that the matching network does not de-tune due to parasitic inductance from the wire-bonds, a differential topology for the PA is chosen, as it provides a virtual short on-chip for the fundamental frequency rather than solely relying on bypass capacitors.

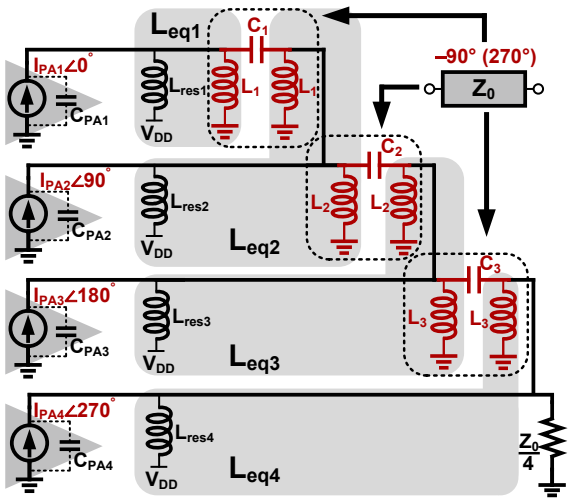

Fig. 3. Implementation of a 4-way Doherty output impedance matching network with consolidated on-chip lumped elements for transmission lines.

The transmission lines in the output matching network are implemented using a high-pass equivalent LC network with ∠-90° (∠270°) delay, thus the input phase for each PA block is updated accordingly. For simplicity of explanation, a single-ended architecture is depicted in Fig. 3. These LC networks, along with the inductors to resonate the drain capacitance and provide biasing, lead to an output match with a total of 10 inductors. Further, since the PA is designed for low-power applications, sizes of the transistors are small, requiring large inductance values (> 10 nH) that are challenging to implement. The use of high-pass LC network helps in consolidating these elements, as shown in Fig. 3. This not only reduces the total number of inductors down to 4, thereby reducing the area of the chip, but also makes them feasible to be generated on-chip [7].

The quadrature signals at the input of the PA are generated using a differential quadrature hybrid, as illustrated in Fig. 4. This structure is followed by a set of differential NOT gates that behave as RF buffers to drive the PA. An LC network is used at the input of these buffers to provide the gate biasing and match the circuit to 50 Ω. The matching network is consolidated with the differential quadrature hybrid structure to reduce the inductors from 6 to 4, while retaining the ability to provide the gate bias.

The overall block diagram of the implemented D4DPA is shown in Fig. 4. Each PA block is comprised of 4-bit binary weighted unit cells with common source (CS) output stages driven by digital pre-amplifiers, where the CS stages are sized to provide the RF currents as depicted in Fig. 1(c). The NOT and NAND digital pre-amplifiers successively drive larger gate capacitances to minimize power dissipation. When all the digital inputs to a PA block are set low, a 4 input OR gate automatically disables the whole PA block to further lower dynamic power dissipation. The baseband digital amplitude control for the PA is implemented through a NAND gate.

To improve the efficiency of the PA, the gate of the output CS stage needs to be biased around its threshold

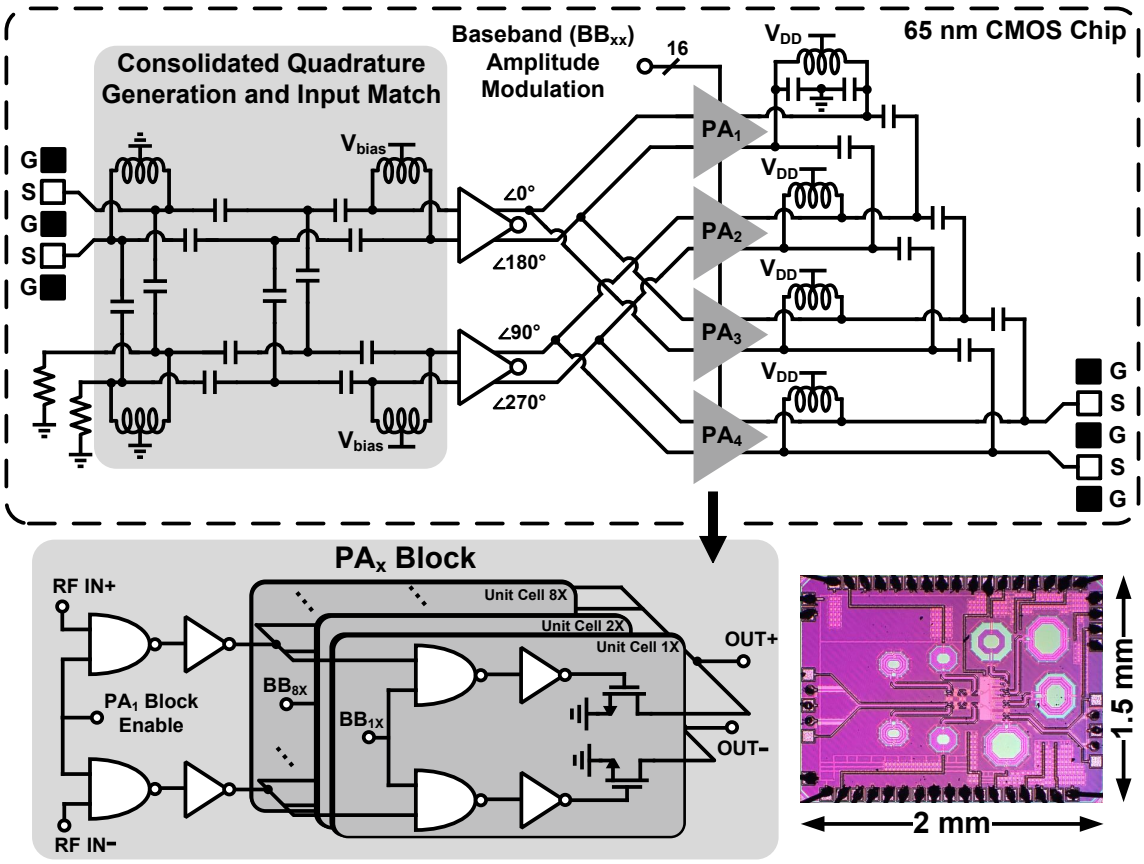

Fig. 4. Overall block diagram, block-level schematic, and die photo of the implemented differential digital 4-way Doherty power amplifier with consolidated output and input matching network and on-chip quadrature signal generation.

voltage. Since inserting an individual gate biasing circuit for each of the CS stages would result in a large number of passives that make it impractical, the biasing is provided through the driver NOT gate by sizing the nmos and pmos devices accordingly. Reliability of this biasing scheme can be enhanced by modifying V_{bias}, which changes the duty factor of the switching RF signal, thereby changing the gate bias of the output CS stage. The NOT driver also presents a low impedance at its output during its operation, which mitigates the stability concern of the CS stage. Fig. 4 shows the die photo of the implemented PA.

IV. Measurements

A. CW Measurements

The drain of the output CS stage is biased at 0.55 V to deliver low output power efficiently. A constant envelope differential signal is provided to the chip, and a pattern generator controls the digital states to vary the output power. The PA achieves a peak DE of 48% and system efficiency (SE) of 31% with a gain of 14 dB and output power (P_{out}) of 7.3 dBm at 4.75 GHz. Here, SE accounts for the power dissipated in the output CS stage and all the driver stages. Fig. 5 shows the performance of the PA in back-off for various digital states and compares it to normalized class B and class A PAs. Also, as Fig. 5 depicts, the PA achieves peak back-off enhancements

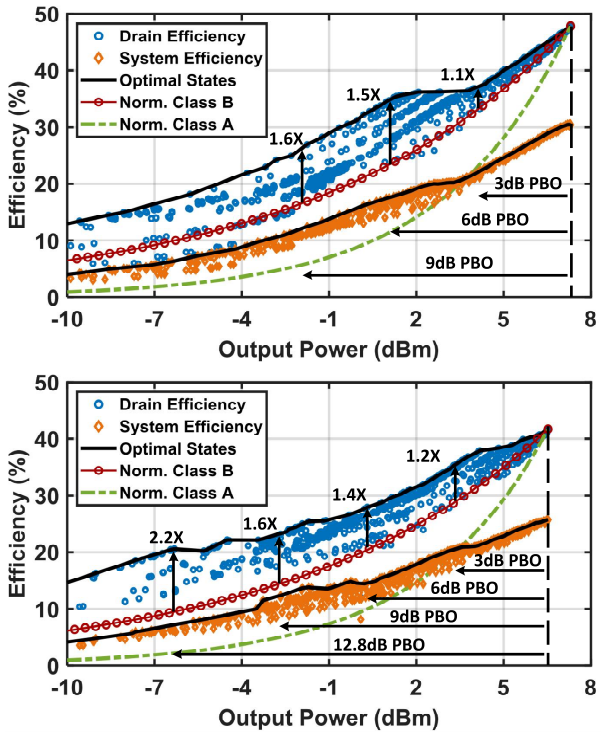

Fig. 5. Measured output stage drain efficiency (DE) and system efficiency (SE) of the implemented PA at 4.75 GHz (top) and 5.25 GHz (bottom) compared to normalized class B and class A PAs.

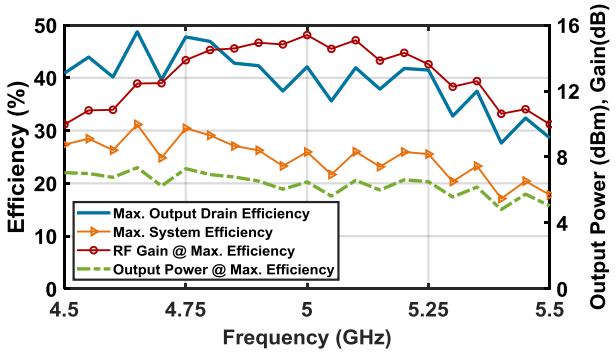

Fig. 6. Measured frequency dependence of the implemented PA for DE, SE, gain, and output power (P_{out}) at peak DE.

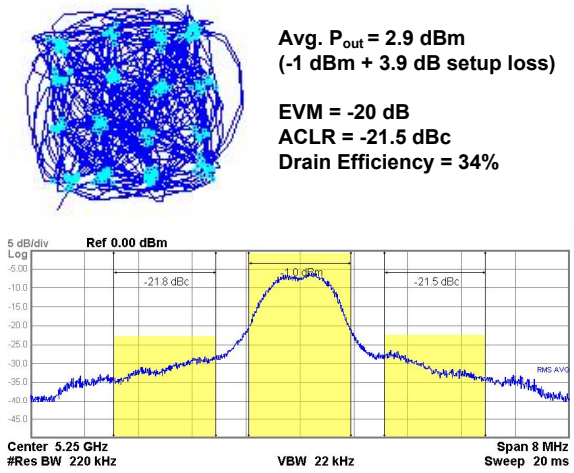

Fig. 7. Measured error vector magnitude (EVM), and adjacent channel leakage ratio (ACLR) for a 1 MSym/s 16 QAM waveform at 5.25 GHz.

at 5.25 GHz with a DE of 42% at 0 dB and 20% at 12.8 dB PBO, respectively. This corresponds to 2.2× improvement over normalized class B PA.

The frequency dependence of the PA's DE, SE, gain, and P_{out} are measured at the peak DE setting, as presented in Fig. 6. The input power at each frequency is set to maximize efficiency while maintaining gain above 10 dB. The peak gain is 15 dB at 5 GHz with P_{out} of 6.5 dBm. Even as the gain lowers due to change in input power, the output power stays relatively constant (±1 dB) from 4.75 GHz to 5.35 GHz.

B. RF Modulation Measurements

A 1 MSym/s phase shift keyed signal is provided to the chip and is synchronized with a pattern generator through a trigger signal to generate a 16 QAM 1 MSym/s RF modulated signal. As shown in Fig. 7, the PA achieves an average P_{out} of 2.9 dBm and DE of 34% at 5.25 GHz with an error vector magnitude (EVM) of -20 dB and adjacent channel leakage ratio (ACLR) of -21.5 dBc without any linearization.

This work is compared with state-of-the-art high-power (HP) and low-power (LP) PAs in Table 1. The implemented PA operates at almost 2× frequency compared to [2] [3], and it achieves competitive peak DE, while performing better than state-of-the-art in DE PBO for all non-V_{DD} switching PAs.

V. Conclusion

A differential digital 4-way Doherty PA is presented for low-power applications. The PA achieves a peak DE of 48% and P_{out} of 7.3 dBm at 4.75 GHz, and it obtains high efficiency in deep PBO. To the best of the authors' knowledge, this is the first paper to demonstrate a digital PA with efficiency enhancement in deep PBO (> 6dB) for low power applications (sub 10 dBm).

Table 1. Comparison to CMOS PAs with PBO Efficiency Enhancement

	[4]	[8]	[3]	[2]	This Work	
Type	HP	HP	LP	LP	**LP**	
Topology	Doherty/ Class G	Out-phasing	2-way Doherty†	Class E/F$_2^{\dagger}$	**4-way Doherty**	
V_{DD} Switching	Yes	No	No	No	**No**	
CMOS node (nm)	65	40	28	28	**65**	
Freq. [GHz]	3.71	5.9	2.15	2.44	**4.75**	**5.25**
$P_{out,peak}$ [dBm]	26.7	22.2	-2*	3	**7.3**	**6.5**
Gain [dB]	16	n/a	n/a	n/a	**14**	**14**
Drain Efficiency [%]						
Peak DE (SE)	40.2 (n/a)	49.2 (34.9)	34* (23)*	48* (41)	**48 (31)**	**42 (26)**
3dB PBO	34*	36*	29*	35*	**37**	**36**
6dB PBO	37	25*	24*	n/a	**35**	**28**
9dB PBO	32*	18*	18*	19*,(a)	**27**	**23**
RF Modulated Measurements						
Avg. P_{out} [dBm]	20.8 16QAM	16.4 64QAM	-7.66 16QAM	3 GFSK	**2.9 16QAM**	
DE [%]	28.8	23.3	n/a	48*,(b)	**34**	
ACLR [dBc]	-21††	n/a	-30.1	n/a	**-21.5**	
EVM [dB]	-24††	-30**	-24.7	-31.4(c)	**-20**	

*Estimated from reported figure ††After AM-PM Linearization **After DPD †Integrated in TX (a)@8dB PBO (b)assumes 0dB PAPR (c)FSK error

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