

## *(Invited)* A Path Toward Vertical GaN Superjunction Devices

To cite this article: Dolar Khachariya *et al* 2020 *ECS Trans.* **98** 69

View the [article online](#) for updates and enhancements.

## A Path Toward Vertical GaN Superjunction Devices

Dolar Khachariya<sup>a</sup>, Dennis Syzmanski<sup>b</sup>, Pramod Reddy<sup>c</sup>, Erhard Kohn<sup>b</sup>, Zlatko Sitar<sup>b,c</sup>,  
Ramón Collazo<sup>b</sup>, and Spyridon Pavlidis<sup>a</sup>

<sup>a</sup> Department of Electrical and Computer Engineering, North Carolina State University,  
Raleigh, NC 27695-7914, USA

<sup>b</sup> Department of Materials Science and Engineering, North Carolina State University,  
Raleigh, NC 27695-7919, USA

<sup>c</sup> Adroit Materials, Inc., 2054 Kildaire Farm Rd., Cary, NC 27518, USA

GaN devices offer exciting competition to incumbent technologies to meet the growing demand for high power electronic devices. The wide bandgap of GaN makes it possible to achieve higher breakdown voltages and reduced on-resistances compared to traditional Si in unipolar devices, as predicted by the classical Baliga figure of merit (BFOM). However, unipolar performance limits can be circumvented using the superjunction (SJ), which has been demonstrated experimentally in both Si and SiC. Due to the current difficulties with selective area doping in GaN, experimental reports of vertical GaN SJs are lacking. In response, we propose the use of the lateral polar junction (LPJ), which is unique to III-Nitrides, to create next-generation vertical GaN SJ devices. We develop a model that provides first order design equations for such a device, and validate it using TCAD simulations of a 1.2 kV diode. A proposed manufacturing approach for LPJ-based GaN SJ is provided.

### Introduction

Power semiconductor devices are widely used in our day-to-day life. They can be found in a broad range of products and systems, such as cell phones, computers, lamps, electric cars and trains, among others (1). The primary purpose of a power device, in all of its applications, is to block the applied voltage in the OFF state while having the lowest resistance in the ON state. Since the second half of the 20<sup>th</sup> century, Si has been heavily used in power devices due to its economic viability. However wide bandgap materials such as SiC and GaN (2), as well as ultrawide bandgap materials such as Ga<sub>2</sub>O<sub>3</sub>, diamond, and AlN (3), have recently gained much attention due to their wider bandgaps, higher breakdown field strength, and higher electron saturation velocities compared to Si.

The Baliga Figure of Merit (BFOM) offers a method to quantitatively evaluate the impact of a semiconductor material properties on a unipolar device's performance (2). It is defined as:

$$BFOM = \epsilon_s \cdot \mu_n \cdot E_C^3 \quad [1]$$

where,  $\epsilon_s$  is the semiconductor permittivity,  $\mu_n$  is electron mobility in the drift region, and  $E_C$  is the critical electric field of the material. The BFOM of GaN has been found to be

approximately 4000 times higher than Si and 6 times higher than SiC (4). This higher BFOM for GaN makes it possible to realize devices that have a smaller on-resistance and area, as well as efficiently operate at higher switching frequencies compared to Si for a given breakdown voltage rating. In practice, Si-based power device technology has already reached its unipolar theoretical limit, while SiC-based power devices are approaching their theoretical limit (5,6). In comparison, GaN-based power devices are showing consistent progress towards, but still far from, their theoretical limit (7-9).

The aforementioned theoretical limit for unipolar devices was considered unbreakable for about 30 years until the demonstration of Si-based RESURF (Reduced SURface Field) devices (10). In a RESURF device, the surface electric field was reduced by creating a 2-dimensional (2D) profile for the electric field, which increased the breakdown voltage (BV) capability of the device. Subsequent theoretical and experimental reports on this new device concept were published in which the device was alternatively referred to as a super-junction (SJ) (11), CoolMOS (12), MDmesh (13), and charge-coupled or charge-balanced device. The main difference compared to conventional power devices, is that the drift region of this new device is realized using either horizontally aligned or vertically stacked alternating p-type and n-type doped columns/pillars, which helps to create a 2D electric field by balancing the charges inside the drift region. The fabrication process flow for SJ devices is not trivial as it requires selective area doping to obtain horizontally or vertically aligned p-type and n-type columns. This is particularly challenging to realize in vertical channel devices with thick drift regions. The two main techniques to achieve a SJ are multiepitaxy with ion-implantation and trench etching with regrowth (14,15). The maturity of Si technology has enabled commercialization of Si-based SJ devices, and numerous publications in the literature are available (15). In recent years, experimental demonstrations of SiC-based SJ devices have also been reported in the literature (16-18). In both Si and SiC, SJ devices have outperformed their conventional counterparts, thus increasing competition among technologies.

A vertical GaN SJ device capable of competing with Si and SiC SJ devices has yet to be reported since lateral regrowth and ion implantation technologies remain challenging. However, the polar nature of GaN presents a unique opportunity to create superjunctions differently. Currently several experimental demonstrations of lateral GaN Polarization Superjunction (PSJ) devices have been reported in the literature (19-23). In these devices, the charge balance is achieved via the engineering of positive (2DHG – 2D Hole Gas) and negative polarization charges (2DEG – 2D Electron Gas) at the interfaces of GaN/AlGaN/GaN. Despite claiming the advantages of the SJ structure, the current performance of these GaN PSJ does not exceed the 1D GaN unipolar theoretical limit. It is essential to show an actual performance improvement in SJ devices by crossing GaN's unipolar theoretical limit. Moreover, there is a need to demonstrate an approach for vertical GaN SJ devices that can compete with vertical Si and SiC technology at high voltages.

This paper presents a novel approach via lateral polar junctions (LPJ) to realize vertical GaN-based SJ devices. The LPJ leverages the differences in defect incorporation in Ga-polar and N-polar GaN during growth to concurrently create lateral p- and n-doped regions during epitaxial growth (24,25), thus bypassing the current technical challenges of ion implantation and etching/regrowth in III-nitrides. In what follows, an analytical model to design vertical GaN SJ device parameters for a given breakdown voltage is presented and

subsequently validated using TCAD simulations of GaN SJ diode. A proposed route to manufacturing these devices is then summarized.

### Design Space of Vertical GaN Superjunction

The optimum performance of a SJ device depends on a variety of device parameters such as p/n column width, thickness, and doping, all of which can be calculated before device fabrication. Many efforts were taken to develop analytical models for Si (11,26), and SiC (27) SJ devices. Similar efforts are ongoing to develop a model for III-Nitride-based SJ devices (28-35). Amongst those reports, only a few present a model for the GaN SJ, and those models are based on complicated infinite series to solve the electric field, which require substantial computation and time. In comparison, a simplified and more intuitive approach to derive equations for modeling various parameters for Si-based SJ devices has been shown by Baliga (36). In this work, we have applied this framework to GaN in order to guide the design of novel devices and provide a reference for experimental results.

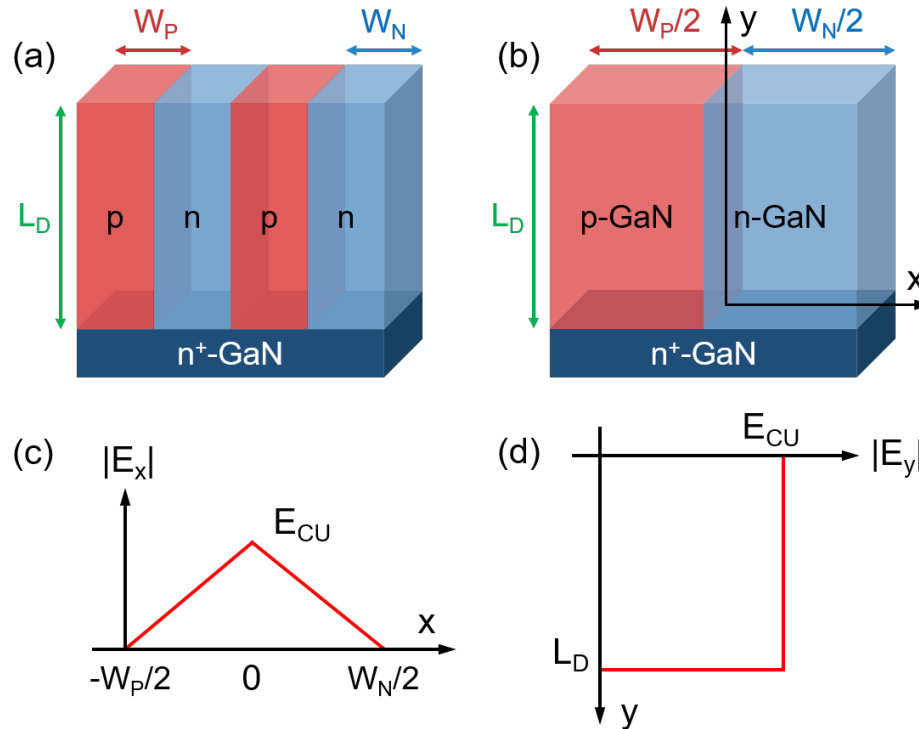


Figure 1. Cross-sectional view of (a) a GaN SJ diode with vertically stacked alternating p and n columns and (b) the unit cell GaN SJ diode structure. The electric field distribution (c) in the x-direction obtained at the middle of the drift region ( $y=L_D/2$ ) and (d) in the y-direction obtained at the ( $x=W_N/2=-W_P/2$ ) at breakdown.

Figure 1(a) shows the unit cell cross-section of the GaN SJ device with a half-width of p and n columns. The lateral depletion region forms between the p and n columns when a reverse bias is applied to the structure, which creates an electric field in the x-direction, as shown in Figure 1(b). By increasing the reverse bias voltage, the depletion in the lateral

direction increases and, with it, the electric field. To achieve better charge coupling, both columns should be totally depleted before the applied reverse bias reaches the breakdown voltage. Thus, when the reverse bias reaches the breakdown voltage, the electric field in the y-direction of the structure will be uniform, defined as the uniform critical electric field ( $E_{CU}$ ) in p and n columns, as shown in Figure 1(c).

As the electric field increases, free carriers are accelerated, which in turn, creates more free carriers through impact events in the depletion region of the drift layer. The number of free carriers increases exponentially with increasing reverse bias, and avalanche breakdown occurs when carrier multiplication reaches infinity, i.e., the impact ionization integral reaches unity (1). The most straightforward form of the impact ionization integral equation can be given as follows:

$$\int_0^{L_D} \alpha_{eff} dy = 1 \quad [2]$$

where,  $\alpha_{eff}$  is the effective value of the electron and hole ionization coefficient and  $L_D$  is the thickness of the vertical p/n columns. Several efforts have been taken to develop impact ionization coefficients for GaN material based on theoretical and experimental work (37,38). In this work,  $\alpha_{eff} = 1.5 \times 10^{-42} \cdot E^7$  is used for calculations as the parameters reported by Baliga (38) are based on experimental results. By replacing the value of  $\alpha_{eff}$  in Eq. [2] and solving it, the relation between breakdown voltage (BV), uniform electric field ( $E_{CU}$ ), and drift region thickness ( $L_D$ ) for GaN SJ devices is obtained:

$$BV = E_{CU} \cdot L_D = 9.44 \times 10^5 \cdot L_D^{6/7} \quad [V] \quad [3]$$

Hence, the thickness of the vertical p/n columns of GaN SJ for the required BV can be calculated using:

$$L_D = 1.07 \times 10^{-7} \cdot BV^{7/6} \quad [cm] \quad [4]$$

The optimum dose for the charge-balanced SJ device can be found by considering the peak value of the electric field, in Figure 1(c), which is  $E_{CU}$ . It is expressed as:

$$Q_{optimum} = qN_D \frac{W_N}{2} = \epsilon_S E_{CU} = qN_A \frac{W_P}{2} \quad [5]$$

where,  $Q_{optimum}$  is the required dose to create a charge balance within the p/n columns,  $\epsilon_S (=10.4\epsilon_0)$  is the permittivity of GaN,  $W_N$  and  $W_P$  are the width of the n and p columns, respectively;  $N_D$  and  $N_A$  are the doping concentrations of the n and p columns, respectively. Using Eqs. [3] and [5], the relationship between the dose and the BV for GaN SJ can be obtained as:

$$N_D \cdot W_N = N_A \cdot W_P = 1.08 \times 10^{14} \cdot BV^{-1/6} \quad [cm^{-2}] \quad [6]$$

Using Eqs. [4] and [6], one can find GaN SJ device parameters for a given BV or vice versa. Also, from Eq. [6], it should be noted that the smaller the p and n column width the higher the doping concentration in the drift region columns. This will allow to have lower on-resistance in the SJ compared to conventional power devices. Figures 2(a) and 2(b)

show the required drift region thickness and the optimum dose for GaN SJ devices at a given BV range until 10 kV. Using the optimum dose graph shown in Figure 2(b), a required doping can be calculated by choosing achievable column widths for a given BV. For comparison, the design parameters for conventional GaN power devices can be written in similar ways and are given as (2):

$$W_{PP} = 1.7 \times 10^{-7} \cdot BV^{7/6} \quad [\text{cm}] \quad [7]$$

and,

$$N_D \cdot W_{PP} = 6.77 \times 10^{13} \cdot BV^{-1/6} \quad [\text{cm}^{-2}] \quad [8]$$

where,  $W_{PP}$  is the homogeneous drift region thickness for parallel plane breakdown case. Thus, from Eqs. [4], [6], [7] and [8], it is clear that the SJ devices can have a smaller drift region thickness and higher doping compared to the conventional devices for a given BV.

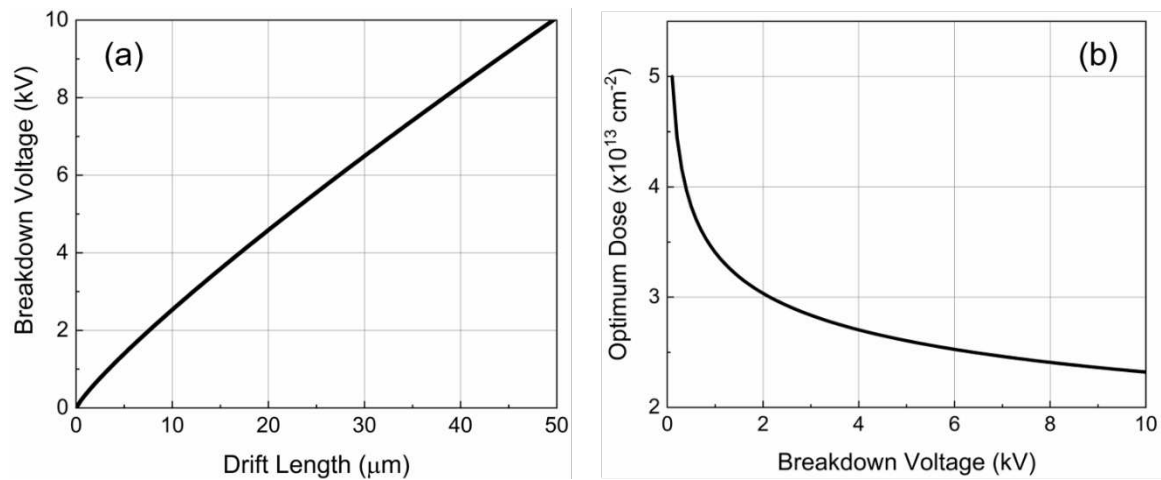


Figure 2. (a) Breakdown voltage versus required drift region thickness, (b) required optimum dose for the two-dimensional charge coupling.

As SJ devices can have larger drift region doping, a lower on-resistance can be obtained compared to equivalent conventional devices. The ideal specific on-resistance for the structure, shown in Figure 1(a), considering unipolar current flow, i.e., only through n column, can be given as (36):

$$R_{on,sp-ideal} = \frac{L_D}{q\mu_n N_D} \cdot \frac{W_N + W_P}{W_N} \quad [9]$$

By replacing the values of  $L_D$  and  $N_D$  ( $=N_A$ ) with respect to BV, the ideal specific on-resistance can be represented in terms of the BV. Thus, the ideal specific on-resistance for GaN SJ devices can be given as:

$$R_{on,sp-ideal} = \frac{1.144 \times 10^{-14} \cdot BV^{4/3} \cdot W_N}{\epsilon_S \mu_n} \quad [\Omega \cdot \text{cm}^2] \quad [10]$$

A similar relationship of on-resistance with respect to BV for the conventional power devices has been derived (2). The mobility ( $\mu_n$ ) for GaN as a function of doping in Eq. [10] is used from (2). Using these equations, the on-resistance versus breakdown voltage characteristics for GaN conventional (1D limit) and SJ devices with different column widths (for  $W_N = W_P$ ) are shown in Figure 3. It is seen that the SJ structure offers very small on-resistance compared to conventional devices designed for the same BV capability. Additionally, the use of smaller column widths further reduces the on-resistance of the SJ devices.

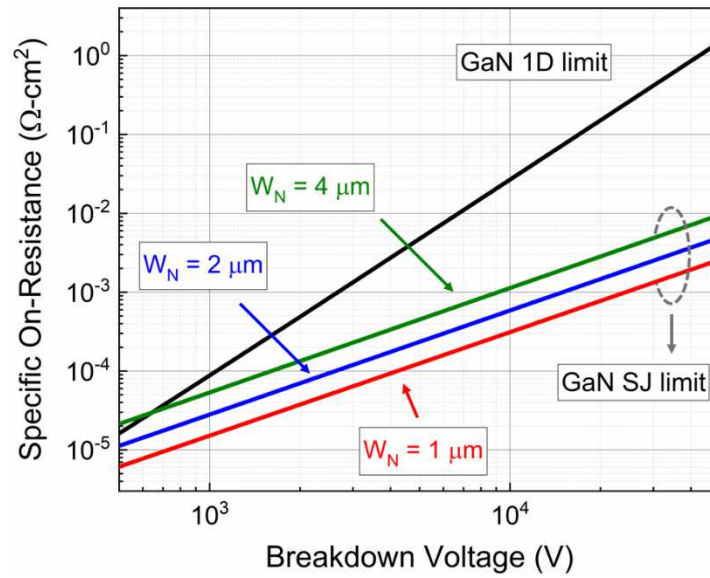


Figure 3. Theoretical limit of the specific on-resistance versus breakdown voltage comparison for GaN SJ devices.

### TCAD Simulations of a GaN Superjunction Diode

TCAD simulations are performed using Silvaco ATLAS to evaluate the accuracy of the developed model for GaN SJ. A 1200 V breakdown voltage GaN SJ diode is designed and simulated to validate the designed equations in previous section. The cross-section of the simulated structure is shown in the Figure 4(a). It should be noted that the structure has an additional  $p^+$ -GaN layer on top in comparison to the structure shown in Figure 1(b). This is used to facilitate modeling of the reverse blocking performance of the SJ diode. The required parameters to simulate the structures are: thickness of the drift region ( $L_D$ ), and half width and doping concentrations of the p/n columns, all of which can be calculated using the above designed model.

According to Eq. [4] the required drift region thickness ( $L_D$ ) to achieve 1200 V breakdown is 4.2  $\mu\text{m}$ . Similarly, using Eq. [6], the required dose ( $N_D \cdot W_N = N_A \cdot W_P$ ) in p/n column is  $3.3 \times 10^{13} \text{ cm}^{-2}$ . Choosing  $W_N = W_P = 1 \mu\text{m}$ , as it is easily manufacturable with the i-line stepper lithography, the required p/n column doping ( $N_A = N_D$ ) is calculated from dose and it is  $3.3 \times 10^{17} \text{ cm}^{-3}$ . The corresponding simulation results show a breakdown voltage around 1180 V, as shown in Figure 4(b), which is in good agreement with the developed model. Figure 4(c) shows the 2-D electric field contour at the 1180 V

breakdown. The 3-D electric field contour is also plotted and shown in Figure 4(d). From these figures, it can be observed that the electric field is uniform across the drift region with a slightly higher E-field near the lateral junction of p and n columns, at the bottom of p, and the top of n column. In comparison, a conventional device with the same drift region doping would have a breakdown voltage around 200 V. Hence, it is seen that the SJ devices clearly offer a performance advantage over their conventional unipolar counterparts.

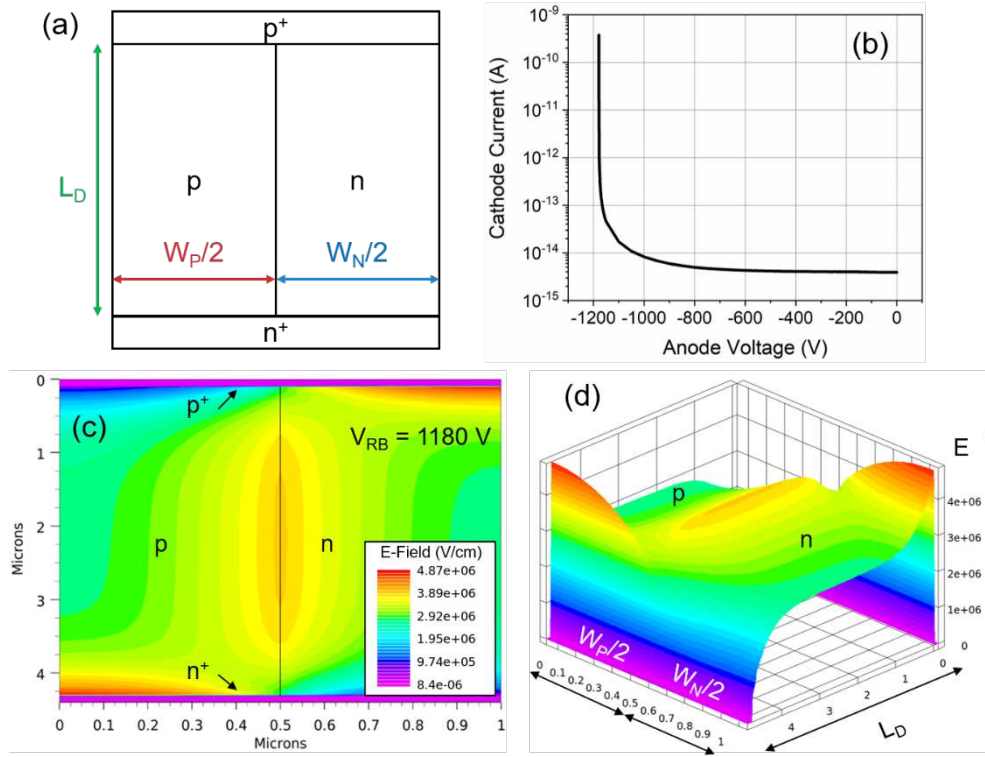


Figure 4. Simulated (a) cross-section structure and (b) blocking I-V characteristics of the 1200 V GaN SJ diode. (c) Two-dimensional and (d) three-dimensional electric field distribution in the device at reverse bias 1180 V.

These results demonstrate that the first order device design parameters for a GaN SJ diode can be calculated using the model designed in this work. It should be noted that these models are not valid in the presence of the charge imbalance (i.e. when  $N_D \cdot W_N \neq N_A \cdot W_P$ ).

### Realization of Vertical GaN Superjunction: A Path Forward

As mentioned in the introduction, there are two main techniques to obtain SJ structures, namely trench etching/regrowth and ion implantation, and they have already been demonstrated to be effective in both Si and SiC technologies. Despite several ongoing efforts to develop similar methods for selective area doping in GaN, these approaches have not been successfully applied to GaN to realize vertical SJ devices. The major issue in etching/regrowth technique is the etching damage to the GaN which leads to the interface charges after the regrowth and thus higher reverse bias leakage (39-42). Whereas in ion implantation, large Mg drive-in (43,44) has been observed, which would restrict the benefit of having smaller p/n column width and limit the reduction in on-resistance. Therefore,



instead of these conventional methods, we propose a novel lateral polar junction approach to realize vertical GaN SJ devices. This approach is only available in III-Nitride technology, and provides a promising path towards selective area doping of thick and narrow p/n columns necessary in high-performance vertical GaN SJ devices.

GaN films can be grown in two different orientations, Ga-polar (0001) and N-polar (000 $\bar{1}$ ). Crystal polarity during GaN epitaxy on sapphire substrates is determined by a low-temperature (LT) AlN buffer layer, the presence of which results in Ga-polar epitaxial films (45,46). Therefore, patterning of the LT AlN buffer via lithography, allows for Ga- and N-polar GaN domains to be grown simultaneously and laterally via metal-organic chemical vapor deposition (MOCVD) (47). This method avoids the trench etching/regrowth and ion implantation techniques conventionally used to realize SJ. Moreover, thick p/n columns can be grown in a single run, which avoids the issue of aligning p/n columns normally seen in multiepitaxy technique. The process steps are illustrated in Figure 5.

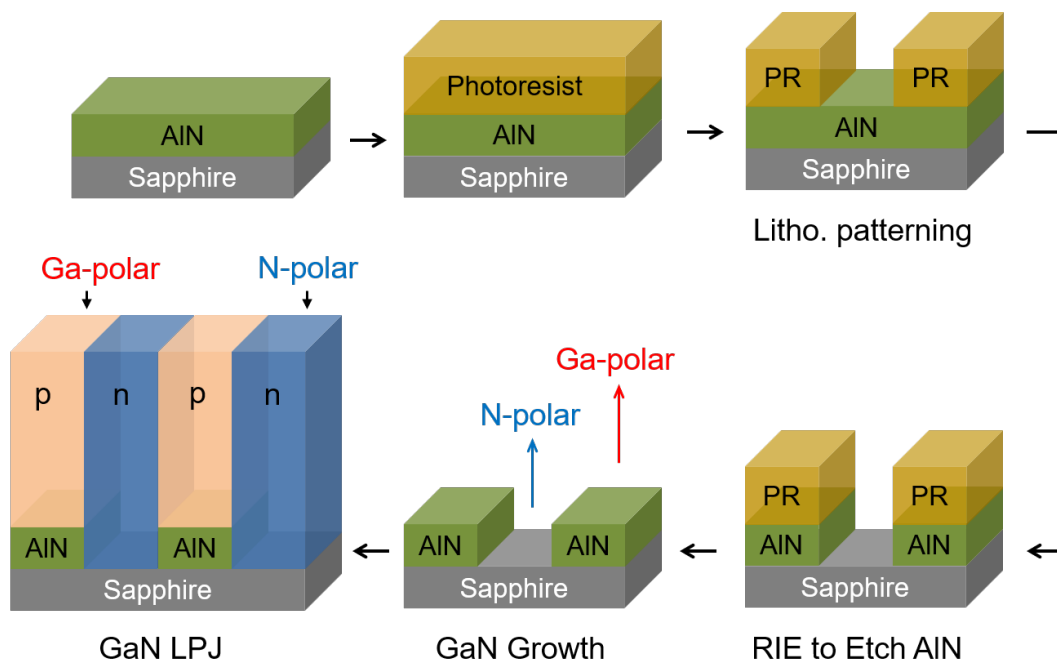


Figure 5. Process flow for fabricating GaN SJ structure using later polar junction (LPJ) approach.

The phenomenon that allows for the superjunction is the asymmetry in defect incorporation. Specifically, preferential incorporation of shallow donor oxygen occurs in N-polar GaN making it n-type while Ga-polar GaN remains semi-insulating (24,25,48-50). In contrast Mg incorporates similarly into GaN for both polarities. Hence, if Mg is introduced in at concentrations below O concentration in N-polar GaN, the Ga-polar domains will become p-type, while the N-polar domains will remain n-type (24,25). Further, Hite *et al.* (51-53) have demonstrated that a thick GaN lateral polar structure exceeding 100  $\mu\text{m}$  can be grown on native GaN substrate thus allowing for fully vertical GaN SJ on GaN substrates. Fully vertical GaN SJ devices with alternating p-type and n-type columns can hence be realized using this LPJ approach.

## Conclusion

The use of a superjunction makes it possible for a material to surpass its unipolar performance limit. There is therefore a clear need for an approach to achieve high-performance GaN SJ devices. Instead of relying on conventional manufacturing approaches, this paper proposes the use of a lateral polar junction – a feature that is unique to III-Nitrides – to make next generation GaN SJ devices. A first-order analytical model to obtain device design parameters is established, and subsequently validated using the TCAD simulations of a 1200 V GaN SJ diode. It is confirmed that not only does the analytical model provide an accurate estimate of the drift layer requirements, but that the GaN SJ will indeed outperform a GaN unipolar device with equivalent drift region doping and thickness. Finally, an approach to manufacturing GaN LPJ-based power devices is outlined.

## Acknowledgments

The authors gratefully acknowledge funding in part from AFOSR (Nos. FA9550-17-1-0225 and FA9550-19-1-0114), NSF (Nos. ECCS-1916800, ECCS-1508854, ECCS-1610992, DMR-1508191, and ECCS-1653383), ARO (Nos. W911NF-15-2-0068, W911NF-16-C-0101, and W911NF-18-1-0415), and DOE (No. DE-SC0011883).

## References

1. B. J. Baliga, *Fundamentals of Power Semiconductor Devices* (Springer Science & Business Media, Boston, MA, 2008).
2. B. J. Baliga, *Gallium Nitride and Silicon Carbide Power Devices* (World Scientific Publishing Company, 2016).
3. J. Y. Tsao, S. Chowdhury, M. A. Hollis, D. Jena, N. M. Johnson, K. A. Jones, R. J. Kaplar, S. Rajan, C. G. Van de Walle, E. Bellotti, C. L. Chua, R. Collazo, M. E. Coltrin, J. A. Cooper, K. R. Evans, S. Graham, T. A. Grotjohn, E. R. Heller, M. Higashiwaki, M. S. Islam, P. W. Juodawlkis, M. A. Khan, A. D. Koehler, J. H. Leach, U. K. Mishra, R. J. Nemanich, R. C. N. Pilawa-Podgurski, J. B. Shealy, Z. Sitar, M. J. Tadjer, A. F. Witulski, M. Wraback, and J. A. Simmons, *Adv. Electron. Mater.*, **4**, 1600501 (2018).
4. A. M. Ozbek and B. J. Baliga, *IEEE Electron Device Lett.*, **32**, 300 (2011).
5. J. W. Palmour, in *2014 IEEE International Electron Devices Meeting* (2014), p. 1.1.1-1.1.8.
6. B. J. Baliga, in *2018 76th Device Research Conference (DRC)* (IEEE, Santa Barbara, CA, 2018), pp. 1–2.
7. E. A. Jones, F.F. Wang, and D. Costinett, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, **4**, 707 (2016).
8. H. Amano, Y. Baines, E. Beam, B. Matteo, T. Bouchet, R. C. Paul, M. Charles, J. C. Kevin, C. Nadim, C. Rongming, S. Carlo De, S. Maria Merlyne De, D. Stefaan, L. D. Cioccio, E. Bernd, E. Takashi, P. Fay, J. F. Joseph, L. Guido, H. Oliver, H. Geoff, H. Thomas, H. Dilini, H. Peter, H. Jie, H. Mengyuan, H. Qingyun, H. Alex, J. Sheng, H. Kawai, K. Dan, K. Martin, K. Ashwani, L. Kean Boon, L. Xu, M. Denis, M. Martin, R. McCarthy, M. Gaudenzio, M. Matteo, E. Morvan, A.

- Nakajima, E. M. S. Narayanan, O. Stephen, P. Tomás, P. Daniel, M. Plissonnier, R. Reddy, S. Min, T. Iain, A. Torres, T. Nicola, V. Unni, J. U. Michael, H. Marleen Van, J. W. David, J. Wang, J. Xie, S. Yagi, Y. Shu, C. Youtsey, Y. Ruiyang, Z. Enrico, Z. Stefan, and Z. Yuhao, *J. Phys. D Appl. Phys.*, **51**, 163001 (2018).
9. T. Ueda, *Jpn. J. Appl. Phys.*, **58**, SC0804 (2019).
  10. J. A. Appels and H. M. J. Vaes, in *1979 International Electron Devices Meeting* (1979), pp. 238–241.
  11. T. Fujihira, *Jpn. J. Appl. Phys.*, **36**, 6254 (1997).
  12. G. Deboy, N. Marz, J.-P. Stengl, H. Strack, J. Tihanyi, and H. Weber, in *1998 International Electron Devices Meeting*. (1998), pp. 683–685.
  13. M. Saggio, D. Fagone, and S. Musumeci, in *12th International Symposium on Power Semiconductor Devices ICs. (ISPSD)* (2000), pp. 65–68.
  14. T. Minato, T. Nitta, A. Uenisi, M. Yano, M. Harada, and S. Hine, in *12th International Symposium on Power Semiconductor Devices & ICs. (ISPSD)* (2000), pp. 73–76.
  15. F. Udrea, G. Deboy, and T. Fujihira, *IEEE Trans. Electron Devices*, **64**, 713 (2017).
  16. X. Zhong, B. Wang, J. Wang, and K. Sheng, *IEEE Trans. Electron Devices*, **65**, 1458 (2018).
  17. R. Kosugi, S. Ji, K. Mochizuki, K. Adachi, S. Segawa, Y. Kawada, Y. Yonezawa, and H. Okumura, in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)* (2019), pp. 39–42.
  18. H. Wang, C. Wang, B. Wang, N. Ren, and K. Sheng, *IEEE Electron Device Lett.*, **41**, 445 (2020).
  19. H. Ishida, D. Shibata, H. Matsuo, M. Yanagihara, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, in *2008 IEEE International Electron Devices Meeting* (2008), pp. 1–4.
  20. H. Ishida, D. Shibata, M. Yanagihara, Y. Uemoto, H. Matsuo, T. Ueda, T. Tanaka, and D. Ueda, *IEEE Electron Device Lett.*, **29**, 1087 (2008).
  21. A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. Narayanan, *IEEE Electron Device Lett.*, **32**, 542 (2011).
  22. V. Unni, H. Long, M. Sweet, A. Balachandran, E. M. S. Narayanan, A. Nakajima, and H. Kawai, in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)* (2014), pp. 245–248.
  23. H. Kawai, S. Yagi, S. Hirata, F. Nakamura, T. Saito, Y. Kamiyama, M. Yamamoto, H. Amano, V. Unni, and E. M. S. Narayanan, *Phys. Status Solidi (a)*, **214**, 1600834 (2017).
  24. R. Collazo, S. Mita, A. Rice, R. F. Dalmau, and Z. Sitar, *Appl. Phys. Lett.*, **91**, 212103 (2007).
  25. R. Collazo, S. Mita, A. Rice, R. Dalmau, P. Wellenius, J. Muth, and Z. Sitar, *Phys. Status Solidi (c)*, **5**, 1977 (2008).
  26. A. G. M. Strollo and E. Napoli, *IEEE Trans. Electron Devices*, **48**, 2161 (2001).
  27. L. Yu and K. Sheng, *IEEE Trans. Electron Devices*, **55**, 1961 (2008).
  28. A. Nakajima, K. Adachi, M. Shimizu, and H. Okumura, *Appl. Phys. Lett.*, **89**, 193501 (2006).
  29. Z. Li and T. P. Chow, *IEEE Trans. Electron Devices*, **60**, 3230 (2013).
  30. B. Song, M. Zhu, Z. Hu, K. Nomoto, D. Jena, and H. G. Xing, in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)* (2015), pp. 273–276.
  31. U. Vineet and E. M. S. Narayanan, *Jpn. J. Appl. Phys.*, **56**, 04CG02 (2017).

32. X. Zhou, J. R. Howell-Clark, Z. Guo, C.W. Hitchcock, and T. P. Chow, *Appl. Phys. Lett.*, **115**, 112104 (2019).
33. M. Xiao, R. Zhang, D. Dong, H. Wang, and Y. Zhang, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, **7**, 1475 (2019).
34. Y. Ma, M. Xiao, R. Zhang, H. Wang, and Y. Zhang, *IEEE J. Electron Devices Soc.*, **8**, 42 (2020).
35. H. Huang, J. Cheng, B. Yi, W. Zhang, and W.T. Ng, *Appl. Phys. Lett.*, **116**, 102103 (2020).
36. B. J. Baliga, *Advanced Power MOSFET Concepts* (Springer Science & Business Media, 2010).
37. Z. Li, V. Pala, and T. P. Chow, *Jpn. J. Appl. Phys.*, **52**, 08JN05 (2013).
38. B. J. Baliga, *Semicond. Sci. Technol.*, **28**, 074011 (2013).
39. Z. Hu, K. Nomoto, M. Qi, W. Li, M. Zhu, X. Gao, D. Jena, and H. G. Xing, *IEEE Electron Device Lett.*, **38**, 1071 (2017).
40. A. Aragon, M. Monavarian, I. Stricklin, G. Pickrell, M. Crawford, A. Allerman, A. M. Armstrong, and D. Feezell, *Phys. Status Solidi (a)*, **217**, 1900757 (2020).
41. G. W. Pickrell, A. M. Armstrong, A. A. Allerman, M. H. Crawford, K. C. Cross, C. E. Glaser, and V. M. Abate, *J. Electron. Mater.*, **48**, 3311 (2019).
42. K. Fu, H. Fu, X. Huang, H. Chen, T.-H. Yang, J. Montes, C. Yang, J. Zhou, and Y. Zhao, *IEEE Electron Device Lett.*, **40**, 1728 (2019).
43. H. Sakurai, M. Omori, S. Yamada, Y. Furukawa, H. Suzuki, T. Narita, K. Kataoka, M. Horita, M. Bockowski, J. Suda, and T. Kachi, *Appl. Phys. Lett.*, **115**, 142104 (2019).
44. H. Sakurai, T. Narita, M. Omori, S. Yamada, A. Koura, M. Iwinska, K. Kataoka, M. Horita, N. Ikarashi, M. Bockowski, J. Suda, and T. Kachi, *Appl. Phys. Express*, **13**, 086501 (2020).
45. R. Collazo, S. Mita, A. Aleksov, R. Schlessner, and Z. Sitar, *J. Cryst. Growth*, **287**, 586 (2006).
46. M. Stutzmann, O. Ambacher, M. Eickhoff, U. Karrer, A. L. Pimenta, R. Neuberger, J. Schallwig, R. Dimitrov, P. J. Schuck, and R. D. Grober, *Phys. Status Solidi (b)*, **228**, 505 (2001).
47. S. Mita, R. Collazo, and Z. Sitar, *J. Cryst. Growth*, **311**, 3044 (2009).
48. R. Kirste, R. Collazo, G. Callsen, M. R. Wagner, T. Kure, J. Sebastian Reparaz, S. Mita, J. Xie, A. Rice, J. Tweedie, Z. Sitar, and A. Hoffmann, *J. Appl. Phys.*, **110**, 093503 (2011).
49. P. Reddy, D. Khachariya, D. Szymanski, M.H. Breckenridge, B. Sarkar, S. Pavlidis, R. Collazo, Z. Sitar, and E. Kohn, *Semicond. Sci. Technol.*, **35**, 055007 (2020).
50. D. Khachariya, D. Szymanski, R. Sengupta, P. Reddy, E. Kohn, Z. Sitar, R. Collazo, and S. Pavlidis, *J. Appl. Phys.*, **128**, 064501 (2020).
51. J. K. Hite, N. D. Bassim, M. E. Twigg, M. A. Mastro, F. J. Kub, and C. R. Eddy, *J. Cryst. Growth*, **332**, 43 (2011).
52. J. Hite, M. Twigg, M. Mastro, J. Freitas, J. Meyer, I. Vurgaftman, S. O'Connor, N. Condon, F. Kub, S. Bowman, and C. Eddy, *Opt. Mater. Express*, **2**, 1203 (2012).
53. J. K. Hite, N. Y. Garces, R. Goswami, M. A. Mastro, F. J. Kub, and C. R. Eddy, *Appl. Phys. Express*, **7**, 025502 (2014).