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An Enhanced Direct Torque Control for A Three-Level T-Type Inverter

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Abstract – Direct torque control (DTC) is a widely used approach for motor drives due to its distinctive advantages, e.g., fast dynamic response and highly robust against motor parameters uncertainties and external disturbances. To achieve lower torque ripple, higher switching frequency is usually required, which however can reduce the drive efficiency. Using the emerging silicon carbide (SiC) devices, which can operate efficiently at much higher switching frequency than their silicon counterparts, thus it could be feasible to achieve high efficiency and low torque ripple simultaneously. In this work, a novel multi-level DTC for a SiC T-type inverter is proposed to significantly reduce the torque and flux ripples, while retaining the fast-dynamic response. The unbalanced dc-link is a common issue of the T-type inverter, which may also lead to higher torque ripple. To address this issue, the proposed DTC algorithm only uses the real voltage space vectors and virtual space vectors (VSVs) that do not contribute to the neutral point current, such that an inherent dc-link capacitor voltage balancing can be achieved without using any active dc link voltage controls or additional dc link voltage and/or current sensors. The feasibility and effectiveness of proposed methods are verified by using both simulation and experimental studies.

Keywords: Direct torque control; motor drive; T-type inverter; virtual space vectors.

I. INTRODUCTION

The direct torque control (DTC) has been applied to various industrial applications, due to its advantages, such as fast dynamic response and robustness to system uncertainties and nonlinearities [1]-[3]. However, compared to the field-oriented control (FOC), the DTC may introduce much higher torque ripple and also higher total harmonic distortion (THD) in the motor currents. To reduce torque ripple, higher switching frequency is usually required by DTC, which however can cause poor drive efficiency. Using the emerging silicon carbide (SiC) devices, which can operate efficiently at much higher switching frequency than their silicon counterparts, it could be feasible to achieve high efficiency and low torque ripple simultaneously.

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Various improved DTC methods have been proposed to address the drawbacks of the conventional DTC. Improvements have been achieved through the use of enhanced modulation approaches and more effective DTC algorithms. For instance, the duty-cycle based DTCs [2]-[6] were proposed to reduce the torque ripple, where two [2], [4] or more [6] voltage vectors are applied over one control cycle. These methods rely on a simple modulator to realize constant switching frequency [7], which however leads to much higher switching losses. From the algorithm perspective, the direct torque and flux control (DTFC) [8], [9], dead-beat control [10], and predictive DTC [11], [12] and the space-vector-modulated (SVM) DTC [13] have been proposed to reduce the torque and flux ripples while retaining the merit such as the fast-dynamic response.

In addition to reduce the torque ripple from the control perspective, the drive performance enhancement can also be achieved through hardware innovations, e.g., employing the multilevel inverters (MLIs) instead of the conventional two-level inverters, especially for the medium- or high-voltage high power drives. The MLIs can generate higher number of voltage levels, which can reduce *dv/dt*, common mode voltages, torque ripple, and current THD. Among all MLIs [14]-[16], the most widely adopted one for medium voltage variable speed drives is the three-level (3-L) neutral point clamped (NPC) inverter [17]-[25]. The DTC drives for 3-L NPC usually have much lower torque and flux ripples compared to their 2-L counterparts, due to the higher numbers of the available voltage vectors.

In this work, a SiC 3-L T-NPC converter is utilized to study the effectiveness of the proposed enhanced DTC method for an interior permanent magnet (IPM) synchronous motor. Due to the oscillations of the neutral-point (NP) voltage, the dc-link voltage balancing is a primary challenge for the 3-L inverters, which can cause excessive voltage stresses on the power devices and dc-link capacitors [26]. In addition, the NP voltage oscillations can lead to lower order harmonics [27] in the output and over time deteriorates the dc-link capacitors and power devices. It is, therefore, desirable to achieve balanced voltage across the dc-link capacitors. In [28], a modified SVM-DTC approach is proposed where the medium voltage vectors are ignored, and the measured dc-link capacitor voltages are utilized to select appropriate small voltage vectors. References [29] and [30] have shown different control strategies for 3-L DTC drive where dc-link capacitor voltages and/or NP currents are measured to find the optimal voltage vector with zero neutral point current.

In this work, an enhanced DTC, using a refined voltage space vector diagram, is proposed. The voltage space vectors used in the proposed DTC only include the real space vectors

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and virtual space vectors (VSV) that do not affect the NP voltage, such that an inherent dc-link voltage balancing can be achieved without using additional dc-link voltage/current sensors or active feedback controls. In addition, the use of the additional VSVs and a multi-level hysteresis torque control in the proposed DTC algorithm can effectively reduce the torque and flux ripples while enhancing the dynamic response. Comprehensive simulations and experiments are conducted to validate the effectiveness of the proposed control scheme.

The remainder of the paper is structured as following. In Section II, the issues of the conventional DTC for the 3-L inverter are presented. In Section III, the proposed enhanced DTC algorithm is presented with the detail analysis. Then, simulation and experimental results are presented in Section IV to validate the feasibility and effectiveness of the proposed enhanced DTC.

II. Issues of the Conventional DTC for 3-L Inverters

To realize a 3-L inverter, there are various topologies available, including, NPC, Active NPC (ANPC) and T-type inverter. All of them are widely used in high power applications. Compared to T-type inverter, the NPC inverter has relatively higher conduction losses, since the load current always flows through two devices connected in series. In addition, the NPC converter has longer conduction path, which may lead to higher voltage stress when switching. Furthermore, the T-type inverter has a smaller number of devices compared to NPC due to the elimination of the clamping diodes [18]–[21]. In this paper, a T-type topology is adopted for the DTC implementation.

A. Modeling of A T-NPC Converter

A typical 3-L T-type topology is presented in Fig.1, where each phase consists of four switch positions, i.e., S_{a1}, S_{a2}, S_{a3} and S_{a4}, using phase a as an example. The S_{a1} and S_{a4} are in the normal half-bridge (HB) configuration, while the S_{a2} and S_{a3} are in the common source (CS) configuration. The output voltage vectors generated by the T-NPC [31] can be expressed as,

$$V = \frac{2}{3}(v_{ao} + k \cdot v_{bo} + k^2 \cdot v_{co}) \tag{1}$$

where, v_{ao}, v_{bo} and v_{co} are the voltages generated by the converter and k is $e^{j2\pi/3}$. Assuming constant and balanced dc-link capacitor voltages, the inverter phase terminal voltage, i.e., line-to-neutral voltage, can be expressed as

$$v_{xo} = s_x \frac{v_{dc}}{2} \tag{2}$$

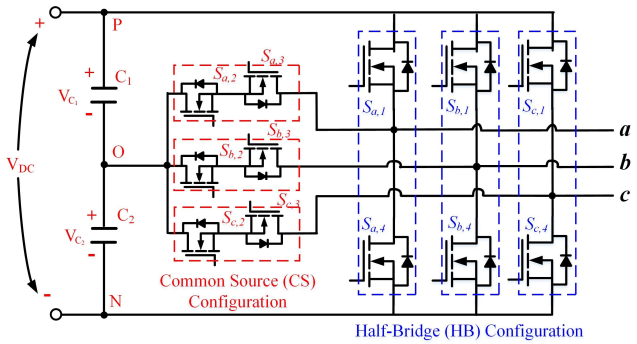

Fig. 1. Schematic of a T-type inverter.

where $x = \{a, b, c\}$ and $v_{dc} = v_{c1} + v_{c2}$. The s_x is the switching state of the phase x, i.e., P state, $s_x = 1$, where the inverter output terminal is connected to the positive rail of the dc-link; O state, $s_x = 0$, where the inverter output terminal is connected to the NP of the dc-link; and N state, $s_x = -1$, where the inverter output terminal is connected to the negative rail of the dc-link.

Fig. 2 shows all the space voltage vectors or the real voltage vectors (RVVs, to distinguish from the virtual space vectors defined later) that a 3-L inverter can generate. Table I summaries the relationships between the switching states and output terminal voltages for 3-L T-type converter phase leg [32]. The gate signals of $S_{x,1}$ and $S_{x,3}$ is always complementary to each other, so as the $S_{x,2}$ and $S_{x,4}$. Based on Table I, the switching state, formed by s_x of each phase and the extend form of the switching state, formed by $S_{x,1}$ and $S_{x,2}$ of each phase of an RVV, V_i, where $i = 0, 1, 2, \ldots, 19$, can be defined as

$$\begin{aligned} V_i &= [s_a\ s_b\ s_c]\text{(Switching States)} \\ &= [s_{a,1}\ s_{a,2}\ s_{b,1}\ s_{b,2}\ s_{c,1}\ s_{c,2}]\text{(Extended Form of Switching States)} \end{aligned} \tag{3}$$

For all the RVVs, the elements of the extended form of the switching states are either 0 or 1. Therefore, when one RVV is applied over a control cycle, there are no switching actions. For a 3-L inverter, all of the RVVs can be divided into four categories based on their amplitude [21], i.e., large voltage vectors ($V_1 \sim V_6$), medium voltage vectors ($V_7 \sim V_{12}$), smaller voltage vectors ($V_{13} \sim V_{18}$) and zero voltage vectors (V_0 and V_{19}).

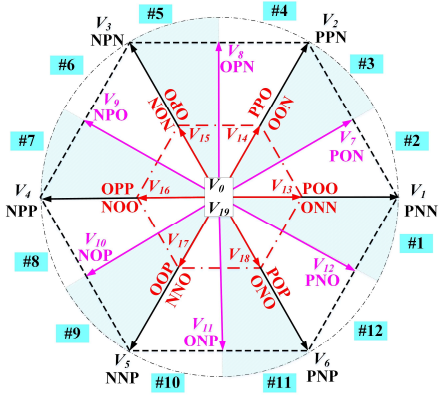

Fig. 2. The voltage vector diagram for a 3-L T-type inverter.

TABLE I
SWITCHING STATES OF A T-TYPE PHASE-LEG

Switching State s_x	Phase Voltage v_{Xo}	Gate Signals $s_{x,1}$	$s_{x,2}$	$s_{x,3}$	$s_{x,4}$
P	$+V_{dc}/2$	1	1	0	0
O	0	0	1	1	0
N	$-V_{dc}/2$	0	0	1	1

In this paper, an IPM motor is considered. The dynamics of the IPM motor can be represented in the dq rotating reference frame as,

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} R + sL_d & -\omega_{re}L_q \\ \omega_{re}L_d & R + sL_q \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_{re}\psi_m \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} \psi_d \\ \psi_q \end{bmatrix} = \begin{bmatrix} \psi_m + L_d i_d \\ L_q i_q \end{bmatrix} \tag{5}$$

where s is a derivative operator, v_d and v_q are the d- and q-axis stator voltages respectively; ω_{re} is the rotor electrical speed; L_d

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and L_q are the d- and q-axis inductances, respectively; ψ_m is the flux linkage produced by the permanent magnets, ψ_d and ψ_q are the d- and q-axis components of the stator flux linkage vector, respectively, and R is the stator resistance. From equation (4) and (5), $|\psi_s|$ can be calculated as

$$|\psi_s| = \sqrt{(\psi_d)^2 + (\psi_q)^2} = \sqrt{(\psi_m + L_d i_d)^2 + (L_q i_q)^2} \quad (6)$$

The electromagnetic torque, T_{em} generated by an IPM motor can be expressed in the dq rotor reference frame as

$$T_{em} = (3/2)P[\psi_m + (L_d - L_q)i_d]i_q \quad (7)$$

where P is the number of pole-pairs.

According to (6) and (7), torque and flux observers can be properly designed. In every control iteration in DTC, the estimated torque and flux are compared with the reference torque and flux. The errors between the estimations and their references are fed to the torque and flux hysteresis loop to select the appropriate voltage vector from the switching table. The four-level (±2, ±1) torque hysteresis [33] and two-level (±1) flux hysteresis controllers, as shown in Fig. 3 and Fig. 4, respectively, are used. Table II is the switching table of a conventional DTC for 3-L converter [29] to determine the proper voltage vector.

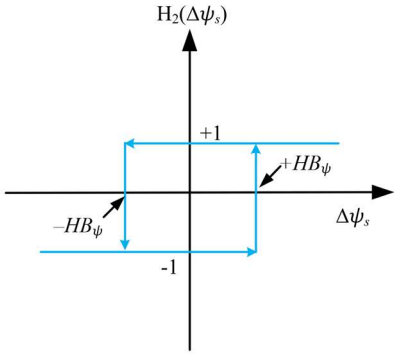

Fig. 3. Flux hysteresis comparator.

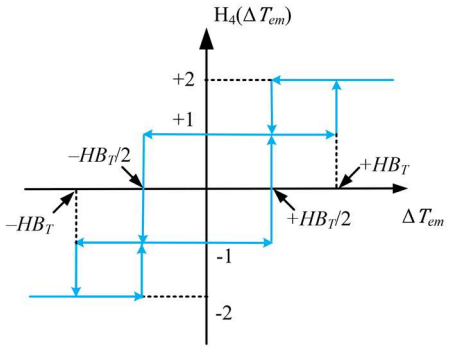

Fig. 4. Conventional four level torque hysteresis comparator.

As shown in Fig. 5, if the stator flux is located in sector #1 and reference torque tracking error, i.e., ΔT_{em}, is in the outer hysteresis band, i.e., $H_4(\Delta T_{em})$ = +2 or –2, there are four available voltage vectors, i.e., two large vectors V_2 and V_5 and two small vectors V_8 and V_{11}. By selecting the proper voltage vector, increasing or decreasing of the torque and stator flux can be achieved, i.e., 1) if V_2 is applied, both $|\psi_s|$ and torque angle, δ, are increased; 2) if V_8 is applied, $|\psi_s|$ is decreased, while δ is increased; 3) if V_5 is applied, both $|\psi_s|$ and δ are decreased; and 4) if V_{11} is applied, $|\psi_s|$ is increased, while δ is decreased. Similarly, if the stator flux is located in sector #1 while the ΔT_{em} is in the inner hysteresis band, i.e., $H_4(\Delta T_{em})$ = +1 or –1, Fig. 6 shows the effect of all 4 available voltage vectors. In Figs. 5 and 6, Ψ_r is denoated as the rotor flux.

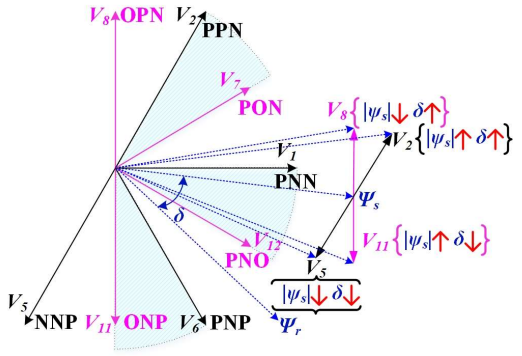

Fig. 5. The voltage vector selection when ΔT_{em} is in outer hysteresis band.

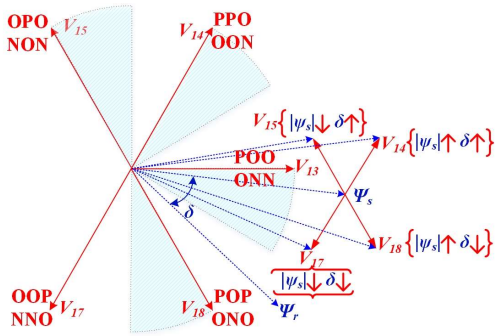

Fig. 6. The voltage vector selection when ΔT_{em} is in inner hysteresis band.

B. *Effect of the RVVs on the NP Voltage*

For a 3-L T-NPC converter, the dc-link usually consists of two identical capacitors sharing the entire dc bus voltage. In the P state, the voltage of the phase terminal with respect to the dc-link neutral point, i.e., V_P, equals to the voltage across the top

TABLE II
THE SWITCHING TABLE OF THE CONVENTIONAL DTC FOR 3-L INVERTER

$H_2(\Delta\psi_s)$	$H_4(\Delta T_{em})$	Sector Number											
		1	2	3	4	5	6	7	8	9	10	11	12
+1	+2	V_2	V_8	V_3	V_9	V_4	V_{10}	V_5	V_{11}	V_6	V_{12}	V_1	V_7
	+1	V_{14}	V_{14}	V_{15}	V_{15}	V_{16}	V_{16}	V_{17}	V_{17}	V_{18}	V_{18}	V_{13}	V_{13}
	–1	V_{18}	V_{18}	V_{13}	V_{13}	V_{14}	V_{14}	V_{15}	V_{15}	V_{16}	V_{16}	V_{17}	V_{17}
	–2	V_8	V_6	V_9	V_1	V_{10}	V_2	V_{11}	V_3	V_{12}	V_4	V_7	V_5
–1	+2	V_{11}	V_3	V_{12}	V_4	V_7	V_5	V_8	V_6	V_9	V_1	V_{10}	V_2
	+1	V_{15}	V_{15}	V_{16}	V_{16}	V_{17}	V_{17}	V_{18}	V_{18}	V_{13}	V_{13}	V_{14}	V_{14}
	–1	V_{17}	V_{17}	V_{18}	V_{18}	V_{13}	V_{13}	V_{14}	V_{14}	V_{15}	V_{15}	V_{16}	V_{16}
	–2	V_5	V_{11}	V_6	V_{12}	V_1	V_7	V_2	V_8	V_3	V_9	V_4	V_{10}

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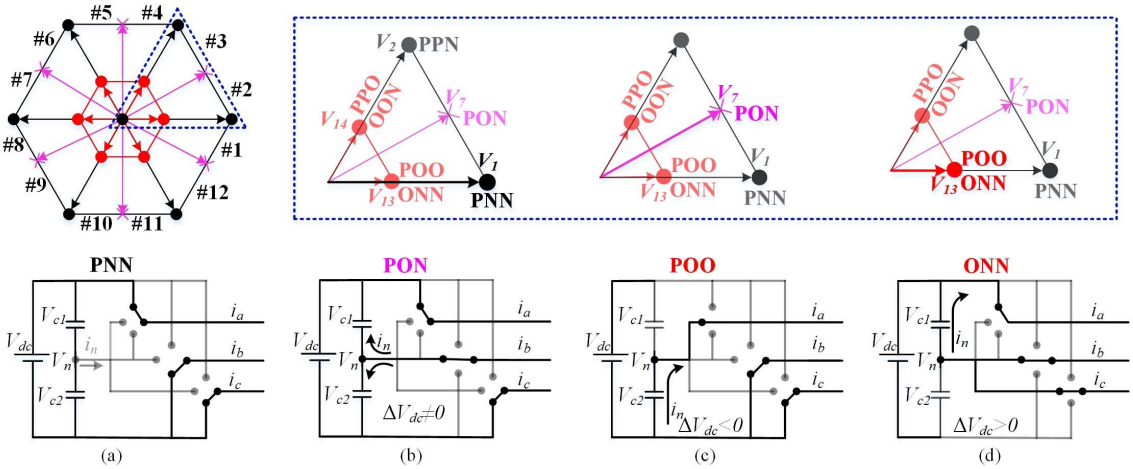

Fig. 7. Circuit diagram for vectors and their influence on NP voltage.

capacitor. During N state, the voltage of the phase terminal with respect to the dc-link neutral point, i.e., V_N, equals to the voltage across the bottom capacitor, but with an opposite sign. For a 3-L converter, the $|V_P|$ and $|V_N|$ should be identical if the voltages across the two dc-link capacitors are the same, i.e., the top and bottom capacitors sharing the dc bus voltage equally. Otherwise, the output voltage waveform will be distorted with increased harmonic components and increased voltage stresses on the power devices [34], [35]. Therefore, the dc-link voltage balancing is necessary to reduce the harmonic and maintain the essential function of the converter.

There are four types of voltage vectors for a T-NPC converter, with each of them has different influence on the NP voltage, i.e., the voltage of the NP with respect to the ground. To analyze the influence of different vectors, as shown in Fig. 7, Sectors 2 and 3 are used as an example for illustration. In Fig. 7, the equivalent circuits for the large vector V_1 (PNN), medium vector V_7 (PON) and small voltage vector V_{13} (POO and ONN) are presented [36]. When V_1 is applied, as shown in Fig. 7(a), both top and bottom capacitors are connected in the circuit, while the NP is not connected to the load. Therefore, the two capacitors are either charged or discharged by the same current. Consequently, V_1 does not lead to dc-link voltage unbalancing. When V_7 is applied, as shown in Fig. 7(b), both the top and bottom capacitors are connected in the circuit as well. However, the NP is also connected to the load, which leads to a non-zero NP current. Therefore, the currents flow through the two dc-link capacitors are different, which can cause dc-link voltage unbalancing. The two possible switching states for the small vector V_{13} is shown in Fig. 7(c) and (d). These two switching states, i.e., POO and ONN, connect different dc-link capacitors to the load through the NP. When $i_a > 0$, switching state ONN reduces V_{c2} and leads to a positive ΔV_{dc}, i.e., $\Delta V_{dc} = V_{c2} - V_{c1}$, while POO reduces V_{c1} and leads to a negative ΔV_{dc}. When $i_a < 0$, the result is the opposite. As a conclusion, the medium voltage vectors affect the NP voltage; the two switching states of a small vector have opposite influence on the NP voltage. If the voltage vectors are not selected carefully, the dc-link voltage unbalance can occur.

C. *Effect of Unbalanced DC Link on Torque Ripple and Stator Current Ripple*

In a conventional DTC for 3-L converter, usually only one voltage vector is applied throughout an entire sampling period. According to previous discussion, if one of the small or medium voltage vectors is applied, the unbalanced dc-link voltage will occur, which can lead to increased ripples in the stator currents. The presence of the ripples in the stator currents can be translated to the torque ripple [37]. Due to the complexity to derive an explicit model of toque ripple due to dc link unbalance in a multilevel DTC drive for an IPM motor, in this work, a numerical analysis was conducted to visualize the relationship between the torque ripple and stator current ripple due to the dc-link capacitor voltages unbalancing. The key parameters of the IPM motor are L_d = 1.12 mH, L_q = 1.58 mH, rotor flux linkage 0.035Wb, and maximum torque 0.8 Nm.

Fig. 8 shows that effect of the ΔV_{dc} on the torque ripple, where the torque ripple and ΔV_{dc} are shown in percentage (%). The study has been performed at full torque, 50% and 25% of the full torque. It is clear from the figure that when the dc-link capacitor voltages are not balanced the torque ripple would be higher. It is worth to mention that the torque ripple reduces at higher speed. Fig. 9 shows the effect of ΔV_{dc} on the stator current THD. It is possible to conclude from the figure that when the dc-link capacitor voltages are not balanced properly or if there is any bias/offset between two dc-link capacitor voltages, the stator current THD would be higher.

III. The Proposed Enhanced DTC with Virtual Space Vectors

The dc-link unbalancing issue in the conventional DTC for a 3-L converter can be mitigated by using the sensed voltages of the two capacitors and/or the NP current to determine the proper voltage vector, which however can increase the system cost and the controller complexity. Now, for a NPC converter, NP current, i_n is the main reason behind the dc-link balancing or unbalancing. Ideally, the average neutral point current, i_n, should be zero to keep the capacitor voltages balanced within a switching cycle, T_s [36]. In order to achieve the zero average neutral point current, the virtual voltage vectors scheme can be

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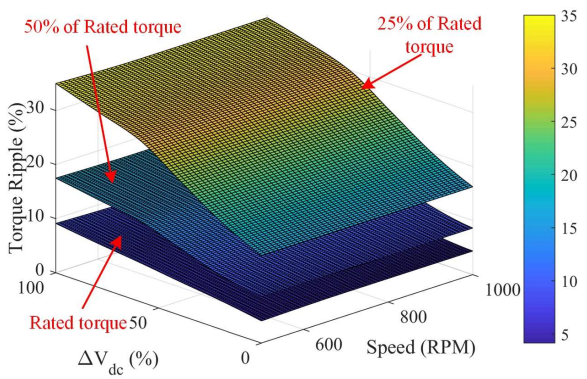

Fig. 8. Relationship among torque ripple (%), ΔV_{dc} and speed (RPM).

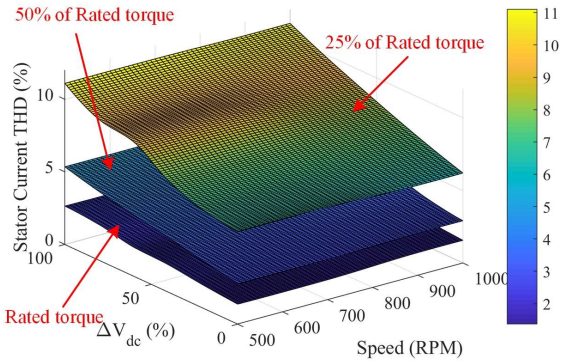

Fig. 9. Relationship among stator current THD (%), ΔV_{dc}, and speed (RPM).

used, which is first introduced in [38]. In this paper, the VSV concept is integrated with the DTC scheme, and VSVs are generated by using the combinations of real voltage vectors (RVVs). The objective of proposed DTC is to achieve an inherent dc-link voltage balancing without using the additional dc link voltage and current sensors. In the proposed method, only the voltage vectors, including original large voltage vector and the VSVs, that do not affect the NP voltage are used. In addition, due to the use of additional VSVs in the DTC, the ripples in the stator current and torque can be reduced.

A. The Proposed Space Vector Diagram

According to the analysis presented in Section II.B, among all the RVVs, the large voltage vectors ($V_1 \sim V_6$) do not affect the NP voltage, while both medium vectors ($V_7 \sim V_{12}$) and small vectors ($V_{13} \sim V_{18}$) can lead to the change of the NP voltage. This conclusion is illustrated in Fig. 10(a), where it is also clearly to see two regular hexagons formed by various voltage vectors, i.e., (1) the outer hexagon formed by large voltage vectors ($V_1 \sim V_6$) and the medium vectors ($V_7 \sim V_{12}$) and (2) the inner hexagon formed by small vectors ($V_{13} \sim V_{18}$). In Fig. 10, the voltage vectors end with red dots are the RVVs that do not affect the NP voltage, while the voltage vectors end with yellow stars are the RVVs affecting the NP voltage.

The proposed voltage space vector diagram is shown in Fig. 10(b). On the outer hexagon, the original medium RVV ($V_7 \sim V_{12}$) are all replaced by the VSVs, while the large RVVs remain the same. The VSVs replacing the original RVVs are still using the same vector numbers but distinguished by a different color in Fig. 10(b). On the inner hexagon, the original small RVV ($V_{13} \sim V_{18}$) are all replaced by the VSVs. In addition, similar to the medium voltage vectors with their tips on the middle of the sides of the outer hexagon, six additional VSVs ($V_{33} \sim V_{38}$) were added and their tips are on the middle of the sides of the inner hexagon. Furthermore, to reduce the torque and flux ripple, a middle hexagon was added, which is formed by 12 VSVs, i.e., $V_{20} \sim V_{31}$. The tips of VSVs $V_{20} \sim V_{25}$ located on the middle of the sides of the middle hexagon, while the tips of VSVs $V_{26} \sim V_{31}$ located on the vertices of the middle hexagon. The details of each hexagon are illustrated in Figs. 10(c)-(e).

All the 36 non-zero voltage vectors in Fig. 10(b) are synthesized as follows,

1. The large voltage vectors, i.e., V_1 to V_6, are kept same as the original since they do not affect the NP current.
2. The VSVs V_7 to V_{12} are synthesized by applying each of the two nearest large voltage vectors for $T_s/2$. Using V_7 as an example

$$\begin{aligned} V_i &= \frac{V_1[0]+V_2[0]}{2} = \frac{[P\ N\ N]+[P\ P\ N]}{2} \\ &= \left[\frac{1+1}{2}\ \frac{1+1}{2}\ \frac{0+1}{2}\ \frac{0+1}{2}\ \frac{0+0}{2}\ \frac{0+0}{2}\right] \\ &= [1\,1\,0.5\,0.5\,0\,0] \end{aligned} \tag{8}$$

   For the new V_7, each of the V_1 with switching state PNN and V_2 with switching state PPN is applied for half of the sampling period, i.e., $T_s/2$. This new voltage vector is equivalent to middle RVV but does not contribute any NP current. In addition, it is obvious to observe from (8) that the elements in the extended form of the switching state for the VSV may be fractional number, which is different from RVV, where all the elements are either 1 or 0.

3. For the VSVs V_{13} to V_{18}, using V_{13} as an example,

$$\begin{aligned} V_{13} &= \frac{1}{2}\left(V_{13}[i_a]+V_{13}[-i_a]\right) = \frac{[P\ \ O\ \ O]+[O\ \ N\ \ N]}{2} \\ &= \left[\frac{1+0}{2}\ \ \frac{1+1}{2}\ \ \frac{0+0}{2}\ \ \frac{1+0}{2}\ \ \frac{0+0}{2}\ \ \frac{1+0}{2}\right] \\ &= [0.5\ \ 1\ \ 0\ \ 0.5\ \ 0\ \ 0.5] \end{aligned} \tag{9}$$

   where $V_{13}[i_a]$ is the original small RVV with switching state POO, which leads to an NP current i_a; $V_{13}[-i_a]$ has switching state ONN, which leads to an NP current $-i_a$. According to (9), if each vector is applied for half of the sampling period $T_s/2$, the average NP current over a sampling period T_s should be zero, such that the NP voltage would not be affected when this synthesized VSV is applied.

4. The VSVs, V_{20} to V_{25}, are generated by the nearest two small RVVs and the middle RVV, so that the NP current is zero. For instance, V_{20} is synthesized as,

$$\begin{aligned} V_{20} &= \frac{1}{3}V_{13}[i_a]+\frac{1}{3}V_{14}[i_c]+\frac{1}{3}V_7[i_b] \\ &= \frac{[O\ \ N\ \ N]+[P\ \ P\ \ O]+[P\ \ O\ \ N]}{3} \\ &= \left[\frac{0+1+1}{3}\ \ \frac{1+1+1}{3}\ \ \frac{0+1+0}{3}\ \ \frac{0+1+1}{3}\right. \\ &\quad \left.\frac{0+0+0}{3}\ \ \frac{0+1+0}{3}\right] \\ &= [0.6667\ \ 1\ \ 0.3333\ \ 0.6667\ \ 0\ \ 0.3333] \end{aligned} \tag{10}$$

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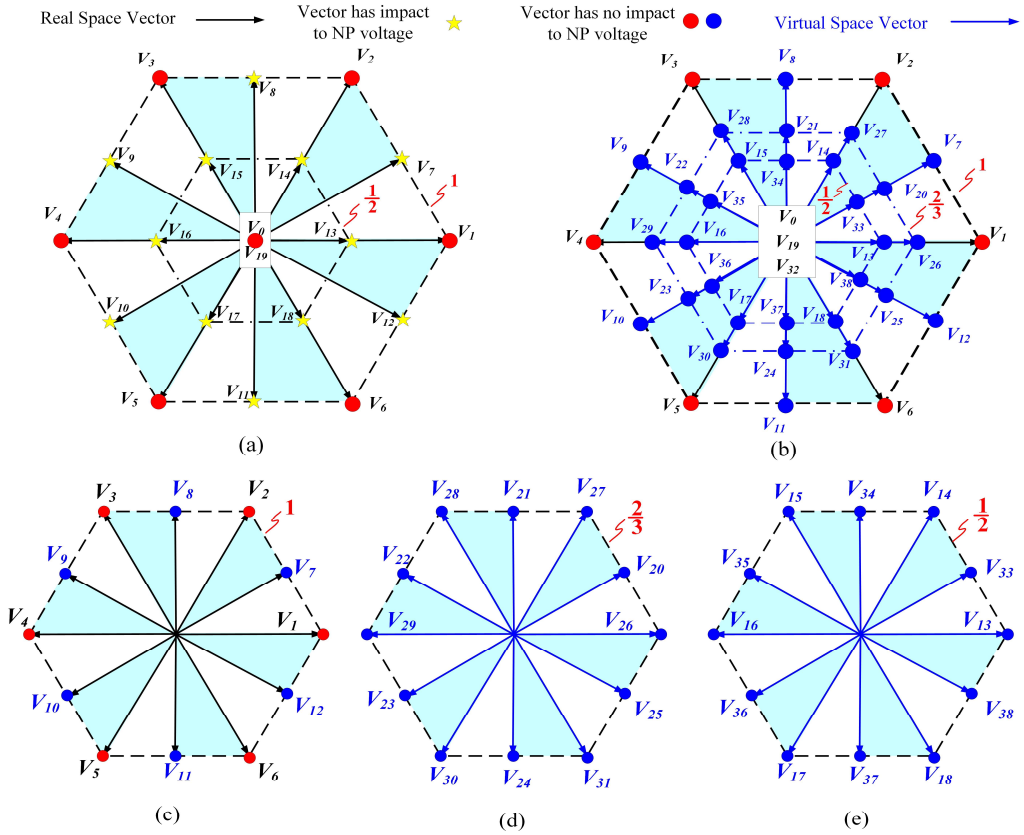

Fig. 10. The proposed space vector diagram.

5. The VSVs, V_{26} to V_{31} are synthesized by tacking 2/3 of their corresponding large voltage vectors and 1/3 of the zero-voltage vectors. For instance, V_{26} is calculated by,

$$V_{26}=\frac{2}{3}V_1[0]+\frac{1}{3}V_{19}[0]=\frac{2}{3}[P\quad N\quad N]+\frac{1}{3}[N\quad N\quad N]$$
$$=\left[\frac{(2\times1)+0}{3}\quad\frac{(2\times1)+0}{3}\quad\frac{(2\times0)+0}{3}\quad\frac{(2\times0)+0}{3}\quad\frac{(2\times0)+0}{3}\quad\frac{(2\times0)+0}{3}\right] \tag{11}$$
$$=[0.6667\quad 0.6667\quad 0\quad 0\quad 0\quad 0]$$

In (11), V_1 is used, which doesn't affect NP current, to generate V_{26}. Therefore, V_{26} does not affect the NP current.

6. The VSVs, V_{33} to V_{38} are generated using the two nearest small VSVs. As an example, V_{33} is calculated as,

$$V_{33}=\frac{1}{2}\left(V_{13}[0]+V_{14}[0]\right)=\left[\frac{0.5+0.5}{2}\quad\frac{1+1}{2}\quad\frac{0+0.5}{2}\quad\frac{0.5+1}{2}\quad\frac{0+0}{2}\quad\frac{0.5+0.5}{2}\right] \tag{12}$$
$$=[0.5\quad 1\quad 0.25\quad 0.75\quad 0\quad 0.5]$$

B. The Proposed Multilevel Torque Hysteresis Controller

Since the proposed voltage vector diagram has three layers of voltage hexagons, a six-level torque hysteresis controller as shown in Fig. 11 is proposed and applied to the proposed DTC. The $\pm HB_T$ represents the outer torque hysteresis band, while the $\pm\alpha\cdot HB_T$ and $\pm\beta\cdot HB_T$ are the inner and middle torque hysteresis bands, respectively. The values for the α and β are tuned offline to trade the dynamic response against the steady state torque tracking error. When the torque tracking error falls within the inner band, i.e., the output of the torque hysteresis $H_6(\Delta T_{em})$ = ±1, the voltage vector to be applied in the next control cycle is chosen from the vectors on the inner voltage hexagon, i.e., V_{13} ~ V_{18} and V_{33} ~ V_{38}, which has the lowest impact to the torque. When the torque tracking error falls within the middle band, i.e., $H_6(\Delta T_{em})$ = ±2, the voltage vector to be applied in the next control cycle is chosen from the vectors on the middle voltage hexagon, i.e., V_{20} ~ V_{25} and V_{26} ~ V_{31}, which has higher impact to the torque than the small voltage vectors due to the higher voltage magnitude. For other conditions, vectors on the outer voltage hexagon are applied. The proposed switching

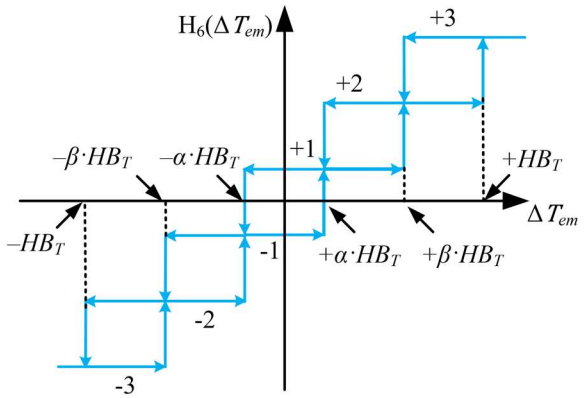

Fig. 11. Modified 6-L torque comparator.

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TABLE III
PROPOSED SWITCHING TABLE

$H(\Delta\psi_s)$	$H_6(\Delta T_{em})$	Sector 1	2	3	4	5	6	7	8	9	10	11	12
+1	+3	V_2	V_8	V_3	V_9	V_4	V_{10}	V_5	V_{11}	V_6	V_{12}	V_1	V_7
	+2	V_{27}	V_{21}	V_{28}	V_{22}	V_{29}	V_{23}	V_{30}	V_{24}	V_{31}	V_{25}	V_{26}	V_{20}
	+1	V_{14}	V_{34}	V_{15}	V_{35}	V_{16}	V_{36}	V_{17}	V_{37}	V_{18}	V_{38}	V_{13}	V_{33}
	–1	V_{18}	V_{38}	V_{13}	V_{33}	V_{14}	V_{34}	V_{15}	V_{35}	V_{16}	V_{36}	V_{17}	V_{37}
	–2	V_{31}	V_{25}	V_{26}	V_{20}	V_{27}	V_{21}	V_{28}	V_{22}	V_{29}	V_{23}	V_{30}	V_{24}
	-3	V_{11}	V_6	V_{12}	V_1	V_7	V_2	V_8	V_3	V_9	V_4	V_{10}	V_5
–1	+3	V_8	V_3	V_9	V_4	V_{10}	V_5	V_{11}	V_6	V_{12}	V_1	V_7	V_2
	+2	V_{28}	V_{22}	V_{29}	V_{23}	V_{30}	V_{24}	V_{31}	V_{25}	V_{26}	V_{20}	V_{27}	V_{21}
	+1	V_{15}	V_{35}	V_{16}	V_{36}	V_{17}	V_{37}	V_{18}	V_{38}	V_{13}	V_{33}	V_{14}	V_{34}
	–1	V_{17}	V_{37}	V_{18}	V_{38}	V_{13}	V_{33}	V_{14}	V_{34}	V_{15}	V_{35}	V_{16}	V_{36}
	–2	V_{30}	V_{24}	V_{31}	V_{25}	V_{26}	V_{20}	V_{27}	V_{21}	V_{28}	V_{22}	V_{29}	V_{23}
	-3	V_5	V_{11}	V_6	V_{12}	V_1	V_7	V_2	V_8	V_3	V_9	V_4	V_{10}

sequences depending on the torque and flux hysteresis loop is shown in Table III.

C. Generate Gate Signals for the VSVs Using a Modulator

An external modulator [39] is introduced to generate the gate signals for the VSVs to be used in the proposed DTC controller. This modulator compares the elements in the extend form of the switching states of voltage vectors, which are similar to the duty ratios, selected by the DTC algorithm to a carrier waveform having a fixed switching frequency. As an example, Fig. 12 shows gate signal generation for the VSV V_{25}, whose extended form of switching state is $[s_{a,1}\ s_{a,2}\ s_{b,1}\ s_{b,2}\ s_{c,1}\ s_{c,2}]$ = [2/3 1 0 1/3 1/3 2/3].

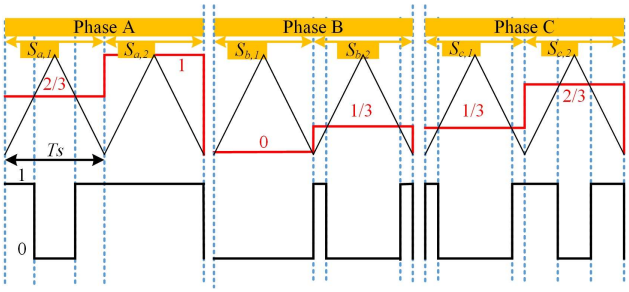

Fig. 12. Gate signal generation of voltage vector V_{25}.

D. Overview of the Proposed DTC

Fig. 13 shows the block diagram of the proposed DTC approach, which still includes the hysteresis controllers for the stator flux linkage and the electromagnetic torque and their corresponding estimators. The flux hysteresis controller is the conventional 2-L hysteresis with the output as $H_2(\Delta\psi_s)$, as shown in Fig. 3, while the torque hysteresis controller is the proposed 6-L hystersis, who output is denoted as $H_6(\Delta T_{em})$. The $H_2(\Delta\psi_s)$ and $H_6(\Delta T_{em})$ are used to identify the optimal voltage space vector to be applied in the next control cycle from the Table III, which is the siwtching table. Once the optimal voltage space vector is selected, its extended form of switching state is sent to an external modulator to generate all the gate signals for a T-type inverter. Due to the use of one or more voltage vectors over a control iteration, the equivalent switching frequency is higher, which helps reduce the current and torque ripples. Compared to the SVM-DTC, since the proposed DTC still uses the discrete voltage vectors, which retain the merits such as the fast-dynamic performance.

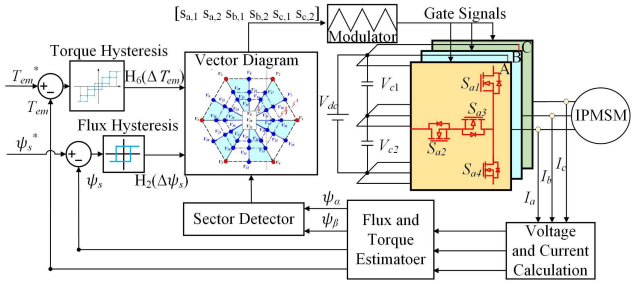

Fig. 13. A block diagram of the enhanced DTC.

IV. SIMULATION AND EXPERIMENTAL STUDIES

A. Simulation Studies:

In this section, simulation results are presented to validate the effectiveness of the proposed enhanced DTC. The machine parameters used in the simulation are presented in Table IV. The motor mechanical speed was kept constant at 500 RPM with a varying torque reference. The sampling frequency of the DTC algorithm in the simulation studies is 50 kHz.

TABLE IV
MACHINE PARAMETERS

Nominal Power	250 W
Maximum torque	0.8 Nm
Flux linkage	0.035Wb
Average L_d	1.12mH
Average L_q	1.58 mH
Base speed	3000 RPM
Pole-pair number	2
Stator resistance	0.27 Ω

Fig. 14 shows the dc-link capacitor voltages, i.e., V_{c1} and V_{c2}, when using the conventional DTC for 3-L T-type converter with additional dc-link voltage balancing control, which requires the measurements of the two capacitor voltages. The torque reference firstly increased from 0.3Nm to 0.7Nm and then step changed to -0.3Nm. As show in Fig. 14, the ripples of the dc link capacitor voltages are higher with larger torque reference. However, the dc capacitor voltages diverged when torque changed its direction with

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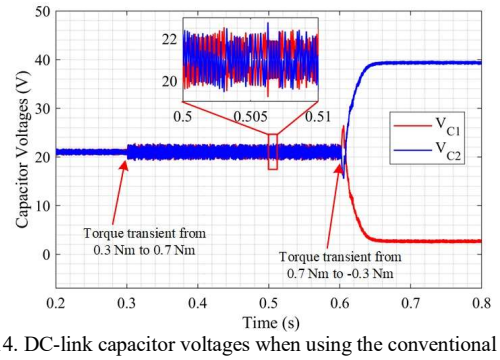

Fig. 14. DC-link capacitor voltages when using the conventional DTC.

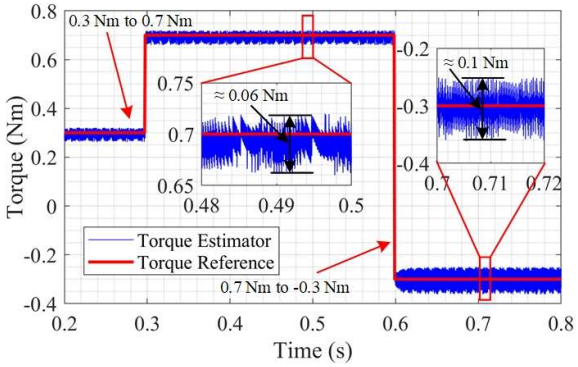

Fig. 15. Torque response when using the conventional DTC.

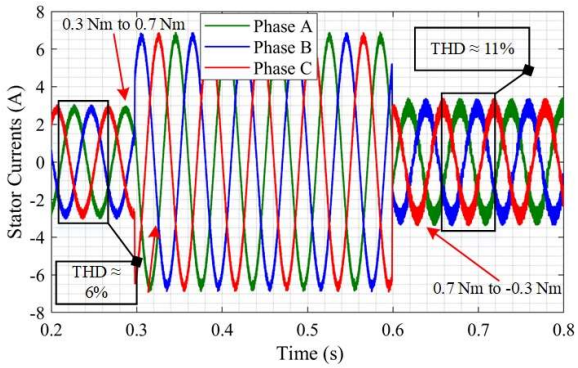

Fig. 16. Three phase stator currents when using the conventional DTC.

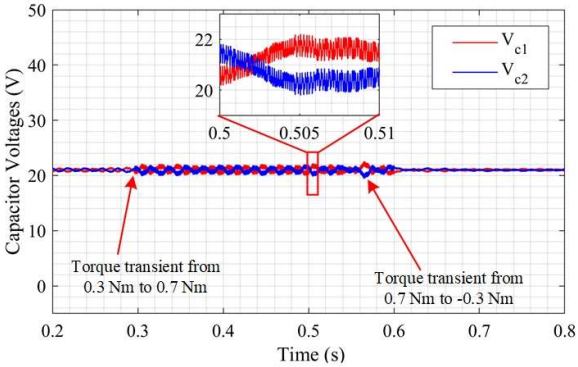

Fig. 17. DC-link capacitor voltages with proposed enhanced DTC.

V_{c1} dropped to zero, while V_{c2} was equal to the dc bus voltage. In this condition, the 3-L inverter operated as a 2-level inverter, which however may overstress the power devices and bottom capacitors in practical applications if they are selected based on half of the dc bus voltage. Fig. 15 shows the torque ripple before and after unbalanced dc-link voltages, when using the conventional DTC, while Fig. 16 shows the corresponding stator currents, whose THD was 6 % when the dc-link was balanced and 11% with unbalanced dc link. Fig. 17 shows the capacitor voltages when using the proposed DTC under the same torque reference profile. The voltage ripples were noticeably reduced, and system remained stable when torque direction changed. Fig. 18 shows the torque ripple when using the proposed method, which shows a clear torque ripple reduction, while Fig. 19

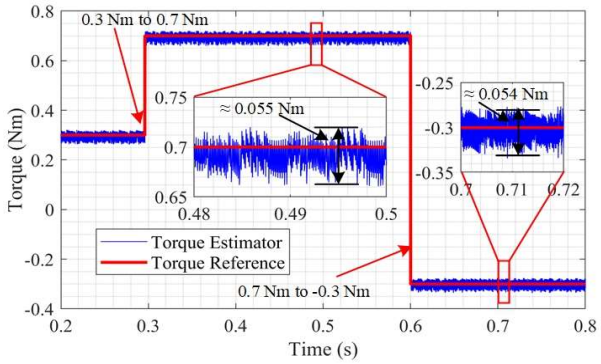

Fig. 18. Torque response with proposed DTC.

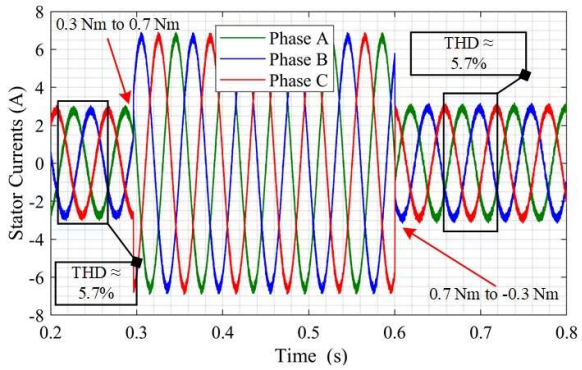

Fig. 19. Three phase stator currents with proposed DTC.

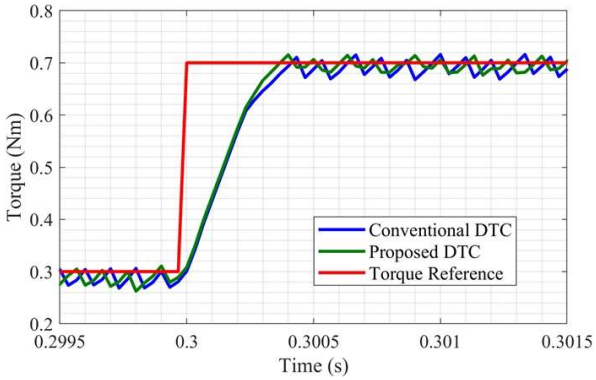

Fig. 20. Comparison of the dynamic responses.

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shows the phase current THD, which was also lower than the case using conventional DTC.

The dynamic performance was also evaluated for both the conventional and proposed DTC as shown in Fig. 20. The dc link capacitor voltages were clamped at constant using dc voltage sources, such that this simulation study can reveal the dynamic performance of both method without the dc link unbalancing issue. The proposed DTC used the same hysteresis band as the conventional DTC. Therefore, in the beginning, both methods had the same slew rate of the torque increase. Then proposed DTC had higher slew rate of the torque increase due to the insertion of middle voltage hexagon, while the conventional DTC was using the vectors on the inner voltage hexagon. At the steady state, both methods had the similar torque ripple. Both methods were validated for variable speed profiles. Fig. 21 and Fig. 22 represent reference toque and torque estimator output under different speeds. As shown in Fig. 21, at higher speed and speed reversal, due to dc-link capacitor voltage offset, the conventional method suffers from high torque ripples. On the other hand, the proposed DTC method has lower torque ripple which can be seen from Fig. 22.

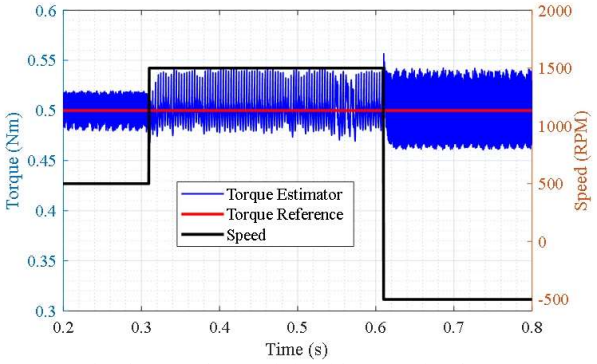

Fig. 21. Speed and torque characteristic with conventional DTC

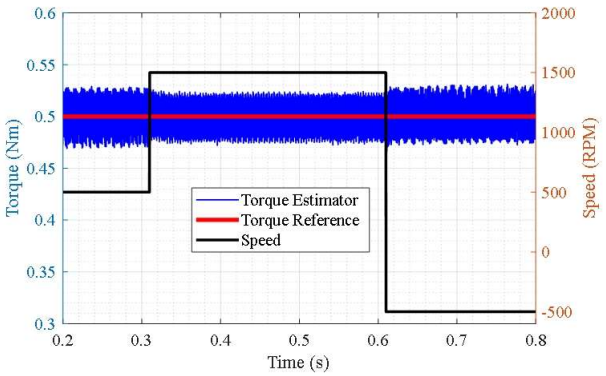

Fig. 22. Speed and torque characteristic with proposed DTC.

B. *Inverter Loss Analysis*

Inverter losses are major part of the overall system loss. Due to the additional switching actions of the proposed DTC, the system efficiency can be lower than that when using the conventional DTC. Therefore, in this section T-type inverter losses are evaluated for both conventional and proposed DTC approaches to quantify the impact to the system efficiency. Switching losses and conduction losses data are extracted from the device datasheet [40]. The conduction loss of a MOSFET is the 1st or 3rd quadrant can be determined as (13) and (14), respectively [22], [32],

$$P_{con(F)} = I_D^2 \cdot R_{DS(on)(F)} \tag{13}$$

$$P_{con(R)} = \begin{cases} I_D^2 \cdot R_{DS(on)(R)}, I_D \le I_{SC} \\ I_D^2 \cdot R'_{DS(on)(R)} + V_{TH} \cdot I_D, I_D > I_{SC} \end{cases} \tag{14}$$

where, I_D and I_{SC} are the MOSFET drain and the threshold current, respectively. $R_{DS(on)(F)}$ and $R_{DS(on)(R)}$ are the ON-state resistances of the devices. $R'_{DS(on)(R)}$ and V_{TH} are the equivalent resistance and the voltage source of the MOSFET and diode parallel circuit, respectively. The switching loss can be represented as,

$$E_{on} = \frac{E_{on(datasheet)} \cdot V_{DS(test)}}{V_{DS(datasheet)}} \tag{15}$$

$$E_{off} = \frac{E_{off(datasheet)} \cdot V_{DS(test)}}{V_{DS(datasheet)}} \tag{16}$$

where, E_{on} and E_{off} are the device turn-on and turn-off losses. $E_{on(datasheet)}$ and $E_{on(datasheet)}$ are turn-on and turn-off losses at a specific voltage mentioned in the datasheet. $V_{DS(datasheet)}$ is the voltage used in the switching characterization by the manufacturer also specified in the datasheet. The diode reverse recovery loss can be denoted as,

$$E_{rr} = \frac{E_{rr(datasheet)} \cdot V_{DS(test)}}{V_{DS(datasheet)}} \tag{17}$$

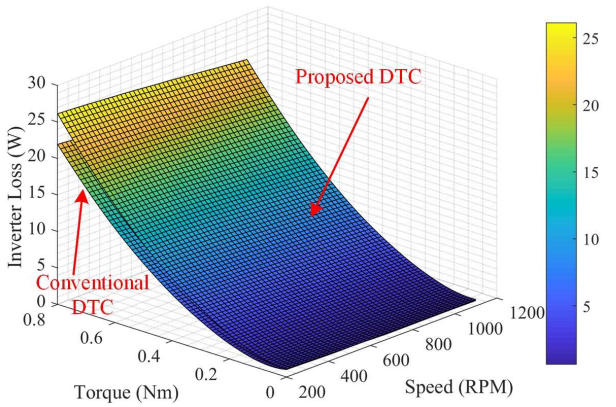

Fig. 23. 3D map of the inverter loss comparison between the conventional and proposed DTC.

Simulation for different operating conditions are conducted to derive the losses for conventional and proposed DTC method. As shown in Fig. 23, since the proposed method has higher equivalent switching frequency, it has higher switching losses than the conventional DTC. However, since the SiC MOSFETs are used in this study, the power devices conduction losses are still dominant. Therefore. The

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efficiency of the system is reduced less than 1% over a wide operating range using the proposed method.

C. *Experimental Studies:*

To further validate the effectiveness of the proposed DTC with additional VSV, experimental studies were performed. The experiment was carried out on the prototype of an all SiC T-type inverter. A 250 W IPM motor was used in the experiment with major parameters shown in Table IV. The overall DTC algorithm is implemented on MicrolabBox dSPACE real time control system. The overall experimental setup is shown in Fig. 24, which consists of an IPM motor controlled by a 3-L T-type inverter, and a DC motor is also adopted to drive the IPM motor and keep a constant speed, which is controlled by a H-bridge converter. The sampling frequency of the DTC is 50 kHz at variable motor shaft speed.

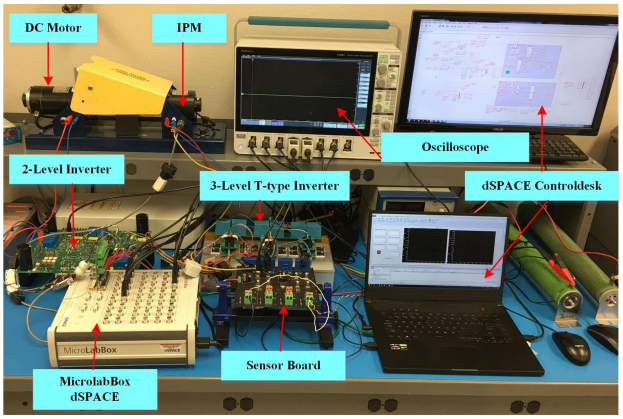

Fig. 24. Experimental setup.

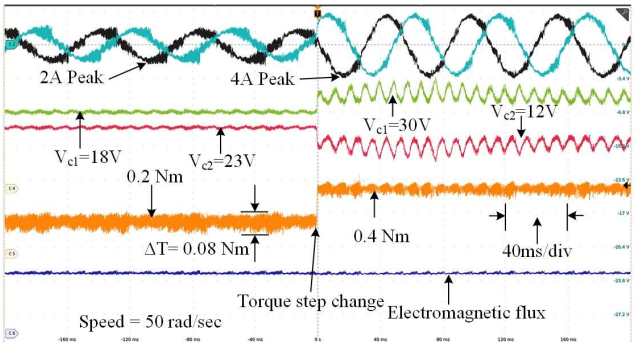

Fig. 25. DC-link unbalanced condition with torque transient.

Fig. 25 shows the experimental results when using conventional DTC without an additional control loop for dc-link voltage, as such the dc-link capacitor voltages were biased and unequal to each other. It is clear to observed from Fig. 25 that when ΔV_{dc} is almost 60% then the torque ripple is around 40% which were close to the numerical analysis done in Fig. 8. To compare with proposed DTC, experiment was conducted, and results are shown in Fig. 26, where the dc capacitor voltages were quite close to each other before and after torque step change. Also, from Fig. 26, it is visible that both torque and stator current ripples reduced significantly. Fig. 27 shows the speed transient response when the dc-link balanced. Torque response with step change in the torque command is shown in Fig. 28, where the dynamic responses are similar to each other under the conventional and proposed DTC.

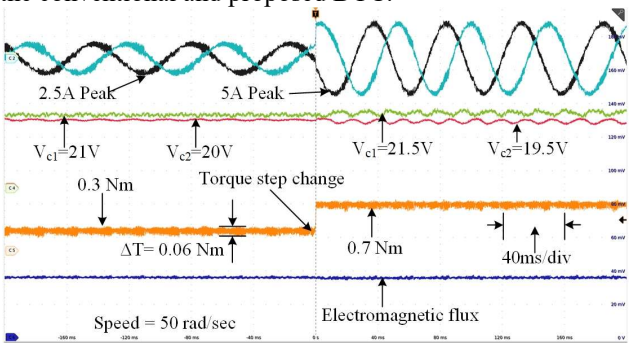

Fig. 26. DC-link balanced condition with torque transient.

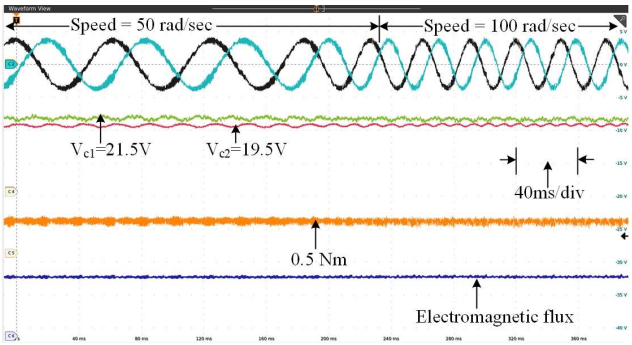

Fig. 27. DC-link balanced condition with speed transient.

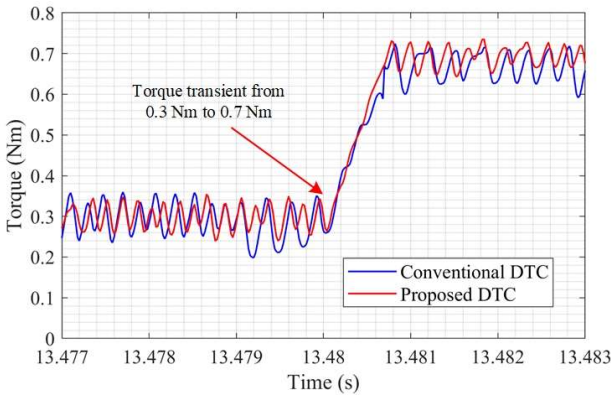

Fig. 28. Torque dynamics for both conventional DTC and proposed DTC.

To compare the performance of the proposed method with the conventional DTC over a wide range of speeds, various tests were conducted. Figs. 29 to 32 are the results at low speeds and in flux weakening mode for both conventional and proposed method, respectively. In Fig. 29, the speed command is 100 RPM. The conventional DTC can balance the dc-link voltages with higher ripples in the

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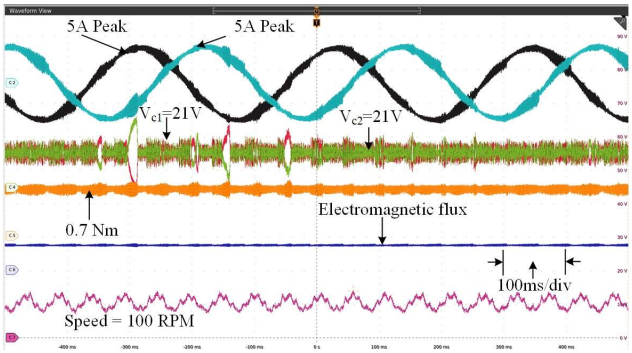

Fig. 29. Low speed response with conventional DTC.

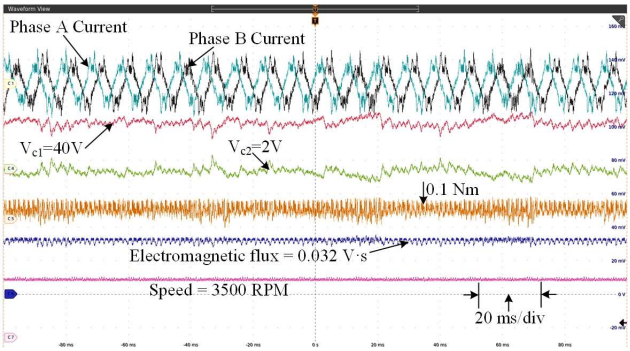

Fig. 30. Conventional DTC in flux weakening region.

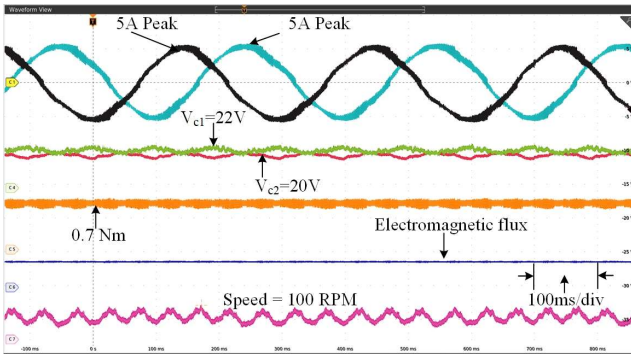

Fig. 31. Low speed response with proposed DTC.

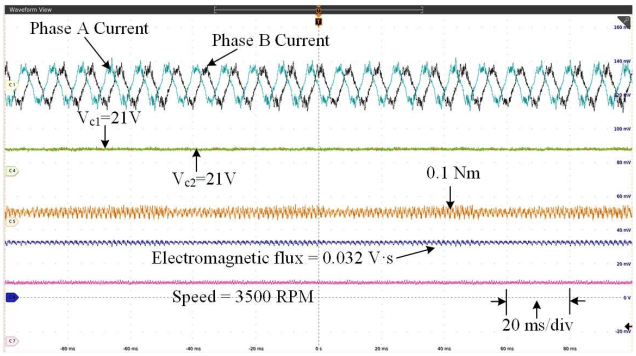

Fig. 32. Proposed DTC in flux weakening region.

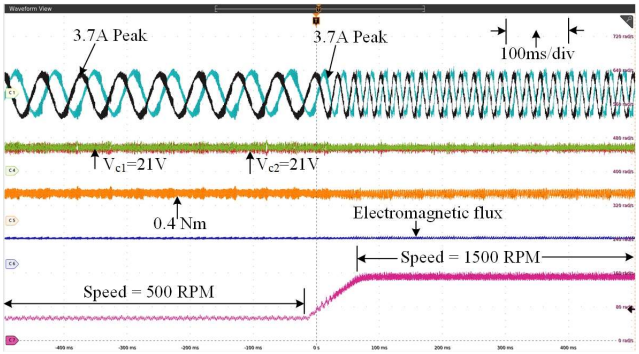

Fig. 33. Acceleration of the motor with conventional DTC.

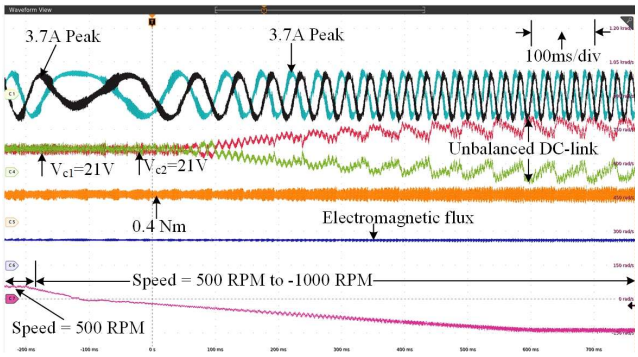

Fig. 34. Speed reversal of the motor with conventional DTC.

stator current and torque compared to Fig. 31, where the results for proposed DTC are shown with same operating conditions. Operation in the flux weakening mode was also evaluated using conventional and proposed DTC as shown in Fig. 30 and Fig. 32. As shown in Fig. 30, the conventional DTC has higher dc-link voltage offset between the capacitors and has higher torque and stator current ripples compared to the proposed method in Fig. 32. And the dc-link voltages are balanced with the VSV based DTC as well.

Acceleration and speed reversal of the motor experiments were also performed to validate the performance of the proposed DTC method. Fig. 33 shows the acceleration of the motor from 500 RPM to 1500 RPM using conventional DTC. The dc-link voltages are measured and considered for selecting the appropriate voltage vector in the conventional DTC method, therefore the V_{c1} and V_{c2} are balanced. However, when the reverse speed is applied, i.e., from 500 RPM to -1000 RPM, the conventional DTC cannot maintain balanced dc-link which is shown in Fig. 34. On the other hand, in both acceleration and speed reversal mode the proposed DTC can maintain balanced dc-link voltages with less torque and current ripples, which are validated in Fig. 35 and Fig. 36, respectively.

Fig. 37 shows the steady state torque comparison between the conventional and proposed DTC when the command torque is 0.4 Nm. From the figure, it is clear that the proposed advanced DTC has more than 20% less torque ripple than the conventional DTC when the speed is maintained at 1500 RPM. Flux ripples also reduced to 3.4% using the proposed DTC, which is 6% less the conventional DTC. The flux ripple comparison is shown in Fig. 38. Fig. 39 represents the THD (%) of the stator current from the experimentally measured current. The conventional DTC has higher stator current THD (%) than the proposed DTC

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as shown in the Fig. 39. Both simulation and experimental results validate the proposed enhanced DTC with of IPM machine.

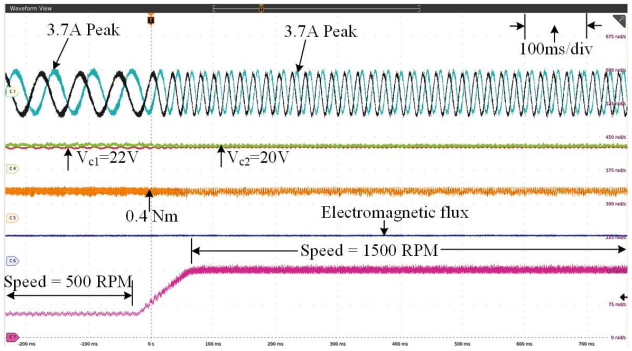

Fig. 35. Acceleration of the motor with proposed DTC.

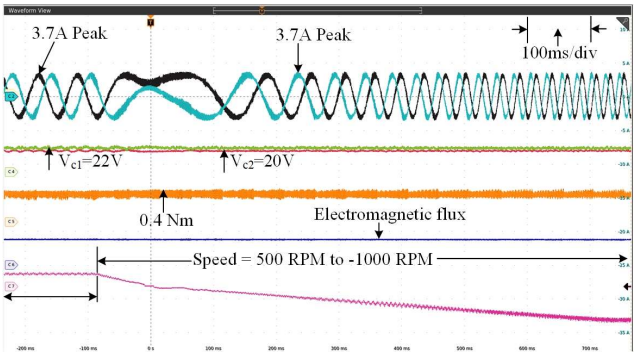

Fig. 36. Speed reversal of the motor with proposed DTC.

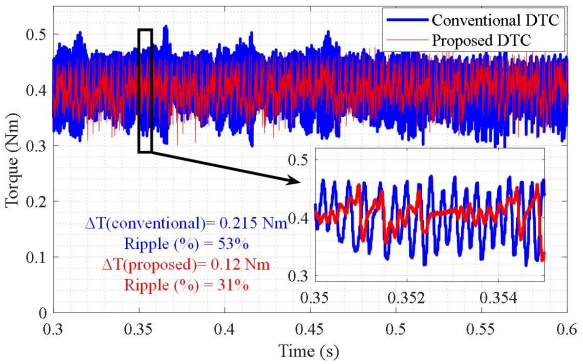

Fig. 37. Steady state torque comparison between conventional and proposed DTC.

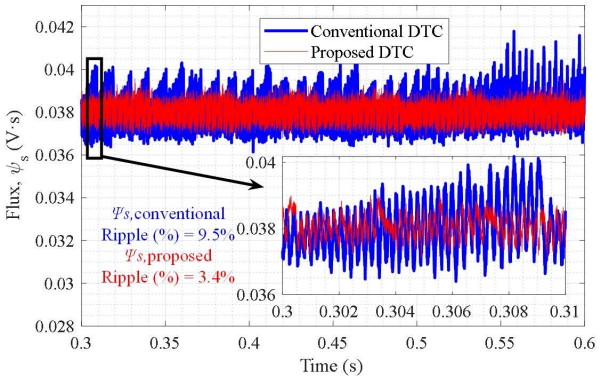

Fig. 38. Flux ripple comparison for both control method.

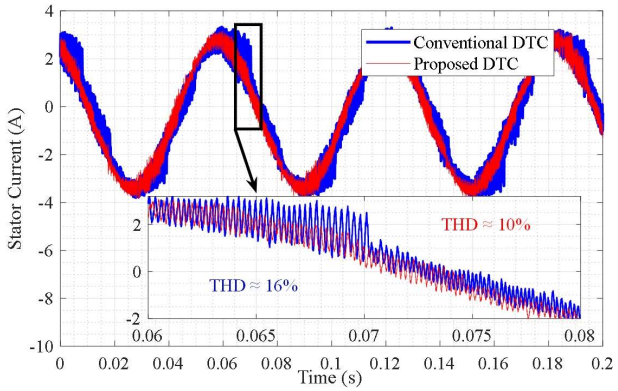

Fig. 39. Stator current THD (%) for both conventional and proposed DTC at 0.4 Nm torque

V. CONCLUSION

In this paper, an enhanced DTC scheme was proposed for 3-L T-type converter with inherent dc link voltage balancing capability. Due to the use additional VSVs, compared with the conventional DTC, the proposed DTC can effectively reduce the torque ripples as well as the stator current harmonics. Moreover, detailed loss analysis was performed to quantify the loss increase due to the use of the proposed method, which however only leads to very minimum efficiency decrease due to the use of SiC MOSFETs. Both simulation and experimental results have been presented to validate the feasibility and effectiveness of proposed method.

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