A Generic Multi-Vector Model Predictive Control With Symmetric Pulse Pattern for Hybrid Multilevel Converters

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***Abstract*—This article presents a generic multi-vector model predictive control (MV-MPC) method that has the potential to be applied to all hybrid multilevel converters (HMCs). It firstly locates the reference voltage vector in the 120° oblique coordinate to select the three adjacent voltage vectors to be applied over one control cycle. Then, the current tracking is guaranteed through duty cycle optimization and dc capacitor voltages are balanced by evaluating possible switching sequences that belong to the voltage vectors with optimal duty cycles. At last, the optimal switching sequence with a symmetric five- or seven-segment pulse pattern is generated using an external modulator. The proposed generic MV-MPC can significantly improve the quality of the output current, while achieving a constant equivalent switching frequency at the same time. Experimental studies on an all silicon carbide HMC prototype, i.e., an active neutral point clamped converter with cascaded H-bridge, are presented to validate the effectiveness of the proposed MV-MPC strategy.**

***Index Terms*—Hybrid multilevel converter (HMC), model predictive control (MPC), optimal duty cycle.**

I. Introduction

HYBRID multilevel converters (HMCs), i.e., a combination of one or more types of power electronic building blocks (PEBBs) [1]-[9], have been extensively employed in various industrial applications over the past few decades, especially in the high power medium voltage (MV) applications [3]-[5]. Generally speaking, the HMC topology requires the use of floating dc capacitors [1], which can significantly impact the controller design in one way or another. Therefore, enhanced control methods to improve the output current quality while regulating the dc capacitor voltages are desired.

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To control HMCs, existing literatures predominantly focus on the use of multi-carrier pulse-width modulation (MC-PWM) [4], [9]-[11] or the space vector modulation (SVM) [6], [8]. However, these modulation methods have several inherent shortcomings. For instance, the dc voltage utilization of the MC-PWM is much lower compared with the SVM. Although the zero-sequence injection approach can be applied to increase the dc voltage utilization, the calculation process of which is very complex especially for multilevel converters [12]. The SVM, when considering the enormous computational burden for multilevel converters, is even more difficult to implement. In addition to the design of the modulation schemes, the control algorithm design is also a challenging task. For the HMCs, in addition to ensure a high-performance current tracking, the neutral-point voltage or floating dc capacitor voltage balancing is always needed. Therefore, additional proportional-integral (PI) or proportional-resonant (PR) controller are required to achieve the multiple control objectives simultaneously [6], [8]. Nevertheless, the co-existence of multiple control loops results in intricate controller parameters tuning. The cross-coupling among control loops may also lead to poor performance.

The model predictive control (MPC), which is a promising alternative to control power electronic converters [13]-[18], has been adopted for almost all power electronic applications [18] over the past few years. Due to its distinct advantages, such as fast dynamic response, straightforward implementation, compatibility with nonlinear constraints, and the capability to simultaneously tackle multiple control objectives [16], MPC is much more powerful to address the challenge of regulating the dc capacitor voltage in an HMC, compared with traditional linear modulation schemes [19], [20]. However, regarding the control of HMCs, there are two major issues associated with the inherent characteristics of the conventional MPC (C-MPC). First, the need to evaluate a tremendous number of switching states makes it computationally impractical. Second, applying only one voltage vector over the entire control cycle leads to increased current ripples and variable equivalent switching frequency, which may vary with the sampling frequency and reference current [16].

A variety of studies have been proposed to address these issues. For instance, a dc capacitor voltage sorting MPC for the modular multilevel converter (MMC) is reported in [21], which significantly improves the computational efficiency. To improve the operation efficiency, a modified MPC is proposed in [22] to replace the time-consuming optimization algorithm

by Diophantine equations. In addition to the studies on computational burden reduction, there are also publications on the improvement of steady-state performance. In [23], a modulated MPC for MMC is proposed, which applies multiple vectors that are formed in the current increment plane over one control cycle, to reduce the total harmonic distortion (THD) of the output current. In [24], a long-horizon MPC is proposed to reduce the output current THD, but encounters exponential increase of computational burden along the increase of the prediction horizon. The authors thereby present a modified sphere decoding algorithm to solve this issue, which greatly improves the computational efficiency. In addition, the MPC combined with the discrete space vector modulation approach is introduced to improve the steady-state performance in [25]-[27], which uses equally subdivided time intervals within one control period. Although the current tracking performance is significantly improved due to the large number of virtual space vectors that are possible for the optimal voltage vector evaluation, the evaluation needs a tremendous amount of computational resource, making it difficult to implement in a real-world control platform. To solve this issue, only three candidate voltage vectors are considered for cost function evaluation in [25]. Similarly, in [26], the proposed approach selects the optimal region including the reference voltage vector in the space vector diagram and only voltage vectors that locate in the optimal region are used in the cost function calculation. In [27], the proposed MPC reduces the number of admissible voltage vectors from 37 to 13 by using a pre-selection approach based on geometrical analysis of virtual vectors. However, it is noteworthy that due to the equal subdivision of the control cycle, the switching pulse pattern is asymmetric, which may lead to more switching actions and less competitive current tracking performance.

To achieve constant equivalent switching frequency while improving the current tracking at the same time, an optimal switching sequence MPC, which selects an optimal set of voltage vectors stored in a lookup table as precalculated sequences, is presented in [28]. However, as the voltage level increases, a huge lookup table should be developed. The multi-vector MPC (MV-MPC) [29], [30], or the three-vector MPC [31], [32], is a promising candidate for achieving both good current tracking and constant switching frequency. In [30], a MV-MPC is proposed for three-phase rectifiers, which achieves constant switching frequency and lower current THD. In [31], a three- vector MPC for motor drive is reported, which has a symmetric switching pulse pattern and also reveals superior current tracking to the C-MPC. However, these existing MV-MPC approaches are not directly applicable to the HMCs. For one thing, the tremendous number of voltage vectors in an HMC makes the selection of the adjacent vectors far more complicated, which cannot be conducted through existing calculation or lookup table approaches [32] due to their heavy computational burden. For another, to achieve equivalent constant switching frequency by symmetric switching sequence, specific switching sequence shaping approach should be meticulously designed for the HMCs, which is entirely different from two-level or three-level converters. To the best of the authors' knowledge, there is still no MV-MPC strategy for HMCs being reported in existing literatures so far.

To this end, this article presents a generic MV- MPC solution that can be applied to any HMCs. It firstly locates the reference vector in the 120° oblique coordinate and selects the three adjacent voltage vectors over one control (sampling) cycle, which converts the computationally inefficient calculation or lookup table approaches [32] to simple integer arithmetic. The current tracking is prioritized through duty cycle optimization of the selected adjacent vectors, and through evaluation of all possible switching sequences that belong to the voltage vectors with optimal duty cycles, dc capacitor voltage balancing is simultaneously achieved without impacting the current tracking. Then, the optimal switching sequence is generated through an external modulator and follows the symmetric pulse pattern of either five- or seven-segment, which are referred to as MV-MPC-I and MV-MPC-II respectively. In a nutshell, the proposed generic MV-MPC is applicable for any HMCs and significantly reduces both the calculation burden and output current ripple while achieving constant equivalent switching frequency at the same time. A typical HMC, which consists of an active-neutral-point- converter (ANPC) stage and H-bridge converter stage, or can be referred to as the ANPC-H converter [1], is used as a case study for the proposed MV-MPC. The experimental results on an all silicon carbide (SiC) ANPC-H prototype are presented to validate the effectiveness of the proposed control strategy.

II. Circuit Analysis and Modeling

The configuration of ANPC-H converter with RL-load is illustrated in Fig. 1, where R and L are the resistance and inductance of the RL-load, u_{dc_1}, u_{dc_2}, u_{dc_a1}, u_{dc_b1}, and u_{dc_c1} are the capacitor voltages of ANPC and H-bridge respectively, i_{dc_1}, i_{dc_2} are the currents of the dc-link capacitors, i_{oa}, i_{ob}, and i_{oc} are the three-phase neutral currents, i_a, i_b, and i_c are the phase currents, U_{dc} is the external dc-source voltage. If the dc voltages are regulated as: $u_{dc\_1} = u_{dc\_2} = U_{dc}/2$, $u_{dc\_a1} = u_{dc\_b1} = u_{dc\_c1} = U_{dc}/4$, the converter output voltage comprises seven voltage levels. Table I shows all the switching states, where S_j are the switching states of phase j, S_{jn} are the switching functions of the power switches M_{jn}, where $j \in \{a, b, c\}$, $n \in \{1, 2, \ldots, 10\}$, and $S_{jn} \in \{0, 1\}$. Specifically, the "O+" or "O−" state of the ANPC stage is adopted when its switching state is shifting from zero to positive state or from negative to zero state, respectively; the "O+" or "O−" state of the H-bridge stage is adopted when its switching state is shifting from non-zero to zero state or from zero to non-zero state, respectively. This can not only guarantee more evenly distributed power loss between M_{j1} and M_{j2} [20], but is also beneficial to the modulation, which will be discussed in Section III. The operation limitation of this kind of topology is thoroughly investigated in [6], and thus, will not be discussed in this paper. The working point chosen for the experiments in this article is within this limitation.

The mathematical model in $\alpha\beta$-coordinate can be given by

$$\boldsymbol{u} = L\frac{d\boldsymbol{i}}{dt} + \boldsymbol{i}R \tag{1}$$

where $\boldsymbol{u} = [u_\alpha\ u_\beta]^{\mathrm{T}}$ and $\boldsymbol{i} = [i_\alpha\ i_\beta]^{\mathrm{T}}$, which are converter voltage and current vectors in $\alpha\beta$-coordinate respectively. Defining the switching states of the ANPC stage and H-bridge stage as S_{jA} and S_{jH}, then S_{jA} and $S_{jH} \in \{-1, 0, 1\}$.

The models of the dc capacitors can be given by

$$i_o = C\frac{d\Delta u_{dc}}{dt} \tag{2}$$

$$S_{jH} i_j = C_1 \frac{du_{dc\_j1}}{dt} \tag{3}$$

where $\Delta u_{dc} = u_{dc\_1} - u_{dc\_2}$, i_j are the phase currents, and i_o is the neutral point current, which can be given by

$$i_o = \sum_{j=a,b,c} \left(1 - \left|S_{jA}\right|\right) i_j \,. \tag{4}$$

Then the discrete-time model can be obtained by applying Euler Forward Approximation to (1), (2)-(4) as

$$\boldsymbol{i}(k+1) = \frac{T_s}{L}\boldsymbol{u}(k) + \left(1 - \frac{RT_s}{L}\right)\boldsymbol{i}(k) \tag{5}$$

$$u_{dc\_j1}(k+1) = \frac{T_s}{C_1}\bar{i}_j(k) + u_{dc\_j1}(k) \tag{6}$$

$$\Delta u_{dc}(k+1) = \frac{T_s}{C}\bar{i}_o(k) + \Delta u_{dc}(k) \tag{7}$$

where T_s is the sampling period (or control cycle), $\bar{i}_j(k)$ and $\bar{i}_o(k)$ are the average current that runs through H-bridge capacitor and average neutral point current over one control cycle at time instant k. When multiple vectors are selected for optimal current tracking, $\bar{i}_j(k)$ and $\bar{i}_o(k)$ can be readily calculated by using the switching states of the selected vectors and their corresponding dwell times.

TABLE I
SWITCHING STATES OF THE ANPC-H CONVERTER

Switching States S_j	S_{jA}	S_{jH}	ANPC			H-Bridge	
			S_{j1}	S_{j2}	S_{j4}	S_{j7}	S_{j9}
6 ($3U_{dc}$/4)	1 (P)	−1 (N)	1	1	0	0	1
5 (U_{dc}/2)	1 (P)	0 (O+)	1	1	0	1	1
	1 (P)	0 (O−)	1	1	0	0	0
4 (U_{dc}/4)	1 (P)	1 (P)	1	1	0	1	0
	0 (O+)	−1 (N)	1	0	0	0	1
	0 (O−)	−1 (N)	0	1	1	0	1
3 (0)	0 (O+)	0 (O+)	1	0	0	1	1
	0 (O+)	0 (O−)	1	0	0	0	0
	0 (O−)	0 (O+)	0	1	1	1	1
	0 (O−)	0 (O−)	0	1	1	0	0
2 (−U_{dc}/4)	0 (O+)	1 (P)	1	0	0	1	0
	0 (O−)	1 (P)	0	1	1	1	0
	−1 (N)	−1 (N)	0	0	1	0	1
1 (−U_{dc}/2)	−1 (N)	0 (O+)	0	0	1	1	1
	−1 (N)	0 (O−)	0	0	1	0	0
0 (−$3U_{dc}$/4)	−1 (N)	1 (P)	0	0	1	1	0

III. MULTI-VECTOR MODEL PREDICTIVE CONTROL

A. Adjacent Voltage Vector Selection

Fig. 2 illustrates the overall architecture of the proposed MV-MPC strategy. When one switching state is applied over each control cycle, the MPC is inherently equivalent to the deadbeat control [25], in which the calculated reference voltage can be adopted to select the adjacent voltage vectors. This reference voltage vector can be given by

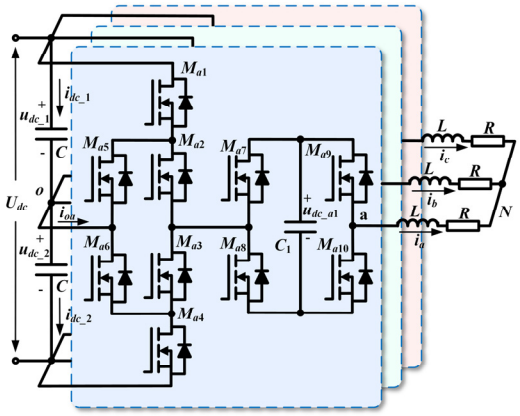


Fig. 1. Topology of the ANPC-H Converter with RL-Load.

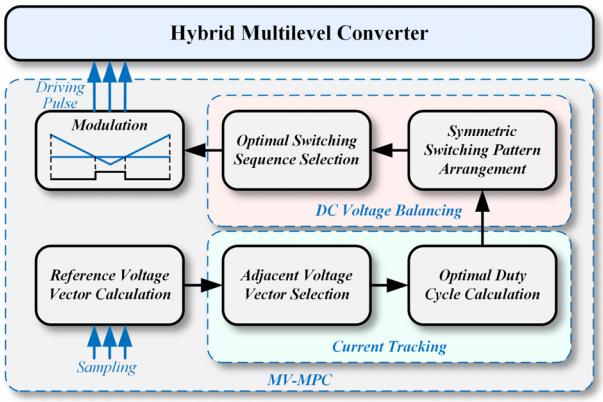


Fig. 2. The proposed MV-MPC architecture.

$$\boldsymbol{u}^*(k) = \frac{L}{T_s}\left[\boldsymbol{i}^*(k+1) - \boldsymbol{i}(k)\right] + \boldsymbol{i}(k)R \tag{8}$$

where $\boldsymbol{i}^*(k+1)$ can be obtained by Lagrange Extrapolation [18].

Fig. 3 demonstrates the space vector diagram along with the reference vector. Due to symmetry of the space vector diagram, the selection process can be equivalently performed in Sector 1 by rotating the reference vectors clockwise by multiples of π/3, the equivalent counterpart in Sector 1 can be defined as $\boldsymbol{u}_1^*(k) = [V_{\alpha 1}\ V_{\beta 1}]^{\mathrm{T}}$. When the reference vector is beyond the hexagon, it is proportionally scaled down to the inscribed circle of the entire hexagon [32]. Then, to facilitate the selection process, the $\alpha\beta$-coordinate is converted to the 120° gh-coordinate [34] by the following transformation equation:

$$\begin{bmatrix} V_{g1} \\ V_{h1} \end{bmatrix} = \begin{bmatrix} 1 & 1/\sqrt{3} \\ 0 & 2/\sqrt{3} \end{bmatrix} \begin{bmatrix} V_{\alpha 1} \\ V_{\beta 1} \end{bmatrix} \tag{9}$$

where $[V_{g1}\ V_{h1}]^{\mathrm{T}}$ stands for the reference vector in the 120° gh-coordinate. Fig. 4 shows all the switching states of Sector 1 in the 120° gh-coordinate. Defining the first switching state as the basic switching state (BSS), then the relationship of BSSs in each sector is presented in Table II, where $[S_{a1}\ S_{b1}\ S_{c1}]$ is the BSS in Sector 1.

The selection process of the three adjacent voltage vectors is depicted in Fig. 4. The first vector $\boldsymbol{V}_1$ in 120° gh-coordinate can be calculated by rounding down function as

$$[g_0 \quad h_0]^{\mathrm{T}} = \left[\lfloor V_{g1} \rfloor \quad \lfloor V_{h1} \rfloor\right]^{\mathrm{T}} \tag{10}$$

Then the BSS of $\boldsymbol{V}_1$ can be given by [g_0 h_0 0]. As it can be seen from Fig. 4(b), the reference voltage vector possibly locates in either triangle A or B, which can be determined by the following criterion:

$$\boldsymbol{u}_1^*(k) \in \begin{cases} \text{A}, & V_{g1} - V_{h1} \le g_0 - h_0 \\ \text{B}, & V_{g1} - V_{h1} > g_0 - h_0 \end{cases}. \tag{11}$$

The vertices of the triangles are three vectors: $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, and $\boldsymbol{V}_3$, which are the three adjacent vectors. Their BSSs can be easily obtained by integer arithmetic based on [g_0 h_0]$^{\mathrm{T}}$. In this way, the selection of the adjacent vectors is dramatically simplified and the computational burden is also significantly reduced.

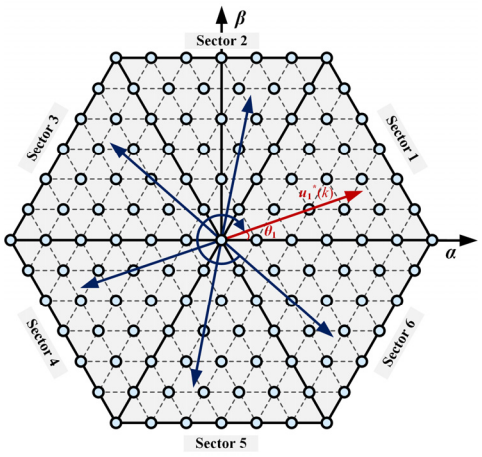
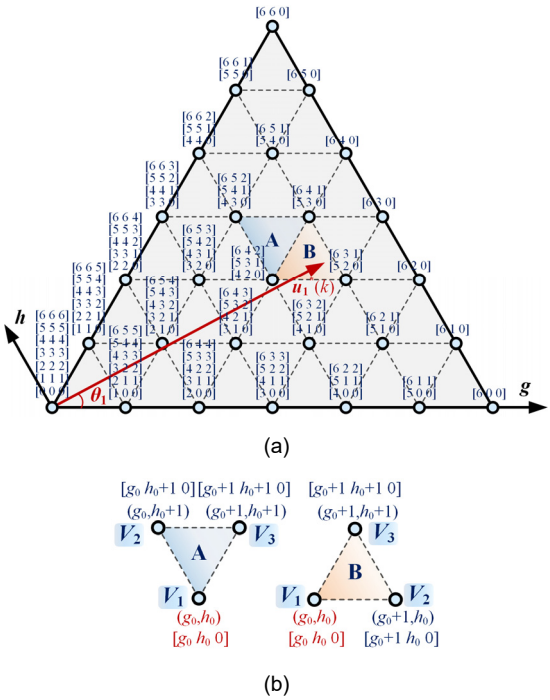


Fig. 3. Reference vector rotation in $\alpha\beta$-coordinate.



(a)

(b)

Fig. 4. Selection process of the adjacent voltage vectors. (a) Switching states in Sector 1. (b) Two types of switching triangles.

B. Optimal Duty Cycle Calculation

The optimal duty cycle is obtained through the current tracking error minimization. The slopes of the selected three voltage vectors can be given by

$$\boldsymbol{s}_i = \frac{1}{L}(\boldsymbol{V}_i - \boldsymbol{i}R) \tag{12}$$

where $i \in \{1, 2, 3\}$, and $\boldsymbol{s}_i = [s_{\alpha i}\ s_{\beta i}]^{\mathrm{T}}$. The predicted current at the end of each control cycle can be given by

$$\begin{cases} i_\alpha(k+1) = i_\alpha(k) + s_{\alpha1}t_1 + s_{\alpha2}t_2 + s_{\alpha3}t_3 \\ i_\beta(k+1) = i_\beta(k) + s_{\beta1}t_1 + s_{\beta2}t_2 + s_{\beta3}t_3 \end{cases}. \tag{13}$$

Then the error can be expressed as

$$\begin{cases} \Delta_\alpha = I_\alpha - s_{\alpha1}t_1 - s_{\alpha2}t_2 - s_{\alpha3}(T_s - t_1 - t_2) \\ \Delta_\beta = I_\beta - s_{\beta1}t_1 - s_{\beta2}t_2 - s_{\beta3}(T_s - t_1 - t_2) \end{cases} \tag{14}$$

where $I_\alpha = i_\alpha^*(k{+}1){-}i_\alpha(k)$ and $I_\beta = i_\beta^*(k{+}1){-}i_\beta(k)$. Therefore, the cost function of current tracking can be given by

$$J = \Delta_\alpha^{\,2} + \Delta_\beta^{\,2}. \tag{15}$$

To achieve the minimum current tracking error, the least square method is used to calculate the optimal duty cycle. The optimal values of t_1 and t_2 should satisfy the extremum value conditions

$$\frac{\partial J}{\partial t_1} = 0\,;\frac{\partial J}{\partial t_2} = 0\,. \tag{16}$$

The optimal duty cycles can be obtained by solving (16) as

$$d_1 = \frac{I_\alpha(s_{\beta3} - s_{\beta2}) + I_\beta(s_{\alpha2} - s_{\alpha3}) + T_s(s_{\alpha3}s_{\beta2} - s_{\alpha2}s_{\beta3})}{T_s s_{\beta1}(s_{\alpha2} - s_{\alpha3}) + T_s s_{\beta2}(s_{\alpha3} - s_{\alpha1}) + T_s s_{\beta3}(s_{\alpha1} - s_{\alpha2})} \tag{17}$$

$$d_2 = \frac{I_\alpha(s_{\beta1} - s_{\beta3}) + I_\beta(s_{\alpha3} - s_{\alpha1}) + T_s(s_{\alpha1}s_{\beta3} - s_{\alpha3}s_{\beta1})}{T_s s_{\beta1}(s_{\alpha2} - s_{\alpha3}) + T_s s_{\beta2}(s_{\alpha3} - s_{\alpha1}) + T_s s_{\beta3}(s_{\alpha1} - s_{\alpha2})} \tag{18}$$

$$d_3 = 1 - d_1 - d_2 \tag{19}$$

where $d_i = t_i/T_s$.

C. Optimal Switching Sequence Determination

After the optimal duty cycles and adjacent voltage vectors are selected, the switching sequence should be ingeniously arranged as per specific rules. Fig. 5 shows the space vector diagram and the switching states of the voltage vectors in selected triangles, where the BSSs are marked as red. To generate a symmetric switching sequence, the following rules should be complied with: 1) only one step of voltage level shifting is allowed over each switching period; 2) voltage level should resume to the initial state at the end of each switching period to reduce switching actions. Therefore, the switching sequences for the MV-MPC-I and MV-MPC-II, which follow the five- or seven-segment pulse pattern, can be restricted to a finite set as demonstrated in Figs. 6 and 7. As it can be seen, there are in total three or four switching states being applied to the MV-MPC-I or MV-MPC-II over each switching period, which are equally distributed around the center of the each switching cycle to form a symmetric pulse pattern.

To be specific, the switching sequences in Sectors 1, 3, and 5 have inverse direction to the ones in Sectors 2, 4, and 6, i.e., either clockwise or counter-clockwise. The six sectors are marked with various colors from dark to light in Figs. 6 and 7. Except for the switching sequences that are comprised of BSSs, the redundant switching sequences are obtained by integer step-increment of the BSSs. Moreover, there are six types of symmetric pulse pattern in total, as illustrated in Figs. 6 and 7.

To better explain the formation process of the candidate switching sequences, the scenario when reference vector locates in Sector 1 and type A triangle is taken as an example. The switching sequences starting from vectors $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, and $\boldsymbol{V}_3$ represent the three types of pulse pattern respectively, which have the same impact on current tracking but different impact on dc capacitor charging or discharging, thus, should be evaluated to balance the dc voltages. Similarly, when the reference vector locates in other sectors and other type of triangle, the candidate switching sequences can be enumerated as well based on this criterion. Therefore, all the switching sequences that form symmetric pulse pattern can be found in a way that leverages the symmetry of the space vector diagram, and thus, the time-consuming lookup table approach [32] can be abandoned. The total numbers of the redundant switching sequences with the initial vector of $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, and $\boldsymbol{V}_3$ can be expressed as follows:

for MV-MPC-I,

$$\begin{cases} m_1 = m_2 = m_3 = N-1-g_0; & u_1^*(k) \in \text{A} \\ m_1 = m_2 = N-1-g_0, m_3 = N-2-g_0; & u_1^*(k) \in \text{B} \end{cases} \tag{20}$$

for MV-MPC-II,

$$\begin{cases} m_1 = m_2 = N-1-g_0, m_3 = N-2-g_0; & u_1^*(k) \in \text{A} \\ m_1 = N-1-g_0, m_2 = m_3 = N-2-g_0; & u_1^*(k) \in \text{B} \end{cases} \tag{21}$$

where N is the total phase voltage level of the converter.

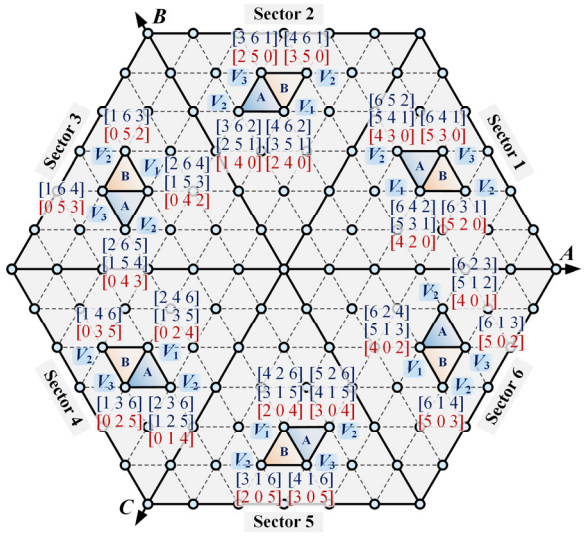


Fig. 5. Space vector diagram and switching sates in six sectors.

To get the optimal switching sequence, the balancing of the dc capacitor voltages can be used as the constraint condition of the optimization problem, which minimizes the error between the desired dc voltages and the predicted ones. Therefore, the cost function of this objective can be given by

$$J = \sum_{j=a,b,c} J_j + J_{dc} \tag{22}$$

where

$$J_j = \left\| u_{dc\_j1}(k+1) - U_{dc}/4 \right\|_2^2 \tag{23}$$

$$J_{dc} = \left\| \Delta u_{dc}(k+1) \right\|_2^2 . \tag{24}$$

It is noteworthy that the MV-MPC-I and MV-MPC-II are approximately equivalent to each other when it comes to dc capacitor voltage balancing. According to (20) and (21), MV-MPC-I has one more redundant switching sequence than the MV-MPC-II does. Nevertheless, this extra five-segment switching sequence is actually incorporated in one particular seven-segment switching sequence, the only difference is that the dwell time of the initial or terminal switching state in the seven-segment sequence is half of that in the five-segment sequence. This trivial difference, over one switching cycle, barely has any impact on the dc capacitor voltage.

The predicted average current can be calculated by

$$\begin{cases} \overline{i_j} = \sum_{i=1}^{k} D_i S_{jH\_i} i_j \\ \overline{i_o} = \sum_{i=1}^{k} D_i \sum_{j=a,b,c} \left(1 - \left|S_{jA\_i}\right|\right) i_j \end{cases} \tag{25}$$

where k equals to 3 or 4, which refers to the number of the switching states in five- or seven-segment switching pattern, respectively. And D_i is the duty cycle of the ith switching state in the selected optimal switching sequence. Therefore, in the MV-MPC-I, k=3 and D_i= d_i, while in the MV-MPC-II, k=4, D_1 = $d_1/2$, D_2 = d_2, D_3 = d_3, and D_4 = $d_1/2$. S_{jH_i} and S_{jA_i} are the switching states of the ANPC stage and H-bridge stage in the ith switching sequence. Then the predicted variables can be calculated by substituting (25) into (6) and (7).

Therefore, the constraint optimization problem for selecting optimal switching sequence can be described as follows:

$$\begin{cases} \min\limits_{S_{jA\_i}, S_{jH\_i}} & J \\ s.t. & \text{equations (6), (7), (17)-(19), and (25)} \\ & S_{jA\_i}, S_{jH\_i} \in \{-1, 0, 1\} \\ & \sum_{i=1}^{k} D_i = 1 \end{cases} . \tag{26}$$

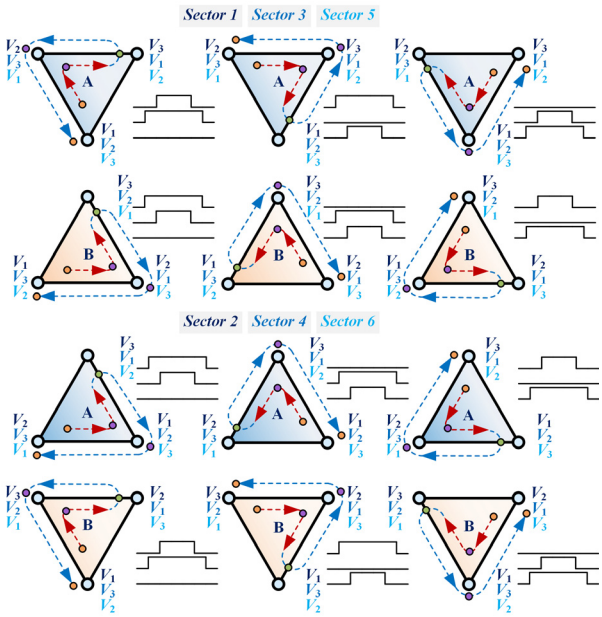


Fig. 6. Switching sequences of the MV-MPC I.

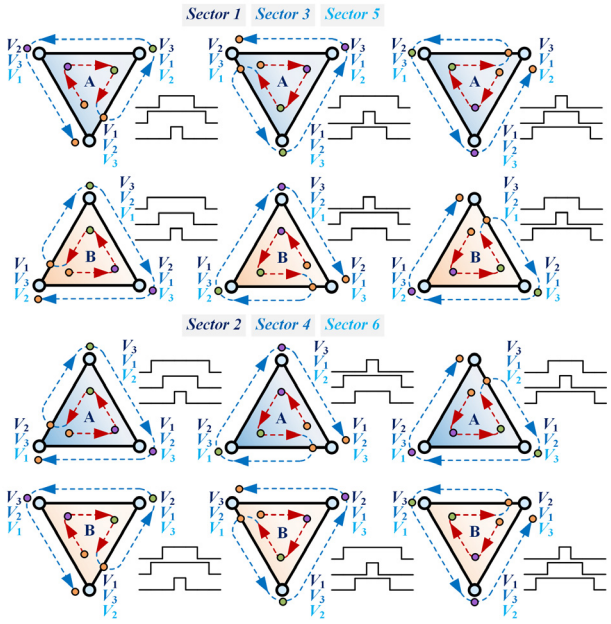


Fig. 7. Switching sequences of the MV-MPC II.

where $j \in \{a, b, c\}$, $i \in \{1, \ldots, k\}$, $k \in \{3, 4\}$. To better present the selection process of the optimal switching state, a flowchart of the evaluation loop is given in Fig. 8, where J_{min} is the minimum cost function value.

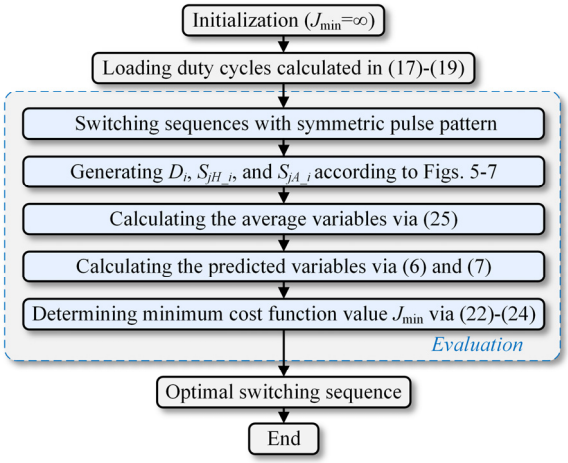


Fig. 8. Flowchart of the optimal switching sequence selection process.

D. Delay Compensation

As it is widely known, a one-step delay always exists in a digital controller due to the process of sampling and algorithm execution [16]. This delay effect can severely jeopardize the performance of MPC especially when the multiple vectors are applied over one control period. The two-step prediction should always be implemented to eradicate the adverse effect [17]. In addition to the current tracking compensation, the dc voltage balancing should also be compensated by the two-step prediction. The dc voltage fluctuations can thereby be reduced because of the compensation.

E. Modulation

As aforementioned in Section II, the alternation of the switching state should always guarantee that the switching functions of the switches, with the switch number of 1, 2, 4, 7, and 9, always change from 0 to 1 in the first half cycle of the selected switching sequence. Accordingly, the modulation can be conducted as follows: 1) calculating the duty cycles of switches M_{j1} to M_{j10}; 2) comparing the duty cycles with a couple of synchronized carriers to generate the driving pulses of each switch. The duty cycles can be calculated by

$$d_{jx} = \sum_{i=1}^{k} D_i S_{jx\_i} \tag{27}$$

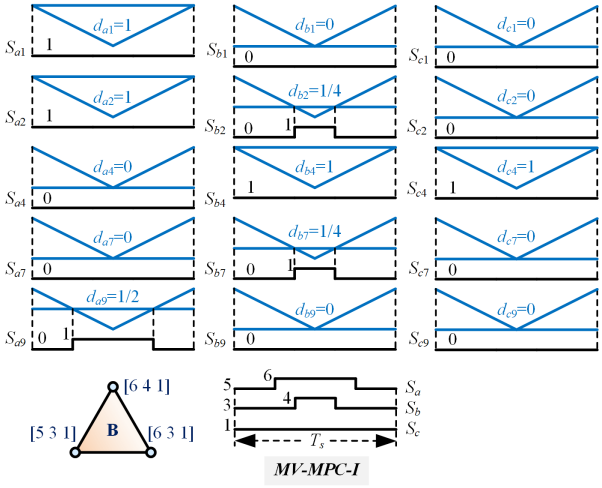


Fig. 9. Modulation process of MV-MPC-I.

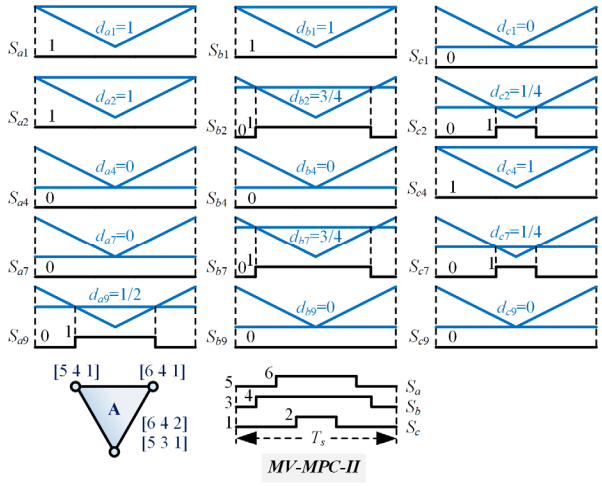


Fig. 10. Modulation process of MV-MPC-II.

where $x \in \{1, 2, 4, 7, 9\}$, $j \in \{a, b, c\}$, d_{jx} is the duty cycle of the switches, S_{jx_i} is the ith switching function of M_{jx}, which can be derived from the ith switching state in the selected optimal switching sequence. Due to the complementary relationship of the power switches, the driving pulses of the other switches can be easily generated in real-time. Fig. 9 gives the modulation process of one specific case in Fig. 5 when MV-MPC-I is adopted. The five-segment pulse sequence, [5 3 1]-[6 3 1]-[6 4 1]-[6 3 1]-[5 3 1], is selected (D_1 = 1/2, D_2 = 1/4, D_3 = 1/4). Therefore, the duty cycles, i.e., d_{jx}, of each switch can be calculated via (28), which are then applied to the modulator. As depicted in Fig. 9, the final pulse pattern is symmetric over one switching cycle. Similarly, Fig. 10 shows the modulation of

MV-MPC-II, where the seven-segment pulse sequence, [5 3 1]-[5 4 1]-[6 4 1]-[6 4 2]-[6 4 1]-[5 4 1]-[5 3 1], is selected (D_1 = D_2 = D_3 = D_4 = 1/4), which also has a symmetric pattern over one switching period.

IV. Experimental Studies

To validate the proposed control strategy, an all-SiC low-power prototype is developed using discrete SiC MOSFETs (CREE/Wolfspeed: C2M0160120D, 1.2 kV, 18 A, 160 mΩ) [35]. The parameters of the system are given in Table II. Fig. 11 exhibits the experimental rig. The control algorithm is implemented in a dSPACE MicroLabBox, while the gate signals are generated using an Intel Max-10 FPGA. The optic fibers are used to transfer gating signals which can enhance the noise immunity.

Fig. 12 demonstrates the average switching frequency comparison among the C-MPC and proposed MV-MPC at various sampling frequencies, where the average switching frequency is calculated based on the actual switching instants of each power switch using a moving averaging tool in MATLAB/Simulink. Since it is difficult to implement the C-MPC due to the massive computational burden, it is replaced by a modified C-MPC, which only evaluates the switching states of the three vectors that encircle the reference voltage vector [25]. As it can be seen, the average switching frequency of the proposed MV-MPC method at the sampling frequency of 10 kHz is approximately similar to that of the C-MPC at the sampling frequency of 20 kHz, and the average switching frequency of the MV-MPC-I at 10 kHz sampling frequency is even lower than that of the C-MPC at 20 kHz sampling frequency. Therefore, the proposed MV-MPV at 10 kHz sampling frequency can be used as benchmarks for comparison with the C-MPC at 20 kHz sampling frequency.

Fig. 13 exhibits the steady-state performance of the C-MPC at 10 and 20 kHz sampling frequency and the proposed control method at 10 kHz sampling frequency. It is obvious to observe that the current ripples of the proposed MV-MPC at 10 kHz sampling frequency are smaller than that of the C-MPC at both 10 and 20 kHz sampling frequencies. The voltages of the dc-link and floating capacitors are all well-regulated under both control strategies. Therefore, it can be concluded that the proposed MV-MPC method is superior to the C-MPC in terms of current tracking at similar average switching frequency.

Fig. 14 presents the transient-state performance of the C-MPC at 10 and 20 kHz sampling frequency and the proposed control method at 10 kHz sampling frequency. As it can be seen, in each case, the dc voltages are well regulated and the dynamic response is fast. The responding time of the C-MPC at 20 kHz sampling frequency is 420 μs, which is slightly shorter than that of the C-MPC at 10 kHz, i.e., 450 μs, due to higher sampling frequency. Regarding the proposed control strategy, both the MV-MPC-I and MV-MPC-II have the same responding time, i.e., 460 μs, which is still very fast. Therefore, it can be concluded that the inherent fast dynamic response characteristic of the C-MPC strategy can be retained in both proposed MV-MPC-I and MV-MPC-II.

Fig. 15 illustrates the current spectrum comparison among the C-MPC at 10 and 20 kHz sampling frequency and the proposed control method at 10 kHz sampling frequency. Since the current THD of the C-MPC at 10 kHz sampling frequency is absolutely worse than that at 20 kHz, it is not included in the figure to make a better and clearer comparison. As it can be seen, the proposed MV-MPC-I and MV-MPC-II have much lower THD than the C-MPC, while the THD of the MV-MPC-II is slightly lower than that of the MV-MPC-I because of the seven-segment pulse pattern. In addition, the spectra of the proposed two methods have a clear harmonic concentration around the sampling frequency and its multiples. These results are consistent with the waveforms in Fig. 13, which proves the superiority of the proposed MV-MPC strategy in terms of the current THD performance.

Fig. 16 gives the comparison of the current THD versus amplitude, which also validate the current ripple reduction effect of the proposed method. As it can be seen, both the proposed MV-MPC-I and MV-MPC-II at 10 kHz sampling frequency have lower current THD at various power volume than the C-MPC at 20 kHz sampling frequency, while the current THD of MV-MPC-II is slightly better than that of the MV-MPC-I. In both cases, the current THD gradually decreases as the current amplitude grows. To highlight the advantage of the proposed MV-MPC strategy in terms of execution time, the turnaround time has been collected in dSPACE real-time mode, as depicted in Fig. 17. As it can be seen, the proposed MV-MPC can enable approximately 40% turnaround time reduction compared with the C-MPC, which verifies another advantage of the proposed MV-MPC method in addition to current THD reduction.

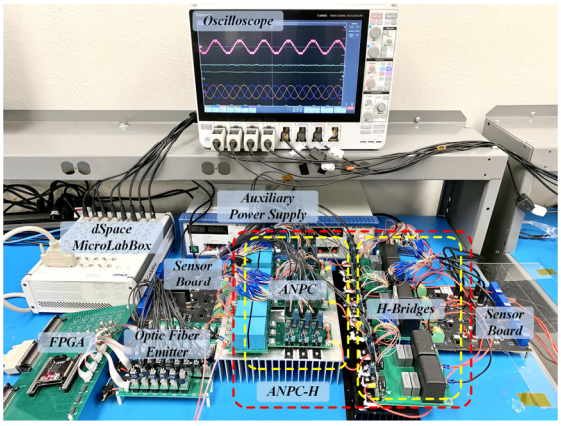


Fig. 11. Experimental rig of the ANPC-H converter.

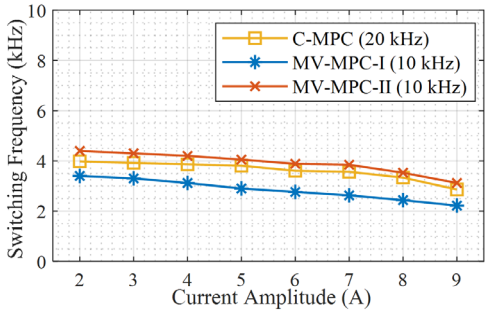


Fig. 12. Average switching frequency comparison.

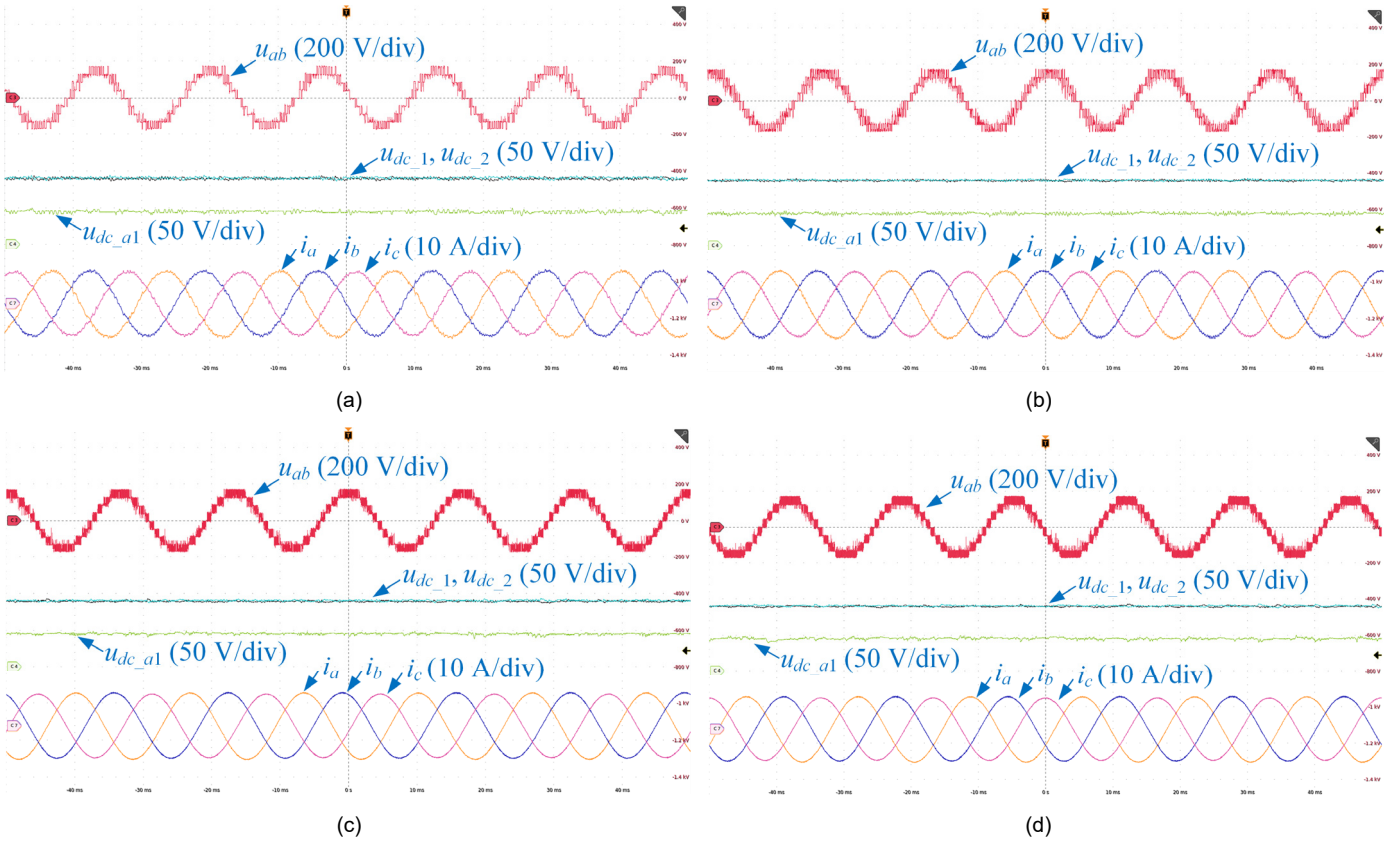


Fig. 13. Experimental waveforms of steady-state at various sampling frequencies. (a) C-MPC with 10 kHz sampling frequency. (b) C-MPC with 20 kHz sampling frequency. (c) MV-MPC-I with 10 kHz sampling frequency. (d) MV-MPC-II with 10 kHz sampling frequency.

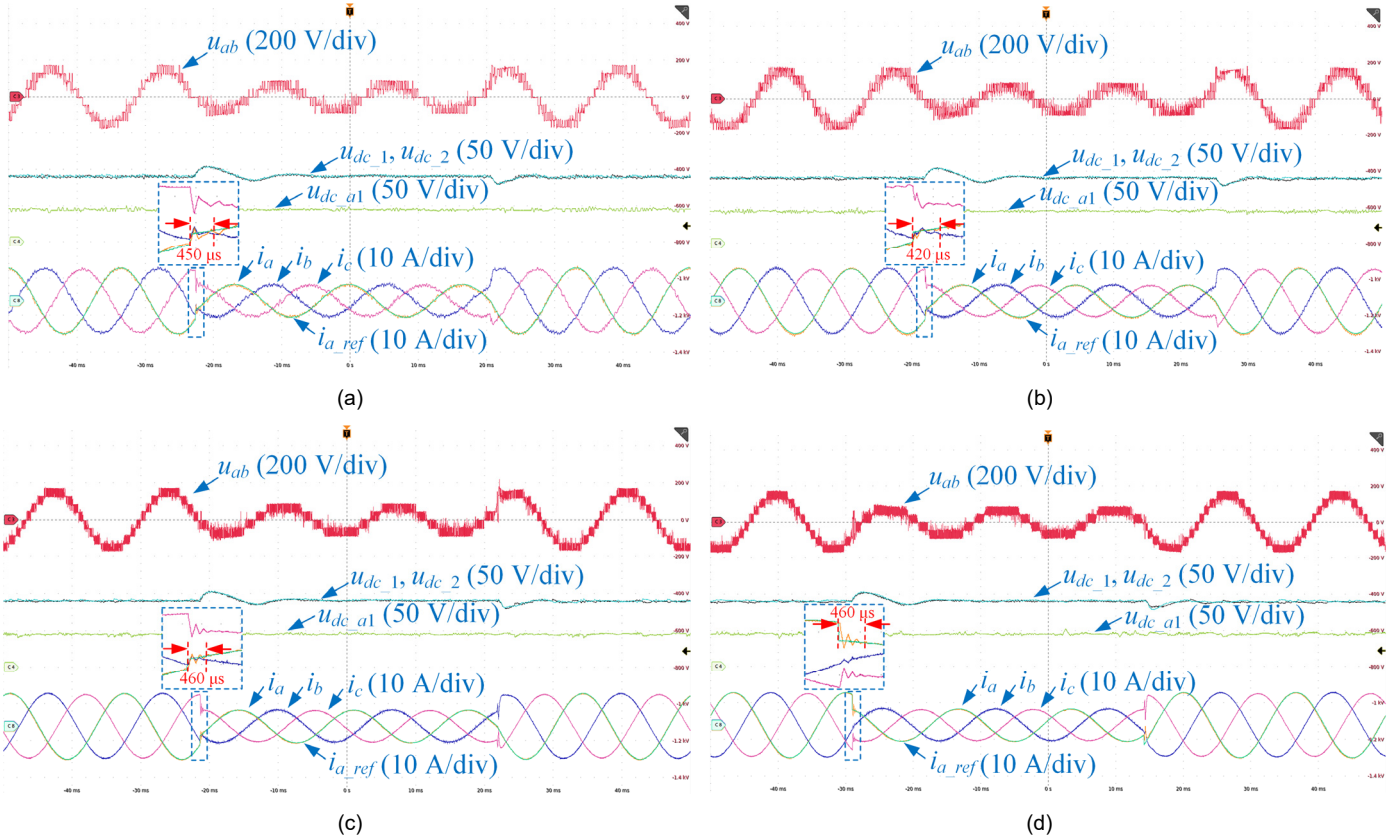


Fig. 14. Experimental waveforms of transient-state at various sampling frequencies. (a) C-MPC with 10 kHz sampling frequency. (b) C-MPC with 20 kHz sampling frequency. (c) MV-MPC-I with 10 kHz sampling frequency. (d) MV-MPC-II with 10 kHz sampling frequency.

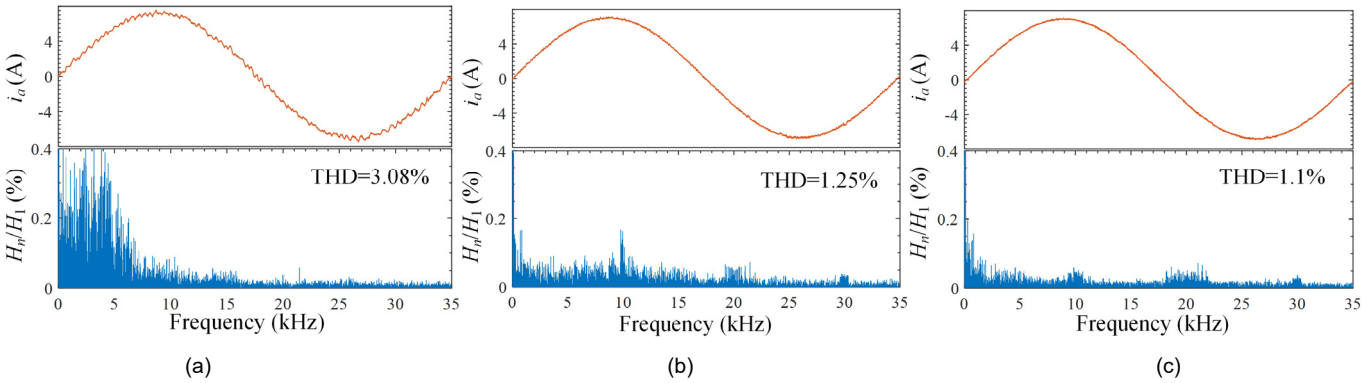


Fig. 15. Current spectrum comparison at various sampling frequency. (a) C-MPC with 20 kHz sampling frequency. (b) MV-MPC-I with 10 kHz sampling frequency. (c) MV-MPC-II with 10 kHz sampling frequency.

TABLE II
SYSTEM PARAMETERS

Variable Description	Symbol	Value
Load inductance	L	4 mH
Load resistance	R	10 Ω
DC-link capacitance	C	240 μF
H-bridge capacitance	C_1	200 μF
DC-link voltage	U_{dc}	180 V
H-bridge dc voltage	$u_{dc\ j1}$	45 V
C-MPC Sampling frequency	f_s	20 kHz
MV-MPC Sampling frequency	f_s	10 kHz
Dead time	T_d	1 μs
Fundamental frequency	f	60 Hz

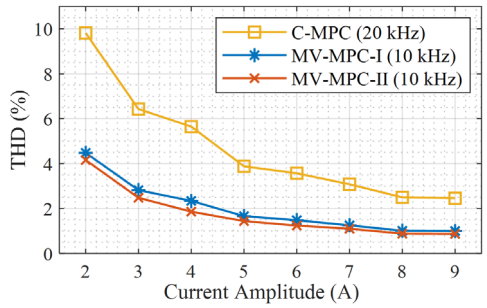


Fig. 16. Current THD comparison.

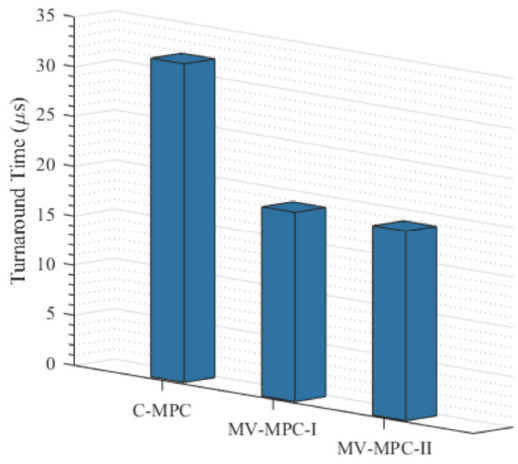


Fig. 17. Turnaround time comparison.

V. CONCLUSION

This article presents a generic MV-MPC strategy for HMCs. It firstly selects the three adjacent voltage vectors over one control cycle by leveraging the integer 120° oblique coordinate system. The current tracking is achieved through a duty cycle optimization approach. Then, the dc capacitor voltage balancing is achieved by evaluating possible switching sequences that belong to the voltage vectors with optimal duty cycles and the optimal switching sequence is generated through an external modulator and follows the symmetric pulse pattern. The steady- and transient-state performances of the proposed method are investigated through experimental tests performed on an all-SiC prototype where the results indicate the following aspects:

1) The proposed generic MV-MPC can significantly reduce both the calculation burden and output current ripple while achieving constant equivalent switching frequency at the same time, and also retains the fast dynamic response characteristic of the conventional MPC.

2) The dc capacitor voltage balancing is independent of the current tacking and thus, has no impact on it.

3) The proposed strategy is very simple and straightforward to implement and is also applicable for an arbitrary HMC.

Therefore, the proposed control method can be considered as a good candidate for high-performance control of the HMCs when fast and accurate current tracking is required.

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