An 800-V High-Density Traction Inverter – Electro-Thermal Characterization and Low-Inductance PCB Bussing Design

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***Abstract*— The need to increase the power density of traction inverters for the electrified transportation systems offers an opportunity to adopt silicon carbide (SiC) devices. To ensure the system reliability, it is critical to select a SiC power module that can dissipate a sufficient amount of power to avoid operating beyond the maximum allowed junction temperature. In this work, a comprehensive electro-thermal characterization procedure based on the virtual junction temperature concept is proposed to characterize the module's maximum power dissipation as a function of coolant temperature. Using the characterization results, it is feasible to determine the module's safe operating area for a traction application in terms of the switching frequency and the coolant temperature. The proposed characterization method is demonstrated on a custom 1200-V SiC module to validate its feasibility for an 800-V, 150-kVA traction inverter system. In addition, the design approach for a low-inductance bussing structure using heavy copper printed circuit board (PCB) is presented in this work, which leads to a snubberless, compact and low-cost system design. Measurements and experimental studies have been performed to validate the effectiveness of PCB bussing design. The overall volume of the inverter system is around 1.75 L, which leads to a volumetric power density of 86 kVA/L.**

***Index Terms*—Optimization, power density, silicon carbide, traction inverter.**

I. Introduction

ELECTRIFICATION is one of the most promising solutions for the future environmental-friendly transportation systems. As an enabling technology, the traction inverter, the power conversion stage between a traction motor and a high-voltage battery or DC link, is critical for the electric vehicles (EV) and hybrid EVs (HEVs) to provide equivalent or better performance than those of comparable internal combustion engine vehicles [1]. It is highly desired that the traction inverters can be compact [2]-[4], cost effective [5], [6], and reliable over a long lifetime [7], [8].

Power density is a very critical target for the traction inverter due to the limited space under the hood, though the packaging constraints vary with the different drivetrain configurations, e.g., a traction inverter can be integrated with a DC/DC converter or even an on-board charger on some vehicle platforms, while a standalone traction inverter or a dual-inverter system may be used in others. It is usually quite difficult to make a fair comparison in terms of the volumetric power density (kW/L) among various traction inverter designs due to the differences in operating conditions, e.g., coolant and/or ambient temperatures, mission profiles and etc. In general, the power density of the traction inverters for commercial on-road vehicles in 2017 is around 18 kW/L [1].

Recently, electrified skateboard chassis [9], which includes the power electronics, motors and the battery energy storage, has demonstrated its superiorities in terms of greater vehicle design freedom, more usable passenger space, and etc. However, a significant increase in power density is required to fit a traction inverter into a skateboard chassis. Various strategies have been outlined in the 2017 roadmap from the U.S. Department of energy [1] to achieve 100 kW/L for a traction inverter with over 100 kW peak power by 2025. To achieve these targets, major technology breakthroughs are still required, which offers an opportunity to replace silicon devices with wide bandgap devices, e.g., the silicon carbide (SiC) MOSFETs, to reduce the size of the power modules while enabling operation at higher temperatures and high switching frequencies while achieving high efficiencies [1].

A significant amount of effort from both academia and industry has gone into research and development of high efficiency and high density SiC traction inverter for EVs and HEVs [10]. In 2016, Toyota prototyped an all SiC inverter and demonstrated it on an HEV. The testing results confirmed a 5% fuel efficiency improvement [11]. Tesla released their SiC MOSFETs based drivetrain on Model 3 in 2018 [12]. In 2019, Delphi Technologies claimed to be the first in the industry with

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volume production of 800-V SiC inverters [13]. In addition, the high temperature operation capability of the SiC devices can enable the use of high-temperature engine coolant for traction inverters, such that the dedicated, low temperature (e.g., 70˚C) cooling loop for the power electronics and motor/generator can be eliminated on HEVs. Wolfspeed has demonstrated a compact 110-kVA, 105 ˚C liquid cooled, SiC traction inverter [14] with a power density of 23.1 kVA/L. This inverter is also capable of operation at or above 140 ˚C ambient. In addition, John Deere has developed various prototypes for the 200-kW 1050-V SiC inverter system [15] which can operate using 115˚C coolant.

Clearly, SiC devices can be a game changer for EV traction inverters. However, a simple drop-in replacement of Si devices cannot fully realize the potential of SiC devices [16]. The inherently faster switching speeds of SiC devices can generate very high dv/dt and di/dt transitions, which may result in excessive voltage overshoots, false triggering, elevated electromagnetic interference (EMI) emissions, etc. A low inductance bussing structure is always desired to mitigate some of these issues [17]. In addition, to ensure the system reliability in the real-world applications, especially when aiming at higher power density, it is critical to select a SiC power module that can dissipate a sufficient amount of power to avoid operating beyond its maximum allowed junction temperature.

Usually the maximum power dissipation rating of the power module is given in the datasheet, which however may have several issues in practical applications. Firstly, the power dissipation rating provided in the datasheet is usually given at a specific case temperature that the system may not operate at, e.g., 25˚C [18]. Secondly, the amount of power that a module can dissipate depends on the cooling system used. Thirdly, the thermal interface material (TIM), which is usually applied between the module baseplate and cold plate surface, also introduces variability in the amount of power that a module can dissipate, as different TIMs have different thermal conductivities.

To address these issues, a comprehensive electrical and thermal characterization procedure is presented in this paper, which consists of several major tests, including the module curve tracing, a virtual junction temperature (VJT) test, and a clamped inductive load (CIL) test. The purpose of the proposed method is to characterize switching losses at different case temperatures and the module's maximum power dissipation (Pmax) as a function of coolant temperature. Based on the characterization results, it is feasible to determine the module's safe operating area (SOA) for a traction application in terms of the switching frequency and the coolant temperature. In this work, the proposed characterization procedure was validated on a custom 1200-V SiC module, as shown in Fig. 1, which has a peak current of 264 A and dimensions are 51.6 mm × 40.8 mm × 14.25 mm. In addition, in this work, the detailed design approach for a low-inductance bussing structure using heavy copper PCB is presented, which leads to a snubberless, low-overshoot and compact system design.

Fig. 1. A picture of the custom 1200-V SiC half-bridge module used in this work and its schematic.

II. The Proposed Electrical and Thermal Characterization Procedure

Fig. 2 shows the overall block diagram of the proposed electrical and thermal characterization method, which includes three major steps, i.e., (1) I-V curving tracing, (2) VJT based P_{max} characterization, and (3) CIL test.

In Step 1, the module is placed on a hot plate for sufficient long time, such that the junction temperature can be the same as the case temperature. Once the temperature is stable, a drain-to-source voltage (V_{ds}) vs. the drain-to-source current (I_{ds}) curve can be measured using a curve tracer. By changing the hot plate temperature, various V_{ds} vs. I_{ds} curves at different temperature can be obtained. Eventually, a 3-dimensional (3D) map, V_{ds} vs. I_{ds} and junction temperature can be obtained. Since the device junction temperature is not directly measured and a single value is used to represented the temperature of the junction area, it is called virtual junction temperature (T_{vj}) as defined in [19], [20] for IGBTs. Therefore, the 3D map is called as VJT map in this work. In addition, from VJT map, a profile of on-state resistance $R_{ds,on}$ vs. T_{vj} can also be obtained.

In Step 2, a VJT test setup, including the power stack, a low voltage power supply, a high current dc source, a power analyzer or voltage/current probes and heating circulator, is utilized. The power stack includes at least the power module, the TIM and the cold plate. The coolant temperature (T_{liquid}) is regulated at a constant by the heating circulator. During the VJT test, the power module is turned on by the low voltage power supply, while the dc source is used to regulate the Ids. The power analyzer or the voltage/current probe is used to monitor the V_{ds} and I_{ds}. When the V_{ds} reaches the value that corresponds to a 175˚C junction temperature on the VJT map, the power dissipation of the module is recorded. This process is repeated for several different T_{liquid}, such that a profile of P_{max} vs. T_{liquid} can be obtained.

In Step 3, a CIL test is performed with the module placed on a hot plate, such that the switching losses at various temperatures, that relevant to the particular application, can be obtained. Then feeding the VJT map, P_{max} vs. T_{liquid}, $R_{ds,on}$ vs. T_{vj}, switching loss data, and possible inverter mission profile into an inverter loss model, a safe operation area map for the power module in terms of switching frequency and T_{liquid} can be eventually obtained. The proposed method has been validated on the module shown in Fig. 1. The detailed characterization process and the related results are presented as follows.

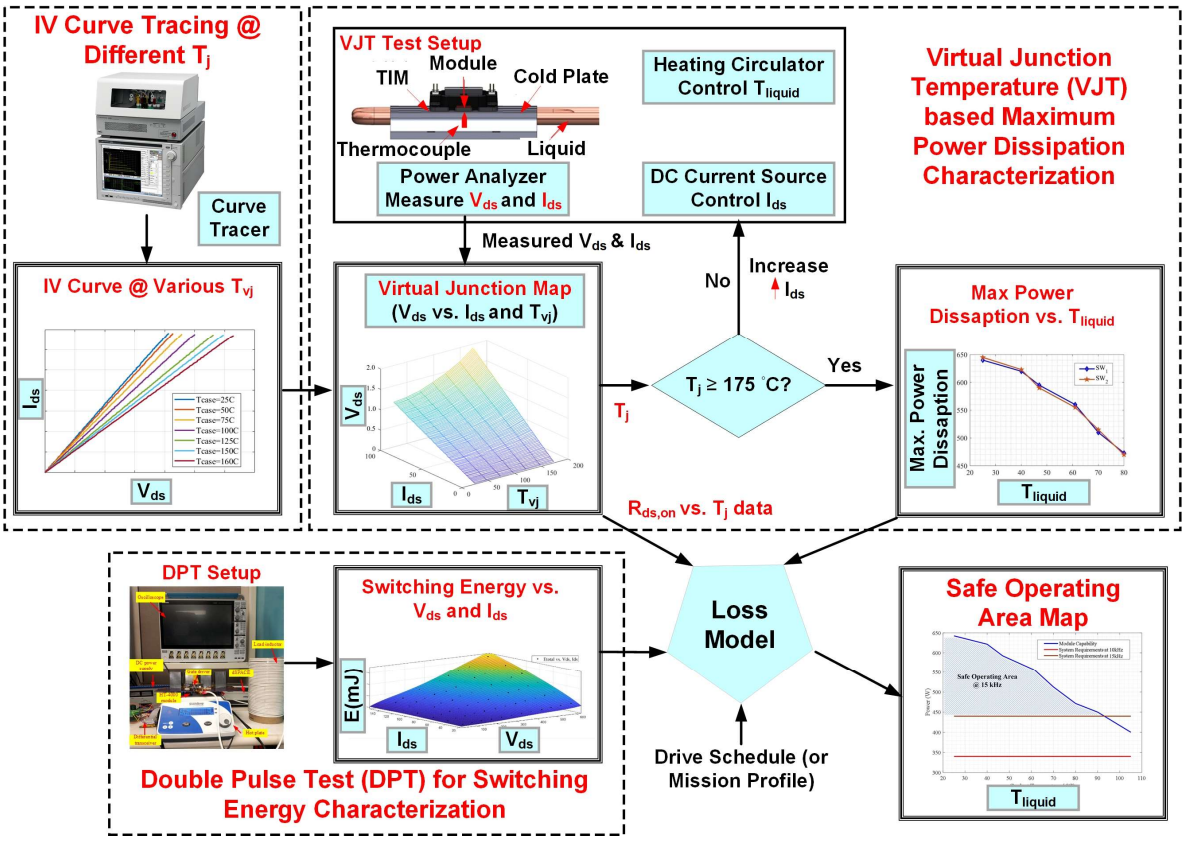


Fig. 2. The overall block diagram of the proposed electrical-thermal characterization procedure.

A. Switching Loss Characterization using CIL Test

Fig. 3 shows the CIL setup for the power module, where a 40.2-μH air-core inductor was used as the load. A high-bandwidth bar strap-type current-viewing resistor (CVR) with a 2.51-mΩ resistance was employed to measure the I_{ds}, while the V_{ds} and the gate-source voltage (V_{gs}) were measured using THDP0200 differential probes from Tektronix. The module was placed on a hot plate to regulate the case temperature, such that CIL tests can be performed at various temperatures. The CIL tests were performed at various DC-link voltages, including both 400 V and 800 V, which are typical bus voltage for automotive traction inverters. The load current varied from 50 A to 250 A. The curves of switching energy versus I_{ds} at 800-V DC-link voltages are shown in Fig. 4, which include the profile of turn-on energy E_{on}, turn-off energy E_{off}, and total energy E_{total}.

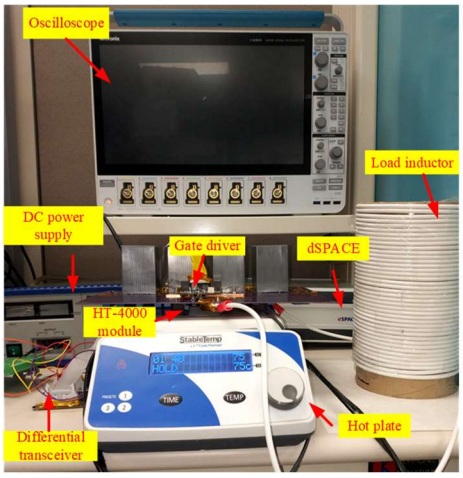


Fig. 3. The CIL setup for the SiC module.

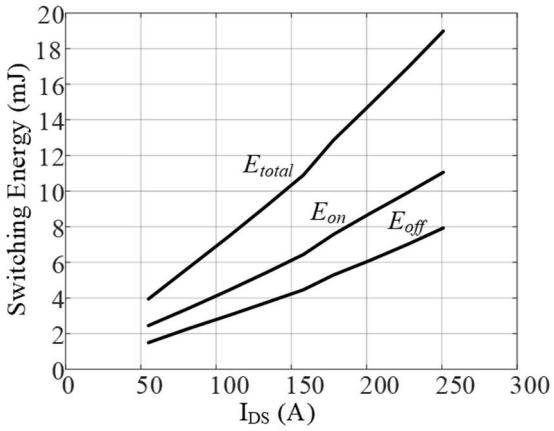


Fig. 4. Measured switching energy when V_{DC} = 800 V.

B. Thermal Characterization using VTJ based Approach

A thermal impedance network from the device junction to the liquid in the cold plate is shown in Fig. 5. Thermal power, i.e., P, that can transfer from the device junction to the liquid flowing through a cold plate, is determined by the thermal impedance from the junction of the module to the liquid of the cold plate, i.e., R_{jl}, and the temperature differential between the two, as

$$R_{jl} = \frac{T_{junction} - T_{liquid}}{P} \quad (1)$$

where $T_{junction}$ is the actual junction temperature of the device in the module. According to (1), it is possible to simply calculate the maximum possible power transfer achievable from the module junction to the liquid using a simplified thermal stack up modeled in Fig. 5. Though this method would yield some accuracy, however, the R_{jl} in every real-life system is different. Also, it is known that each of the impedances in the model, e.g., the thermal impedances from junction to module case R_{jc}, the TIM R_{TIM}, and the cold plate surface to liquid R_{SL} are all values advertised by manufacturers, which may not align with what the end users see in their systems. Considering these unclarities, the most accurate way to find the maximum possible power dissipation that the module can achieve is to perform experimental characterizations for the actual system that comprised of the power module, TIM, cold plate, and coolant with controlled flow rate and temperature.

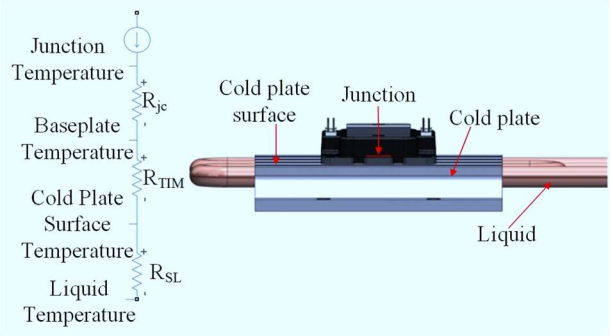


Fig. 5. A picture of the power module mounted on top of a cold plate and its equivalent thermal model.

A VJT test setup, as shown in Figs. 6, was built to identify the maximum power dissipation (P_{max}) of the 1200-V SiC module sample in the system to be prototyped. To accomplish this, the VJT map for the module was recorded using a curve tracer. The test requires a hole to be present in the cold plate to place a thermocouple probe through to measure the module case temperature T_c. Fig. 6 shows the cold plate modified by tapping mounting holes for the module and drilling holes to allow for probing of the baseplate. In addition, a fixture was 3D printed to hold the thermocouple probe on the module baseplate.

In the VJT test, the PCB was connected to a DC power supply, while the cold plate pipes were connected to a recirculating cooler/heater. The module gate connections were connected to a 15-V supply. A power analyzer was connected across the module to monitor its I_{ds} and V_{ds}. The high-current DC supply was placed in the current control mode and the drain current was increased while V_{ds} was monitored. When V_{ds} reached the value that corresponded to a 175°C junction temperature, the power dissipation of the module was recorded. This process was repeated for several different coolant temperatures. The results of the measured P_{max} vs. coolant temperature for the top (SW_1) and bottom (SW_2) switch positions are presented in Fig. 7. Other details are presented in Tables I and II, which include the measured P_{max}, the coolant temperature (T_{liquid}), case temperature (T_{case}), virtual junction temperature (T_{vj}) and the calculated thermal impedance from junction to module case R_{jc}.

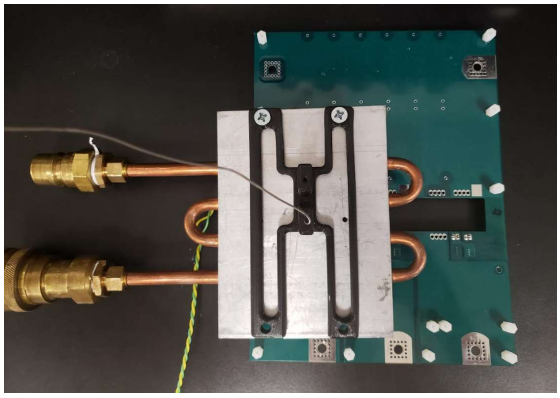


Fig. 6. Bottom view of the VJT setup developed for the custom SiC module.

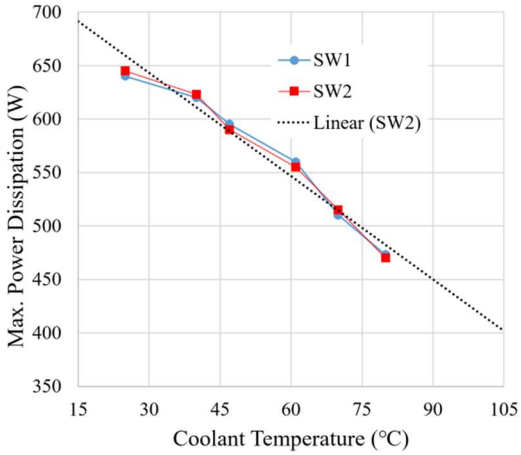


Fig. 7. The maximum power dissipation vs. the coolant temperature.

TABLE I
MAXIMUM POWER DISSIPATION IN THE TOP SWITCH POSITION

	T_{liquid} (°C)	P_{max} (W)	V_{DS} (V)	I_D (A)	T_{case} (°C)	T_{vj} (°C)	R_{jc} (°C/W)
SW_1	25	640	2.75	244	76	175	0.155
	40	620	2.65	234	84	175	0.147
	47	595	2.50	230	86	175	0.150
	61	560	2.56	219	98	175	0.138
	70	510	2.41	212	103	175	0.141
	80	473	2.31	205	110	175	0.137

TABLE II
MAXIMUM POWER DISSIPATION IN THE BOTTOM SWITCH POSITION

	T_{liquid} (°C)	P_{max} (W)	V_{DS} (V)	I_D (A)	T_{case} (°C)	T_{vj} (°C)	R_{jc} (°C/W)
SW_2	25	645	2.80	230	76	175	0.153
	40	623	2.67	233	84	175	0.146
	47	590	2.55	231	86	175	0.151
	61	555	2.50	222	98	175	0.139
	70	515	2.43	212	103	175	0.140
	80	470	2.30	204	110	175	0.138

C. Switching Frequency Selection for the SiC Power Modules

A comprehensive power loss analysis is performed using a model in Matlab/Simulink™ [5] with embedded switching losses captured by the CIL tests. Under the full load of 150 kW with a power factor of 0.9 lagging and utilizing sinusoidal pulse-width modulation, the module's average power dissipation is 440 W when switching at 15 kHz and 380 W at 10 kHz. When compared to the data in Tables I and II, it is clear that the power module meets the power dissipation requirements of the system at full load. However, according to Fig. 8, to achieve 150 kW with higher coolant temperature, e.g., 105°C, the switching frequency must be decreased, e.g., 10 kHz, since the achievable module power dissipation is only 400 W at 105°C. The simulated efficiency curves, when switching frequency are 10 kHz and 15 kHz, are shown in Fig. 9.

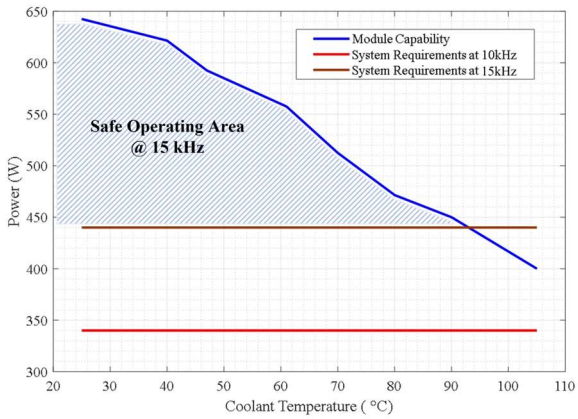


Fig. 8. System requirements for the module vs. the realistic power dissipation capability of the module.

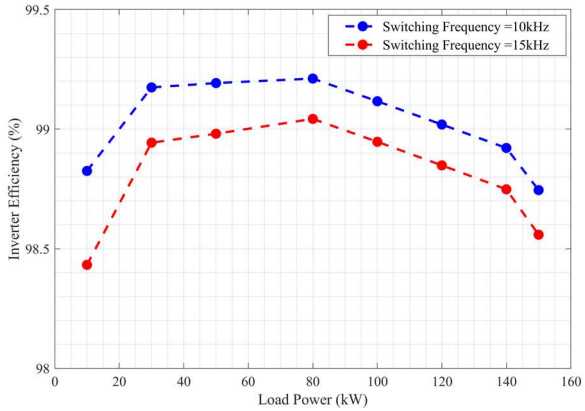


Fig. 9. The simulated efficiency curves.

III. Low-Inductance PCB Bussing Design

In a traction inverter system, a well-designed bussing structure should be able to tightly integrate the major components, such as the power modules and capacitors, while only contributing very minimum stray inductance to the current commutation loop (CCL), which mitigates the voltage overshoot during switching transients. The design of the power module, especially the arrangements of the power terminals, in turn affects the bussing design. In this section, the modules' impact to the bussing design, especially the PCB based bussing, is firstly discussed. Then the proposed low inductance bussing design for the custom SiC module is presented and followed by finite element analysis (FEA) simulation and experimental validations. Following design variables should be considered in the PCB based bussing, including (1) the number of the PCB layers and the thickness of each layer, which are critical to the temperature rise of the bussing structure; (2) the design of DC traces/layers and the stacking order of the DC layers, which is critical to reduce the bussing stray inductance; and (3) the number of DC input terminals, which is critical to the current distribution on the DC planes as well as the parasitic inductance.

A. Modules' Impact to the PCB Bussing Design

A three-phase traction inverter can be designed using either a three-phase six-pack module or three single phase half-bridge (HB) modules. The commercially available off-the-shelf SiC HB modules for automotive traction applications can be generally classified into two types based on the arrangement of their power terminals, i.e., the midpoint, or the AC output of the HB module, is located between the DC+ and DC– terminals, as shown in Fig. 10(b) or the DC terminals are placed on one side, while the AC output is on the other side, as shown in Fig. 10(c) and (d).

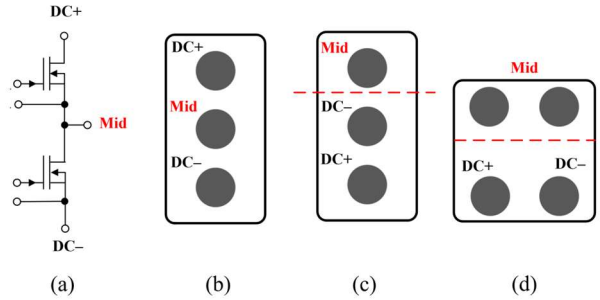
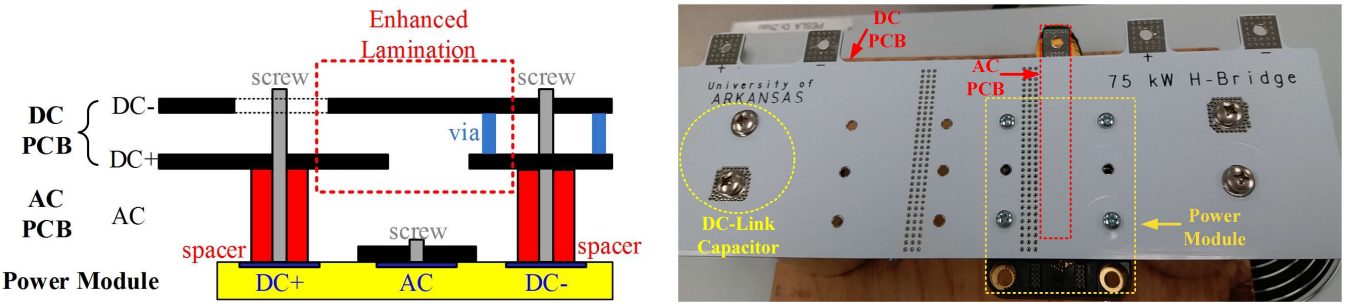


Fig. 10. The HB module (a) the schematic and (b)-(d) possible module power terminals arrangements.

The Wolfspeed CAS325M12HM2 [21] is an example of the first type of SiC modules. To design a low-inductance bussing, as presented in [22], the DC+ and DC– busbars are laminated into one structure and the AC busbar is separated from the DC busbars. Spacers are used to lift the DC busbars, such that the AC busbar can be bolted down to the module midpoint without affecting the lamination between the DC+ and DC– busbars, which is critical to minimize the stray inductance of the bussing structure. However, when using PCB bussing, the design can be complicated to accommodate all the constraints set by the power module and the PCB manufacturing process. The same module was used in the reference [23] to design a three-phase traction inverter, where an 8-layer laminated PCB bussing was proposed, which integrated all the AC and DC layers in a single PCB structure. In addition, snubber circuits were added to reduce the voltage overshoot.

Fig. 11 shows another PCB bussing design for an H-bridge converter using the same SiC module. The bussing was designed by the authors based on idea of the copper busbar design presented in [22], i.e., a two-layer heavy copper PCB



(a) (b)

Fig. 11. A low inductance PCB bussing design for the module with midpoint located between DC+ and DC- terminals (a) a diagram to illustrate the bussing design and (b) the picture of the prototype.

consists of DC+ and DC- layers and a separate PCB for the AC output. Spacers were still required to lift the DC PCB. As shown in Fig. 11(a), the DC– was placed on top of the DC+ plane. However, the DC– of the module requires a good contact with the DC– in the PCB. To address this issue, a large amount of vias were utilized to connect the DC– plane to the bottom layer. This PCB bussing design was complicated, which however resulted in very low inductance and didn't require addition snubbers to be added. The picture of the designed PCB bussing connected with module and capacitors is shown in Fig. 11(b).

The module used in this work, as shown in Fig. 1, has the power terminals arranged similar to that in Fig. 10(d), where DC terminals are placed on one side and the AC output is on the other side. This decouples the AC bussing design from the DC bussing, which can enable a seamless integration of all AC and DC bussing into one PCB and will significantly reduce the complexity of the PCB bussing design process. In addition, the module sample can be directly soldered to the PCB without using additional screws, though press-fit pin sockets were used to connect the modules to PCB to ensure stable and low-inductance connections. More details are presented in the following sections.

B. PCB Bussing Design Considerations for the Custom SiC Module

Since the module sample can be mounted to a PCB, the volume that the bussing added to the system as well as distances between the components could be minimized, which brought the added benefit of reducing parasitics. When designing the PCB bussing structure, special attention was given to the trace width and copper weight when dealing with systems that may carry large currents. If the traces are not sufficiently wide or the copper is not thick enough, the current carrying copper in the PCB reaches its glass transition temperature, typically rated around 175°C and begin to delaminate, causing the PCB to come apart and fail. Apart from that, attention was also given to the spacing between the different traces within the PCB. Both the copper width/weight and trace spacing in PCBs were designed by following the IPC-2221A and IPC-2221B [24]. The former outlines the minimum copper weight and thickness required for a given current level and desired temperature rise to avoid overheating the PCB, while the later outlines the minimum clearance between different PCB traces to avoid short circuits between traces.

Parasitic inductance minimization with even current density distribution among three phases was the top priority in the layout behind following the listed IPC standards. It is very advantageous to have the least inductance possible in the power loop, which consists of the bussing, power module, and DC-link capacitors. Excessive inductance in the power loop can lead to voltage ringing, elevated EMI emissions, and excessive voltage and current overshoots. Balanced impedance from the input to each power module is also critical. If the impedance from the input to each module is significantly different, it results in dissimilar switching performance among different phases of the inverter. To minimize the parasitic inductance and make the current density throughout the bussing as even as possible, several simulations using ANSYS are conducted to optimize the location and number of DC power terminals to the inverter, orientation of the DC-link capacitors, and shape of the DC traces.

A current density simulation in ANSYS of an early proposed PCB design for this research, presented in Fig. 12, demonstrates the impedance imbalance between each phase. From the simulation, it is very evident that the design with two DC terminals, i.e., one positive and one negative, the impedance from the input to each power module was very imbalanced, resulting in more current sinking to the power module on the left than any other devices. Furthermore, the current at the single input tab resulted in a current density above 5A/mm^2, which exceeds the maximum safe current density for a PCB. Together, those facts pointed toward a multiple input tabs design.

Contrary to the 2-terminal design, the 6-terminal design, i.e., three positive and three negative terminals, shown in Fig. 13, exhibits relatively even current distribution from the DC positive tabs to the drain of the high side position of each power module, especially considering that there are several holes in the DC plane because of the capacitor array. The current density distribution shown in Fig. 13 is only for the DC+ layer, thus only three DC positive terminals are present. From Fig. 13, it is clear that the majority of DC current distribution does not cross the midpoint of the modules or go above the middle output tab of the inverter. Therefore, the AC traces were routed in the leftover space above the midpoint of the power modules as shown in Fig. 13.

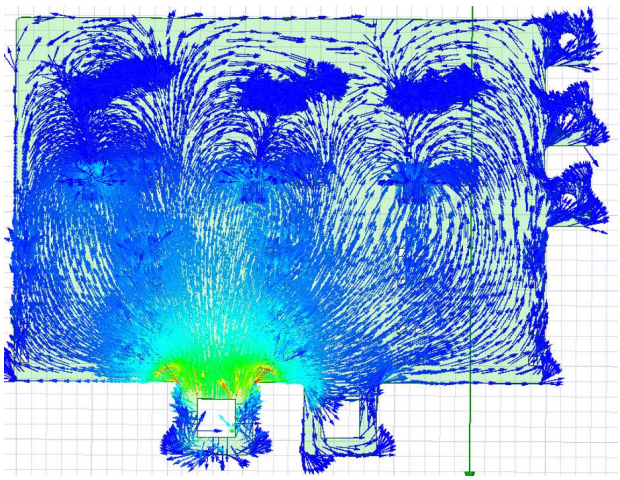


Fig. 12. Current density distribution of the 2-terminal design.

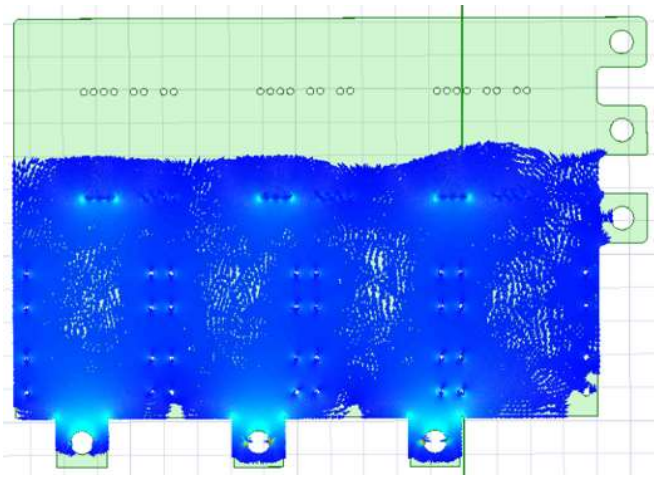


Fig. 13. Current density distribution on a DC positive layer of the 6-terminal design.

To further minimize the loop inductance, the DC-link bussing is split into four layers, consisting of alternating identical positive and negative layers. Based on the IPC-2221A and IPC-2221B standards, 200A with a realistic ambient temperature of 32°C (90°F), an allowable PCB temperature rise to 175°C, and 4 oz. copper, the minimum copper trace width is calculated as 51.3 mm. The required spacing between the high voltage traces to achieve electrical insulation up to 1000V is 1.5 mm for internal PCB layers and 2.33 mm for coated external PCB layers. The detailed PCB layout design for each layer is shown in Fig. 14.

In this work, with the reliability, overall system volume, capacitance rating, ripple current requirement [25], voltage rating at high temperature, and capacitance rating at high temperature in mind, an array of 8 Vishay MKP1848C61012JP4 capacitors in parallel is chosen as the DC-link capacitor. Each capacitor is rated for 1440-V at 70-°C, 850-V at 105°C, 10 µF, and 11 A rms. Combined, the capacitor array yields a total DC-link capacitance of 80 µF and ripple current capability of 88 A RMS current. As can be seen from Fig. 14, the DC-link capacitors are placed tightly on the PCB bussing to reduce the volume of DC-link.

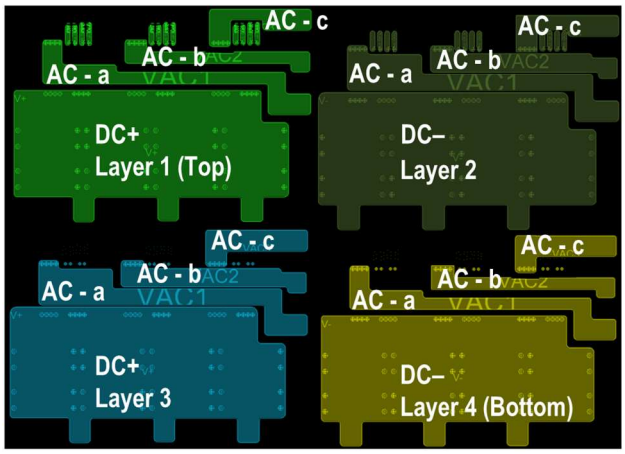


Fig. 14. PCB bussing layout design.

C. *Current Density Analysis*

To evaluate the current distribution in the PCB bussing design shown in Fig. 14, the current density analysis was performed using ANSYS simulation. The model of the PCB bussing is shown in Fig. 15. In the simulation, the current density for the DC+ layer and DC– layer was analyzed separately. For the DC+ layer, three input tabs were defined as the current sources, which equally shared the rated DC link current, while the DC+ terminals of the modules were defined as sinks. The current density simulation result for DC+ layer is shown in Fig. 16(a). For the DC– layer, the DC– terminals of the modules were defined as the current sources, while the DC– tabs were defined as sinks. The current density simulation result for DC– layer is shown in Fig. 16(b). From the simulation results, the current was evenly distributed for both layers and the maximum current density was lower than 5 A/mm^2.

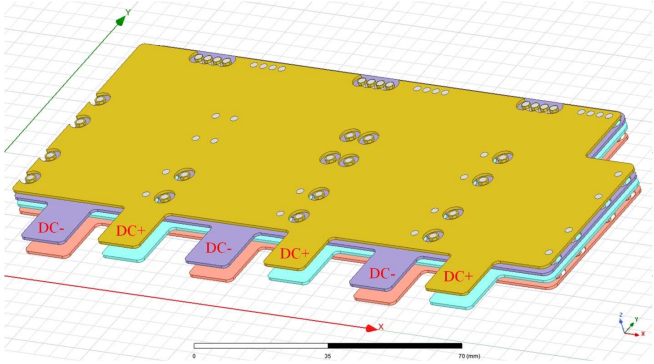
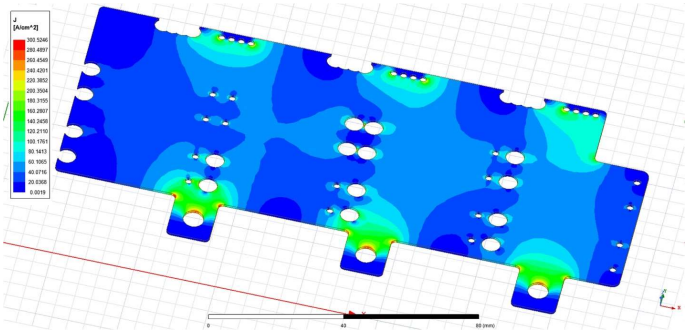
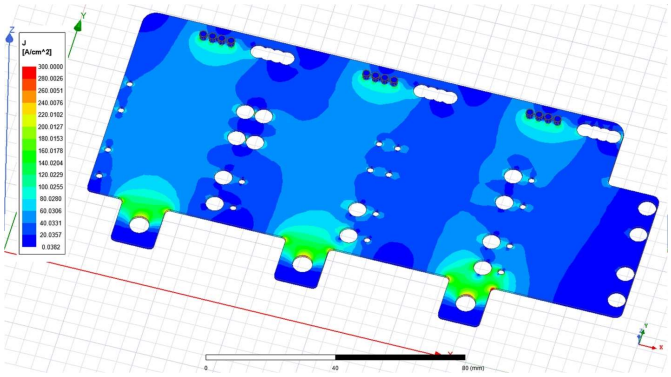


Fig. 15. DC bussing model in ANSYS for current density analysis.

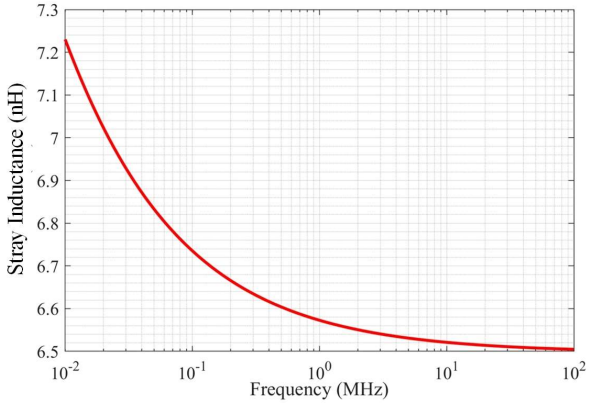


(a)

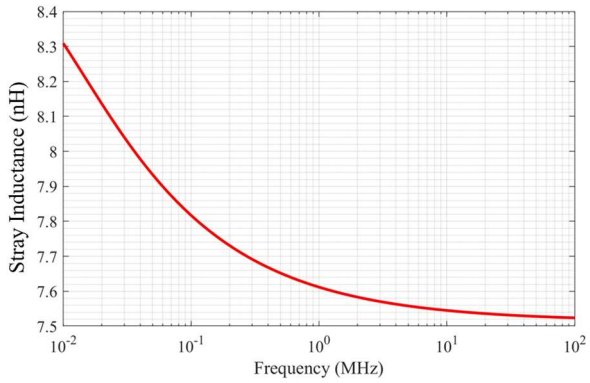


(b)

Fig. 16. Current density simulation results: (a) DC+ layer and (b) DC– layer.



(a)



(b)

Fig. 17. The simulated stray inductance of the PCB bussing for (a) 6-terminal design and (b) 2-terminal design.

D. Parasitic Inductance Extraction and Measurement

ANSYS Q3D extractor was used to determine the parasitic inductance of to the 4-layer PCB bussing and DC-link capacitors. As shown in Fig. 17(a), the simulated stray inductance is around 6.5 nH at 10 MHz, which is a relatively low value that is expected to yield acceptable switching performance. As a comparison, the simulated parasitic inductance for the 2-terminal design is 7.5 nH. The stray inductance reduction in the 6-terminal design is mainly due to the balanced current distribution on the DC planes. The actual parasitic inductance of the prototyped bussing structure, including the stray inductance of the PCB bussing and DC-link capacitor bank, was measured using a Keysight E4990 impedance analyzer. Each phase's parasitic inductance measured in the range of 6.8 nH to 7.0 nH, which is close to the simulation result. Fig. 18 displays an example of the measured impedance plot.

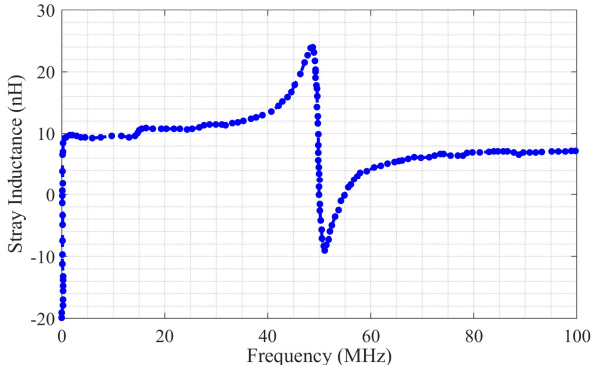
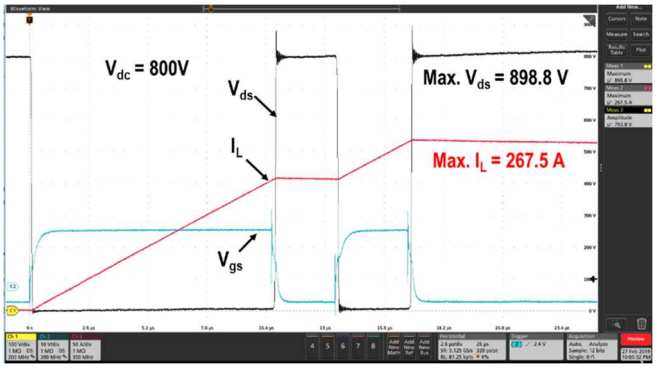
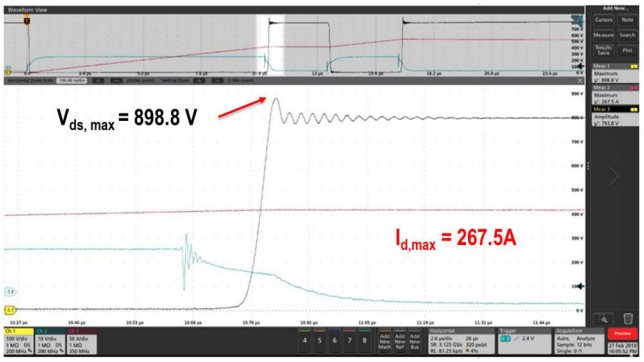


Fig. 18. The measured loop impedance for inverter phase *a*.

DPT was performed for the module in each phase to verify the switching performance of the SiC modules in the actual inverter system. The V_{ds} was measured by a differential probe THDP0200, while load current was measured by a current probe TRCP0600, since it is not feasible to mount CVR on the actual prototype. A typical DPT result for one phase of the inverter is shown in Fig. 19, where the switching performance can be observed at the maximum desired current, i.e., 267.5 A, which is slighted above the maximum rated current of the power module. With the 800-V DC bus voltage, the voltage overshoot of the V_{ds} is less than 100 V, which validates the low inductance bussing design. Based on this result, considering the available headroom, the DC-link voltage can be further increased to 900 V.



(a)



(b)

Fig. 19. (a) typical DPT results for a SiC module in the actual inverter and (b) a zoomed-in view of the turn-off transient.

IV. Traction Inverter System Assembly and Experimental Validation

To achieve high power density, all components are modeled in SolidWorks and arranged in the most compact fashion possible. The cold plate is custom designed by Wieland Microcool, which is a channeled cold plate that offers very low thermal impedance without sacrificing much in terms of volume. A custom PCB mounted dual-channel differential isolated gate driver is used to drive the SiC modules. The gate driver has roughly the same size footprint as the power module and also has all the essential protections such as undervoltage lockout, reverse polarity, and fault indicators with lockout built in. As the exploded view shown in Fig. 20, the proposed traction inverter system consists of the SiC power modules and gate drivers from Wolfspeed, a DC link formed by 8 Vishay MKP1848C61012JP4 capacitors, the custom Wieland Microcool cold plate, and the PCB bussing. The modules are connected to the bussing using press fit pin sockets. The overall system dimensions of the power stage, as shown in Fig. 21, are 6.88" × 4.80" × 2.49", leading to a total volume of 1.35 L. The volume of the custom enclosure is 1.75 L, which yields a power density of 86 kVA/L.

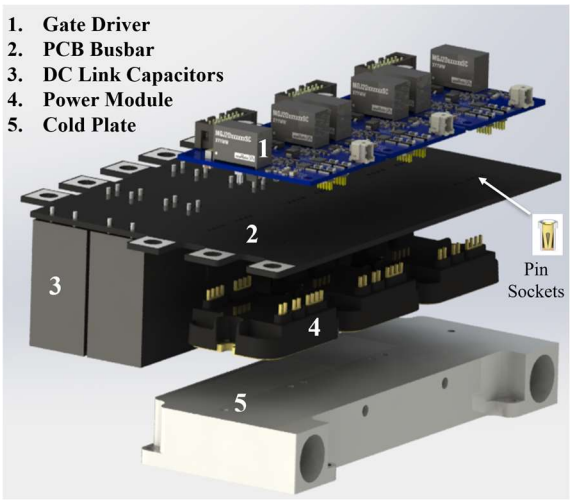


Fig. 20. The exploded view inverter system design.

Fig. 21. A picture of the traction inverter prototype.

The continuous power test for the inverter prototype is also performed to evaluate the performance of the inverter connected to a resistive-inductive (RL). The gate signals were generated by a dSPACE MicrolabBox and an interface board is used to connect the gate pulse from dSPACE to gate driver via transceiver. The phase current and phase voltages are captured in the oscilloscope.

Fig. 22 presents the experimental waveform of the inverter at 700-V dc-link voltage with 0.8 modulation index and 150-A peak output current. Two line-to-line output voltages of the inverter are shown as V_{ab} and V_{bc} and the phase *a* output current given as I_a. In this experiment, no additional output filter is used, therefore, the line-to-line voltage at the inverter terminal is a typical PWM voltage waveform, while the output line current is sinusoidal due to the use of RL load. To mimic a motor load, experiments are also done to achieve variable output frequency. As shown in Fig. 23, a step change in the fundamental frequency was applied to validate the traction mode of the inverter, where the fundamental frequency of the output AC was increased from 500 Hz to 1500 Hz. The output current was maintained at 150 A when changing the frequency.

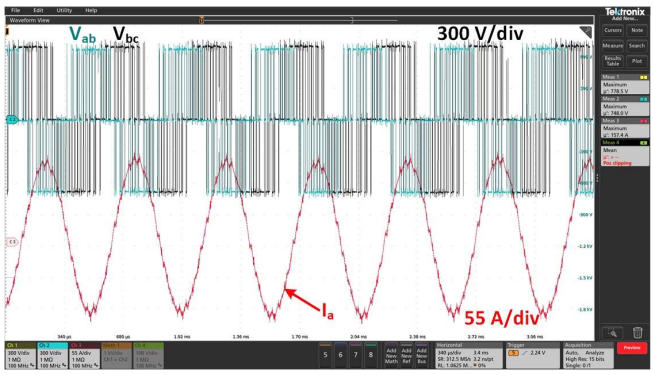


Fig. 22. Three-phase continuous test results with static load.

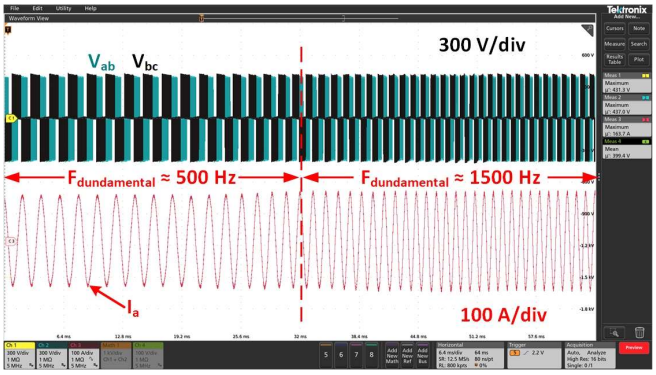


Fig. 23. Inverter test results with variable fundamental frequency.

V. Conclusion

In this work, a comprehensive electrical and thermal characterization procedure is presented to characterize maximum power dissipation the SiC module as a function of coolant temperature. Using data collected by the proposed characterizations, it is feasible to determine the module's safe operating area for a traction application in terms of the switching frequency and the coolant temperature. In this work, the proposed characterization procedure was validated on a custom 1200-V SiC module. In addition, low-inductance low-

cost PCB bussing design is proposed to enable a snubberless system with low-overshoot. Experimental studies have been performed to validate the effectiveness of bussing design. The overall volume of the designed 150 kVA 800V inverter is around 1.75 L, which leads to an inverter volumetric power density of 86 kVA/L.

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