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ABSTRACT

The gate charge change (ΔQ_g) of GaN-on-Si power devices subjected to different substrate biases has been investigated. On-wafer pulse-mode voltage stress measurement is examined to probe the physical insight of different trap mechanisms into Q_g characteristics. Distinct injected electrons interacting with the buffer traps lead to a significant decrease (increase) in Q_g under negative (positive) substrate bias. Different levels of degradation on ΔQ_{gd} to ΔQ_{gs} after stress under negative and positive substrate biases indicate uneven distribution of acceptor-like traps and uniform distribution of donor-like traps in the GaN buffer level. Using Arrhenius plots associated with the ΔQ_g shift, three dominant buffer traps with activation energies of $E_V + 0.542$ eV, $E_C - 0.604$ eV, and $E_C - 0.608$ eV are extracted.

GaN-on-Si power devices have been widely studied in recent years owing to outstanding electrical performance including high voltage breakdown voltages, low on-resistance (R_{on}), and high switching speed.[1,2] In order to achieve high power efficiency, stable and low R_{on} and small Q_g have been regarded as two critical parameters to reduce conduction loss and switching loss in a power converter, respectively.[3] The effect of substrate biases on dynamic R_{on} degradation due to traps in the GaN buffer layer has gained a lot of attention recently.[4] Nevertheless, Q_g under different substrate biases and its physical insight are not well understood.

In GaN-on-Si lateral power devices, the Si substrate can be used as an independent contact termination rather than a thermal cooling pad.[5] Although some studies have shown the benefit of using positive substrate bias to reduce dynamic R_{on} degradation with reduced acceptor-like traps,[6] it remains unclear what type of substrate connection is a better choice for reducing Q_g. The relationship between the trap mechanisms induced from substrate biases and Q_g characteristics is not quite clear.

In this work, we systematically investigate the impact of substrate biases on the Q_g of the GaN-on-Si power devices using the pulse-mode voltage stress measurement to mimic the power converter circuit operation environment. Three dominant GaN buffer traps are extracted from the Arrhenius plots under different substrate biases. Different levels of degradation on ΔQ_{gd} and ΔQ_{gs} under negative substrate biases suggest an uneven lateral distribution of ionization of acceptor-like traps in the buffer layer.

GaN-on-Si devices, using a CMOS-compatible process flow, with a nominal threshold voltage of ≈ -8.7 V, are examined in this study. The epitaxial structure is grown on a p-type silicon substrate (111) by means of metalorganic chemical vapor deposition (MOCVD) and features a stack of an AlN nucleation layer, a graded AlGaN buffer, a carbon doping GaN layer, an $Al_{0.3}Ga_{0.7}N$ barrier layer, an extra GaN cap layer, a SiN passivation layer deposited by PECVD, and a Ni/Au gate metal evaporated to form a Schottky contact. Finally, Ti/Al/Ni/Au drain and source Ohmic contacts are realized.

The traditional Q_g measurement is usually based on a packaged device with external discrete components, which cannot be integrated with the pulse-mode stress measurement. In order to implement the on-wafer measurement, a Q_g measurement to separate Q_{gd} from Q_{gs} was proposed by Krishnam *et al.* using C–V measurement data.[7] The extracted Q_{gd} and Q_{gs} plots under different substrate biases are shown in Fig. 1(b). The opposite effect of substrate bias on Q_g subjected to positive and negative biases suggests a distinct electron injection mechanism relating to different buffer traps.

In order to mimic the power converter circuit operation environment, the pulse-mode stress measurement has been adopted to

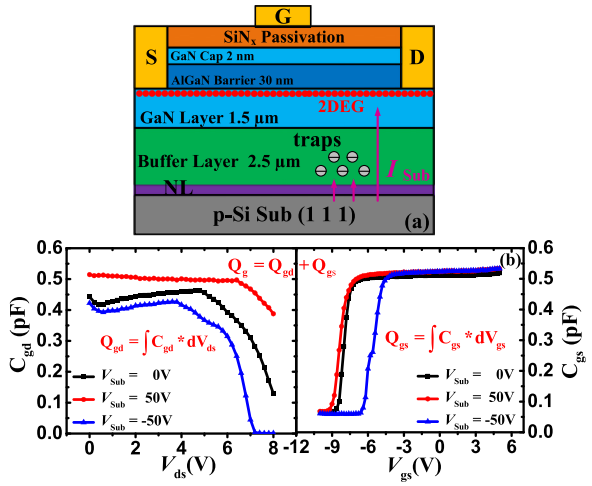

FIG. 1. (a) Schematic of measured GaN-on-Si power devices with $L_{gd}/L_g/L_{gs} = 2/1/2\ \mu m$. (b) Q_g extraction using the C–V measurement under different substrate biases.

evaluate the Q_g degradation as in our previous paper.[4] The device under the wafer-level test was continuously switched between the off-state at $V_{GL} = -10$ V and $V_{DH} = 40$ V and the on-state at $V_{GH} = -5$ V and $V_{DL} = 1$ V with a pulse period of 3.1 μs. Both drain and gate voltage waveforms with a DC substrate bias were provided by using the two ultra-fast pulse I–V PMU modules (4225) with a Keithley 4200A SCS. To avoid the recovery effect, ΔQ_g is recorded on-the-fly right after the pulse, which is applied to the gate and drain terminals, and its reaction time is much less than the recombination time of most kinds of traps to assure an accurate extraction of Q_g.[8]

To study the impact of substrate bias and buffer traps on the Q_g distribution, the correlation between Q_{gd} and four representative negative/positive substrate biases is illustrated in Figs. 2(a) and 2(b). With

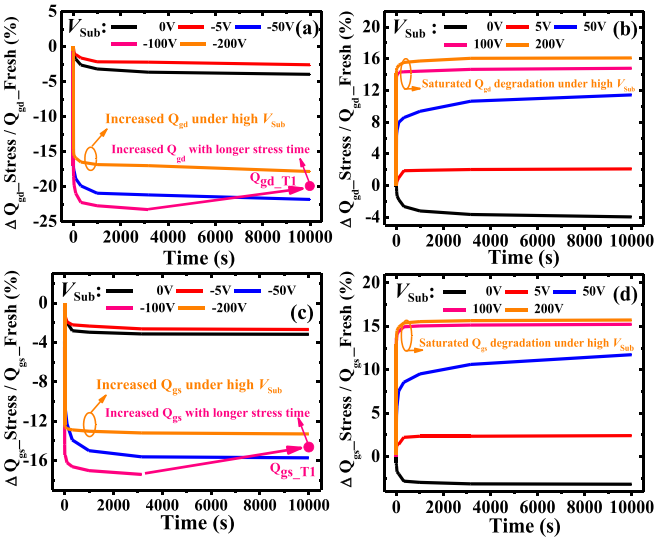

FIG. 2. Q_{gd} shifting characteristics under (a) negative and (b) positive substrate biases. Q_{gs} shifting characteristics under (c) negative and (d) positive substrate biases.

the increasing magnitude of negative substrate bias, the ionized acceptor-like buffer traps play a key role under increased negative substrate bias,[9] where the generated negative net charges result in a reduction of Q_{gd} by 20% after 10 000 s of pulse-mode stress. It is interesting to note that increased Q_{gd} has been observed at very low negative substrate bias (e.g., $V_{Sub} = -5$ V). This indicates that the ionization of donor-like buffer traps produces positive net charges to compensate the 2DEG with increased Q_{gd}.[4] An unexpected increased Q_{gd} has been observed with long stress time at $V_{Sub} = -100$ V, and this phenomenon continuously occurs at $V_{Sub} = -200$ V. It is believed that high-energy accelerated electrons under high negative substrate biases are injected from the substrate to the buffer layer to ionize more buffer traps with increased Q_{gd}.

The correlation between ΔQ_{gd} and positive substrate bias is demonstrated in Fig. 2(b). The normalized ΔQ_{gd} is up from 3.2% to 14% with a positive substrate bias from 5 V to 100 V after 10 000 s of pulse-mode stress. A hole accumulation layer has been formed at the interface of the NL/Si junction under the positive substrate biases. The negative top-to-substrate voltage difference provides a reservoir of free electrons from 2DEG, which can be more effectively injected into the buffer layer and verified by the relatively higher vertical leakage current.[4] An increased negative net charge is induced by the neutralized donor-like traps with the electron injection in the buffer layer and is regarded to as the dominant source for the increased Q_{gd} under positive substrate biasing. When the positive substrate biasing goes beyond 100 V, more holes are accumulated in the NL/Substrate junction with a larger negative top-to-substrate voltage difference, which induces a high mirror electron concentration in the buffer layer. A saturated Q_{gd} change is due to the dynamic equilibrium between the 2DEG electron injection, neutralized donor-like traps, and the mirror electrons under high positive substrate biases.

ΔQ_{gs} shows similar behavior under different positive and negative substrate biases as Figs. 2(c) and 2(d). The ionized donor-like traps and acceptor-like traps play a pivotal role under positive, small negative, and large negative substrate biases, respectively. High energy electrons from the inverted substrate induce increased Q_{gs} with longer stress time at large negative substrate biases. The saturated ΔQ_{gs} change under large positive substrate bias is owing to the equilibrium of a dynamic process between 2DEG electron injection, neutralized donor-like traps, and the mirror electrons under high positive substrate biases. In addition, the ΔQ_{gs} shift is smaller than that of ΔQ_{gd} under negative substrate biases but shows similar degradation under positive substrate biases. This implies that the acceptor-like trap concentration between the gate and drain region is much larger than that between the gate and source region. On the contrary, the uniform distribution of donor-like traps introduces the same level of ΔQ_{gd} and ΔQ_{gs} degradation under positive substrate biases.

The same behavior of Q_g has been observed as ΔQ_{gd} and ΔQ_{gs} characteristics in Table I. It is interesting to note that ΔQ_{gd} contributes more than ΔQ_{gs} to the Q_g degradation, which indicates that the equivalent capacitance between the gate and drain region is much larger than that between the gate and the source region.

The physical mechanisms and energy band diagrams of the measured Q_g degradation under positive or negative substrate biases are discussed with trapping/de-trapping in the buffer layer as depicted in Fig. 3. The distinct electron accumulation mechanisms induce an increase in ΔQ_g under positive V_{Sub} [see Fig. 3(a)]. The built-in electric

TABLE I. Q_g shifting characteristics under V_{Sub} (at 10 000 s stress time).

V_{Sub}	$\Delta Q_g/Q_g$ (%)	Contribution from ΔQ_{gd}	Contribution from ΔQ_{gs}
−5	−2.65	68.24%	31.75%
−50	−17.70	59.92%	40.07%
−100	−16.36 (Q_{g_T1})	60.35%	39.65%
−200	−14.77	60.73%	39.27%
5	2.31	70.50%	29.50%
50	11.65	68.08%	31.92%
100	15.10	68.13%	31.87%
200	15.85	66.98%	33.02%

field from a positive V_{Sub} generates a hole-accumulation layer at the interface between the nuclear layer and p-type Si substrate and the energy band in the buffer layer as seen in Fig. 3(c). The electron injection from the 2DEG neutralizes donor-like traps in the buffer layer and is regarded to as the dominant source for the Q_g change under positive substrate biasing. The uniform distribution of ionized donor-like traps induces a balanced increase in Q_{gd} and Q_{gs}. When the positive substrate bias goes beyond 100 V, holes are accumulated in the NL/Substrate junction with larger negative band bending, which induces a high mirror electron concentration in the buffer layer. These mirror electrons also help neutralize the donor-like traps to release the electron injection from the 2DEG with the saturated Q_g change under high positive substrate bias.

There are two types of traps under a negative substrate bias as shown in Fig. 3(b). For instance, under a small negative substrate bias (such as $V_{Sub} < -10$ V), donor-like traps coming from the oxygen of MOCVD play a dominant role in increasing the Q_g change.[10] Ionized donor-like traps will perform as positive net charges in the buffer layer, which will then compensate the negative deep-level acceptor-like traps induced by off-state drain voltage. With the increased negative substrate bias, the p-silicon substrate will perform from deep-depletion mode to inverted silicon with electron accumulation at the NL/Si junction as shown by the band diagram in Fig. 3(c). The decreased Q_g obtained with a negative V_{Sub} seems to be contrary to what was reported in Ref. 11. Such a difference could come from different substrate voltage levels, which are over 200 V in substrate bias used in Ref. 11. In this work, low voltage devices with $|V_{Sub}| < 200$ V were measured. The smaller negative substrate biases cannot produce enough high-energy electrons to overcome the energy barrier of the NL/Si junction at the low negative substrate biases. As a result, the electron space charges from the depletion of the p-type silicon substrate induce mirror holes in the buffer layer to accelerate the de-trapping process in the ionized acceptor-like traps with decreased Q_g. However, when the substrate bias is larger than −100 V, an inverted p-silicon at the NL/Si junction has been illustrated as the positive band bending. The accumulate electrons can be injected via thermionic emission and Poole–Frenkel effects at high negative substrate biases to ionize more acceptor-like traps in the buffer layer.[12] The increased number of ionized acceptor-like traps, which performed as the negative net charges, will increase the equivalent charge for the device charge system as combined with 2DEG. The increased equivalent charge in the device will induce an increasing Q_g under high negative substrate biases as indicated by measurement data. In addition, a high acceptor-like trap concentration between the gate and drain regions induces an imbalance between Q_{gd} and Q_{gs} changes.

In order to determine the trap mechanisms under each substrate bias, temperature-dependent measurement has been conducted to extract the trap energy distribution. We found that Q_{g_T1} has an Arrhenius dependence on temperature, as shown in Fig. 4(a), with an activation energy of 30.15 meV. This value is consistent with the ionization energy of p-type acceptors in the p-type substrate,[13] thus supporting the hypothesis on the increased Q_g at long stress time and high negative substrate bias relating to hole accumulation in the substrate.

By applying pulse-mode stress with different temperatures, the Arrhenius plot is drawn using the points (T, τ) when τ is the emission process time constant measured for the considered traps at the ambient temperature T.[14] Using this procedure, Arrhenius plots depicted in Fig. 4(b) with three typical substrate biases have been illustrated. According to the Arrhenius plot, the level of the acceptor-like traps at $E_V + 0.542$ eV (close to the reported carbon-induced level at $E_C - 2.85$ eV in GaN) was extracted, supporting the analysis of decreased Q_g under negative

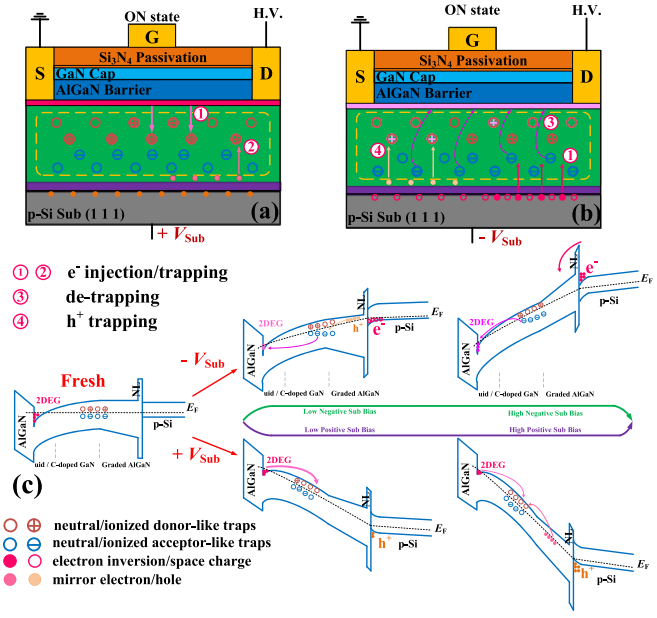

FIG. 3. Schematics of the buffer trapping/de-trapping at (a) positive substrate bias, (b) negative substrate bias, and (c) band diagram under different substrate bias conditions.

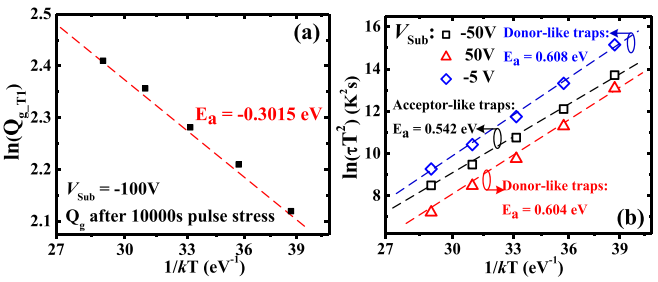

FIG. 4. Arrhenius plots of (a) Q_{g_T1} with the corresponding activation energy. (b) Different substrate biases with the corresponding activation energy.

substrate bias by depleting the 2DEG from acceptor-like buffer traps.[15] The donor-like trap levels at $E_C - 0.604$ eV and $E_C - 0.608$ eV were extracted,[15] supporting the increased Q_g with donor-like traps under small negative substrate bias and high positive substrate bias.

In summary, the effect of substrate biases on Q_g characteristics has been investigated under pulse-mode voltage stress. Compared to that of grounded substrate bias, a significant decrease in Q_g has been observed resulting from the acceptor-like buffer traps under high negative substrate biases. However, the high-energy hole-injection with 30.15 meV activation energy neutralizes the ionized buffer traps with an increased Q_g under higher negative substrate biases. On the contrary, an increased Q_g is attributed to the donor-like buffer traps under positive substrate biases. Traps with an activation energy of $E_a \sim 0.542$ eV are most likely acceptor-like traps, which is correlated with C doping in the buffer layer. The other two traps with $E_a \sim 0.608$ eV and $E_a \sim 0.604$ eV are most likely donor-like traps under small negative substrate biases and positive substrate biases, respectively. In addition, different ΔQ_{gd} and ΔQ_{gs} changes under negative substrate biases indicate an uneven distribution of acceptor-like traps, while the same degradation level of ΔQ_{gd} and ΔQ_{gs} under positive substrate biases suggests a uniform distribution of donor-like traps from oxygen in the MOCVD process.

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REFERENCES

[1]A. Q. Huang, Proc. IEEE **105**, 2019 (2017).
[2]A. Binder, S. Khan, W. Yang, J. S. Yuan, B. Krishnan, and P. M. Shea, ECS J. Solid State Sci. Technol. **8**, Q15 (2019).
[3]R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, IEEE Trans. Power Electron. **32**, 6416 (2017).
[4]W. Yang, J. S. Yuan, B. Krishnan, and P. Shea, in IEEE International Reliability Physics Symposium (IRPS), Monterey, USA, 31 March–4 April (2019), pp. 1–7.
[5]G. Tang, J. Wei, Z. Zhang, X. Tang, M. Hua, H. Wang, and K. J. Chen, IEEE Electron Device Lett. **38**, 937 (2017).
[6]W. Yang, J. S. Yuan, B. Krishnan, and P. Shea, IEEE Trans. Device Mater. Reliab. **19**, 350 (2019).
[7]V. Krishnamurthy, A. Gyure, and P. Francis, in IEEE International Conference on Microelectronic Test Structures, San Diego, USA, 19–22 March (2012), pp. 98–100.
[8]M. Denais, C. Parthasarathy, G. Ribes, Y. R. Tauriac, N. Revil, A. Bravaix, V. Huard, and F. Perrier, in IEEE International Electron Devices Meeting (IEDM), San Francisco, USA, 13–15 December (2004), pp. 109–112.
[9]W. Yang, J. S. Yuan, B. Krishnan, A. J. Tzou, and W. K. Yeh, in IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, USA, 31 October–2 November (2018), pp. 103–107.
[10]D. Bisi, M. Meneghini, F. A. Marino, D. Marcon, S. Stoffels, M. V. Hove, S. Decoutere, G. Meneghesso, and E. Zanoni, IEEE Electron Device Lett. **35**, 1004 (2014).
[11]H. Zhang, S. Yang, and K. Sheng, *In IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Chicago, USA, 13-17 May 2018, pp. 100–103.
[12]P. Moens, A. Banerjee, M. J. Uren, M. Meneghini, S. Karboyan, I. Chatterjee, P. Vanmeerbeek, M. Cäsar, C. Liu, A. Salih, E. Zanoni, G. Meneghesso, M. Kuball, and M. Tack, in *IEEE International Electron Devices Meeting (IEDM)*, Washington, USA, 7-9 Dec. 2015, pp. 35-32.
[13]M. Borga, M. Meneghini, S. Stoffels, X. Li, N. Posthuma, M. V. Hove, S. Decoutere, G. Meneghesso, and E. Zanoni, IEEE Trans. Electron Devices **65**, 2765 (2018).
[14]D. V. Lang, J. Appl. Phys. **45**, 3023 (1974).
[15]D. W. Cardwell, A. Sasikumar, A. R. Arehart, S. W. Kaun, J. Lu, S. Keller, J. S. Speck, U. K. Mishra, S. A. Ringel, and J. P. Pelz, Appl. Phys. Lett. **102**, 193509 (2013).