

A Hardware-in-the-Loop Platform for DC Protection

Mark Vygoder, *Student Member, IEEE*, Matthew Milton, Jacob Gudex, *Student Member, IEEE*, Robert Cuzner, *Senior Member, IEEE*, Andrea Benigni, *Senior Member, IEEE*

Abstract—Real-time (RT) simulation of power and energy conversion systems allows engineers to interface both simulation- and hardware-based controls using controller hardware-in-the-loop (CHiL) simulation of networks of power electronic converters (PECs) in order to de-risk highly developmental systems such as next generation electrified transportation systems and dc microgrids. CHiL exploration and performance verification moves a design from Technology Readiness Level (TRL) 3 to TRL 4 without incurring significant cost investments in developmental hardware platforms, which otherwise discourages such endeavors. A real-time CHiL simulation platform suitable for explorations of protective equipment, protection schemes and networked PEC dc and mixed dc-ac power distribution architectures must be capable of simulating common-mode behavior, various grounding schemes, and fault transients at sufficiently high resolution. This paper demonstrates this capability using a Latency-Based Linear Multistep Compound (LB-LMC) simulation method implemented in a commercially sustainable, adaptable and expandable FPGA-based test and instrumentation platform. The proposed CHiL platform achieves real-time power system simulations, including detailed switching commutations of networked PECs, with 50 ns resolution, and faithfully produces resonant and transient behaviors associated with line-to-ground (LG) and line-to-line (LL) faults and fault recovery in ungrounded PEC-based dc systems. This resolution in RT cannot be achieved with today's commercial off-the-shelf CHiL platforms. This paper demonstrates the need for high resolution RT simulation of LG and LL faults within dc systems, and demonstrates a CHiL approach that enables dc protection design explorations and protective control hardware testing while taking into account the realistic aspects that affect fault characteristics in PEC-based dc systems, such as cable current rating and length, cable and PEC parasitic LG capacitance and PEC internal response to fault scenarios.

Index Terms—Hardware-in-the-Loop simulation, Power system Simulation, Fault protection, microgrids, Power distribution faults

I. INTRODUCTION

Utilization of power and energy from multiple, time-variant distributed energy resources (DERs), requires either ac-dc or dc-dc power electronic converter (PEC) interfaces between DERs and a distributed network for power and energy delivery.

This material is based upon work supported in part by the National Science Foundation, Grant No. 1650470, and in part Office of Naval Research, Grant N00014-16-1-3042, and N0024-19-2-0004. Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of these institutions.

M. Vygoder, J. Gudex and R. Cuzner are with the Department of Electrical Engineering, University of Wisconsin-Milwaukee, Milwaukee, WI 53211 USA (email: mvygoder@uwm.edu; jdgudex@uwm.edu; robcuzner@ieee.org).

M. Milton is with the Department of Electrical Engineering, University of South Carolina, Columbia, SC, 29208 USA (email: mmilton@email.sc.edu).

A. Benigni is the Chair of Methods for Simulation of Energy Systems, RWTH Aachen University, and is with the Institute of Energy and Climate Research: Energy Systems Engineering (IEK-10), Forschungszentrum Juelich GmbH, Wilhelm-Johnen-Str., 52428 Juelich, Germany (email: a.benigni@fz-juelich.de).

In electrified transportation systems and microgrids efficiencies and resiliency improvements can be gained through the use of dc power distribution networks in order to decouple propulsion from generation with power electronics [1]–[3] and mitigate the challenges associated with ac synchronization during connection to DERs and re-configuration of energy-flow paths [4]. In such systems, much, and in some cases, *all* of the power and energy supplied from DERs flows through networked PECs that are interconnected via cables in a dc distribution system.

All cabled distribution systems necessarily require protection against interconnected electrical equipment and cable insulation failures and catastrophic events that manifest themselves through both gradual and sudden inception of line-to-line (LL) and line-to-ground (LG) faults. For dc distribution systems, these protective systems present not only a challenge but a major risk due to the lack of standards and experience-based design practices [5], [6]. Microgrids, electrified ships, and More Electric Aircraft (MEA) will have relatively short distribution cable lengths (compared to conventional utility-based ac distribution), large sections of cabled dc distribution, and, generally, a meshed power and energy delivery structure. Depending on the application, implementations may be Low Voltage dc (LVdc) and Medium Voltage dc (MVdc) and distinct protective system solutions are needed spanning the ranges from 300 Vdc to 36 kVdc, with nominal current ratings from 100s to 1000s of amperes.

Any viable protective system must be able to accurately detect, locate and isolate very low impedance, sudden inception LL and LG faults. Fault discrimination sequences should occur with minimal disturbance to the system during and after fault isolation actions. Because these systems are fed by PEC-based DERs, a race condition occurs between the time it takes for fault isolation and the time before PECs, which are needed to stay online for system recovery, shut down from internal self-protective actions. The fault during inception is characterized by high di/dt second order response(s) between cable inductance(s) and parasitic LG capacitance(s) or inline PEC filter capacitance(s) [7]. High di/dt fault currents must be arrested within micro-seconds or milli-seconds (depending upon system size, rating and architecture) through either solid-state circuit breakers (SSCBs), with a series fast-acting mechanically isolating no-load switch (NLSw), or through capacitor-discharge inhibiting PEC topologies that coordinate with NLSw distribution panels through high-speed communications. Radially distributed architectures require extremely fast coordination to achieve overcurrent relay capability [8]. Meshed distribution architectures and ring buses will, as a minimum, require high-speed communications between protective devices for protective relaying.

Protective systems design for dc systems is highly developmental design implementations are integral to other design decisions, such as system architectures, PEC topology and energy storage placements and amount. This paper describes the development and validation of a Real-time (RT) simulation, controller hardware-in-the-loop (CHiL) platform, having sufficient capability simulation time resolution for dc system fault characterization and subsequent dc protective design explorations. It is capable of simulating protection devices, distribution networks, PECs and associated controls and communications with sufficient time resolution to understand the impacts of LL and LG fault behavior on design decisions. It has sufficient detail to discover internal PEC control and hardware interactions with single and multiple LL and LG fault scenarios. The CHiL capability enables testing adequate to determine communications latency and test control hardware solutions. This capability is enabled through a Latency-Based Linear Multistep Compound (LB-LMC) RT simulation method, described in this paper. The authors have previously demonstrated the capability of this LB-LMC method, executed in an Xilinx VC707 Virtex-7 FPGA evaluation board, to perform RT simulations of multiple PEC-based meshed distribution networks, including switching frequency behavior, with 50 ns simulation time resolution [9] [10]. The same approach is also suitable for expandable, multi-FPGA hardware platforms, to enable a wide range of system implementations [11].

This paper demonstrates the adaptation of the LB-LMC RT FPGA-based simulation method to fault characterization of PEC-based dc systems and implements the method into a National Instruments (NI) FPGA based hardware platform that is commercially sustainable, adaptable and expandable. The resulting platform enables dc protection design in a RT environment development of protective system requirements and solutions through an integrative CHiL simulation environment. This approach paves the way for exploration integrated control and protection requirements and solutions for emerging LVdc and MVdc applications at the Technical Readiness Level (TRL) 4 level. To achieve this end and provide a framework for future protective system design explorations for dc systems, this paper demonstrates the simulation of LG and LL fault transients and associated DM and CM behaviors in RT with sufficient time resolution, using a case study on a 1.5 MW, 12 kV, ac-to-dc Voltage Source Rectifier (VSR).

II. JUSTIFICATION OF COMBINED RT SIMULATION/CHiL APPROACH

RT simulation of power systems provides an opportunity to advance to higher TRLs [12] when paired with CHiL-based RT controls [13], [14]. Table I describes TRL as applied to power electronics development. Offline simulation can be considered as TRL 3. Examples of TRL 3 can be seen in [7], [15], [16]. Implementing the design into CHiL allows engineers to move from TRL 3 to TRL 4 (or even up to TRL 6) by enabling testing and validation of control schemes in an RT environment on real hardware.

Due to the speed and resolution requirements of LVdc and MVdc protection systems, performing RT CHiL simulations

TABLE I
TRL AS APPLIED TO POWER ELECTRONICS

TRL	Description	Simulation Environment
9	System proven through successful operations.	-
8	System completed and qualified through testing and demonstration activities (ready to procure).	-
7	Demonstration of a system prototype in an operational environment.	-
6	Demonstration of system or subsystem model or prototype in the relevant environment.	CHiL / PHiL
5	Component or breadboard validation in the relevant environment	CHiL / PHiL
4	Component or breadboard validation in a laboratory environment.	CHiL
3	Analytical and experimental critical function and/or characteristic proof of concept.	Offline
2	Technology concepts and/or applications formulated.	-
1	Basic principles observed and reported.	-

to evaluate and validate fault detection, coordination, and isolation schemes in Commercial-off-the-shelf (COTS) systems are limited in scope due to the simulation time step of COTS systems. This results in having to develop laboratory-scale hardware to truly understand the performance of the system. Laboratory-scale, Low Voltage (LV) hardware may also be considered TRL 4, as seen in [17]–[19]. A downside is this approach results in limited test coverage of the protection scheme and inevitable sub-optimal design. Furthermore, once laboratory hardware is built, it is virtually impossible to explore alternative solutions due to the costs involved in such systems.

Additionally, scaling up laboratory hardware to full-scale hardware, requires almost a full, if not a complete, redesign of the protection hardware and controls. However, running a CHiL simulation takes less development time, is safer to run (especially when performing fault protection), and allows for more design exploration. Validating the protection scheme with CHiL allows for more carryover to the full-scale system, which reduces development times and risks when progressing to higher TRLs compared to laboratory hardware. While, from a fault standpoint, there will always be field conditions that cannot be adequately simulated with CHiL, it is reasonable to expect the fault behaviors that can be simulated, and the system response to them, should be explored rigorously in a sandbox environment before committing to hardware.

Examples of CHiL-based dc protection can be seen in [20], [21], but are for High Voltage dc (HVdc) systems with kilometers of cabling or with non-zero fault impedance, which both significantly limit the di/dt of the fault transient. Low Voltage dc (LVdc) and Medium Voltage dc (MVdc) systems have much shorter cable lengths, which significantly increase the di/dt of the fault transient. An extensive review of microgrid CHiL applications is given in [22], but examples of RT CHiL of dc protection are missing.

Next, one could use Power Hardware-in-the-Loop (PHiL) simulation [23] to process to TRL 5 or 6. Examples of dc protection at TRL 5 or 6 can be found in [24]–[27].

Additionally, most COTS RT simulation systems are

meant for testing controls of power electronics to validate differential-mode (DM) behavior, but not necessarily common-mode (CM) nor fault transient behavior. These behaviors are particularly crucial to the design of PEC-based systems. Fault-induced resonant CM voltages dictate LG voltage stresses on the system. Furthermore, multiple LG fault-induced CM circulating currents between non-isolated paralleled converters, and through unintended fault current paths internal to PECs can cause voltage stresses in components within the system at magnitudes greater than twice the rated system voltage (depending upon meshed inter-connection schemes) [28]. Thus, CM and correct grounding must be included in the RT simulation.

To achieve PEC-based distribution system simulations in RT suitable for testing of protective approaches, the RT simulation must be able to simulate:

- 1) Sufficient simulated fault transient resolution to test out the capability of the protective control hardware;
- 2) Accurate simulation of earthed neutral (TT), chassis neutral (TN) and floating (IT) grounding schemes to enable correct LG fault characterization;
- 3) Mixed-mode (MM) DM/CM behavior resulting from PEC network asymmetry and the impacts of controls delays and Pulse-Width Modulation (PWM);
- 4) Ability to perform high-speed Field Programmable Gate Array (FPGA)-to-FPGA communication sufficient for high-speed protective relaying;
- 5) Ability to simulate large networks through plug and play parallel-ability of the RT simulator components;
- 6) Ability to add limitations such as compute and sensor bandwidth, and communication delays, to derive the performance required for protection schemes, controls, and sensors.

Section III describes the limitations of COTS RT simulators for dc application and discusses CHiL solutions. Section IV addresses LG capacitance in dc systems, and their relation to LG faults and RT simulation. Section V provides a summary of the LB-LMC simulation method used, and its implementation in FPGA hardware, which enables RT simulation time steps in the tens of nanoseconds (ns). Section VI discusses NI FPGA platforms for Hardware-in-the-Loop (HiL) RT simulation, and describes the implementation of the LB-LMC solver in NI FPGA platforms. Section VII describes an RT simulation model of a VSR with floating ground and shows CM and fault transient behavior captured at 20 MHz resolution. Section VIII demonstrates fault current transients for an LL fault applied to the dc outputs of common dc bus-interfacing VSR converters captured at 20 MHz resolution in RT, and shows the additional resolution gained with the proposed platform compared to COTS solutions. Lastly, Section IX summarizes conclusions.

III. REAL-TIME SIMULATION FOR DC PROTECTION

Fig. 1 shows a pseudo-quantitative-qualitative curve of CPU and FPGA based RT Simulation platforms, both COTS and LB-LMC versus their circuit size, and their application towards protection. CPU based RT solvers can achieve time steps in the 10's of microseconds (μs) for small systems or

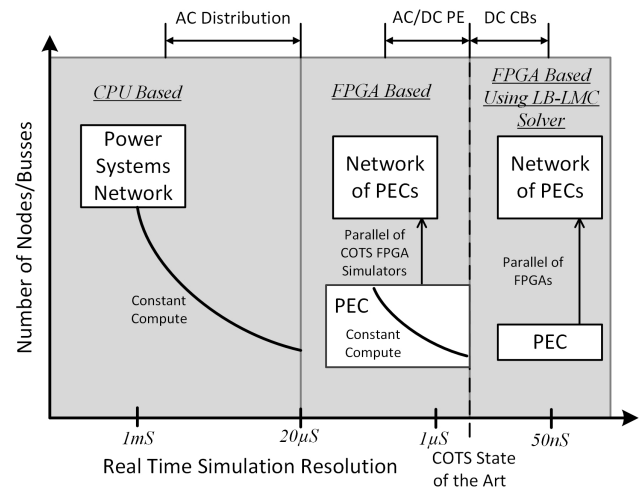


Fig. 1. Real-time simulation resolution vs model size.

milliseconds for large systems. An exponential decay is drawn to represent the trade-off between system size and achievable time step for a given amount of computing. For RT simulation of power systems, power systems faults, and line commutated devices, 10's of μs of simulation resolution is adequate. These solvers can exploit natural time delays in considerable cable lengths to enable parallel computation of larger power systems.

With the introduction of power electronics into electrical distribution systems, higher frequency dynamics such as switching events, harmonics, and passive component dynamics now need to be simulated, and achieving lower time steps smaller than 10's of μs became necessary. However, this became difficult for CPU based RT simulators due to the jitter of the operating systems (OS). The FPGA's inherent ability to parallel computations, reconfigure its hardware for specific circuits, reduction of execution latency, and the lack of required OS, allowed for the hardware improvements needed for RT simulators to achieve lower time steps.

FPGA based RT simulators also have constant compute curves, with time steps ranging from a few hundred ns for minimal systems to 20 μs on the higher end. From the authors' experience, most systems of reasonable size run between 1-4 μs . This range of time steps is sufficient for most power electronic systems. To achieve larger power electronics networks, FPGA based solvers need to be paralleled.

The first step in performing protection design for a distribution system, fault characterization must be performed to determine the differences between fault current at different nodes in the system. The differences in currents between these nodes determine the settings at different breaker locations. A case study was performed for an LVdc residential microgrid in [29]. It was shown, due to the short cabling inductance of the system, the time-trip characteristics between the upstream and downstream breakers were on the order of μs . In [24], MVdc SSCBs were tested for both operation and coordination for MVdc shipboard applications. In the validation of the controls, the author noted an attempt to test operation and coordination in a COTS RT environment. However, in testing fault scenarios

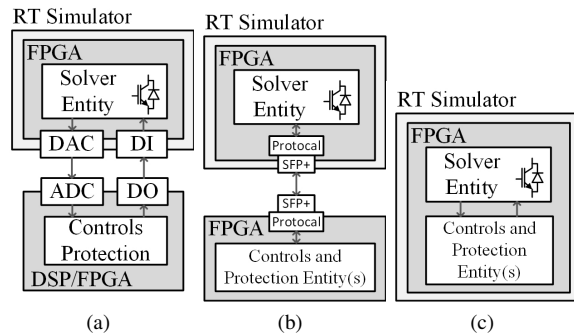


Fig. 2. Controller Hardware-in-the-Loop interfaces between RT Simulator and Controls/Protection Scheme via (a) Analog/Digital IOs, (b) FPGA-to-FPGA Gigabit Serial, and (c) on same FPGA.

with minimum cabling required by the protection system design specification, the time of operations of the SSCB was on the order of a μs , and the RT COTS platform did not have sufficient interface bandwidth capabilities to validate coordination and operation of SSCBs.

In both these examples, and in general, if coordination must occur on the μs time scale, then the simulation must have a time step orders of magnitude smaller than μs to have sufficient resolution to simulate the fault transients. Additionally, the RT simulation platform's interface latency between the simulator itself and the controls or hardware under test must be low enough not to interfere with the testing. For these reasons, COTS platforms did not have sufficient resolution for the tripping and coordination being assessed. LB-LMC RT simulation method can achieve 50 ns time steps on Xilinx 7-series FPGA [9], [10]. For these cases described above, this would have provided enough resolution.

Fig. 2a shows a typical CHiL interface for power electronics. The RT simulator is on an FPGA, and the controls platform is on an FPGA or DSP. The two interface with analog and digital inputs/outputs (IOs). This approach is easy to implement and works if a controller has already been selected for the application. However, if the protection scheme is still being designed/verified, then selecting a controller can limit the design prematurely as the controller requirements such as bandwidth, compute, and signal resolution may be unknown or may not be sufficient. Additionally, the DAC/ADC interface of the controller and RT simulation platform, can limit possible solutions as both have bandwidth and resolution limitations. At the 10's of MHz level, a level required to see the full resolution of a 50 ns RT solver, commercial DAC options that can interface to FPGAs can be limited, either by the number of output channels, price, or ease of implementation.

Fig. 2b shows the controls and RT simulation platform interfacing via a duplex Gigabit serial protocol SFP+ (small form-factor pluggable transceiver) based protocols. These communication protocols can transmit data over fiber optic and is capable of up to 10 Gbit/s per channel (Gigabit Ethernet could also be used). The exact latency can vary, but are generally on the order of a few hundred ns. An advantage of this approach includes no limitation on the number of signals transferring data, nor the resolution of the signals. These settings are up

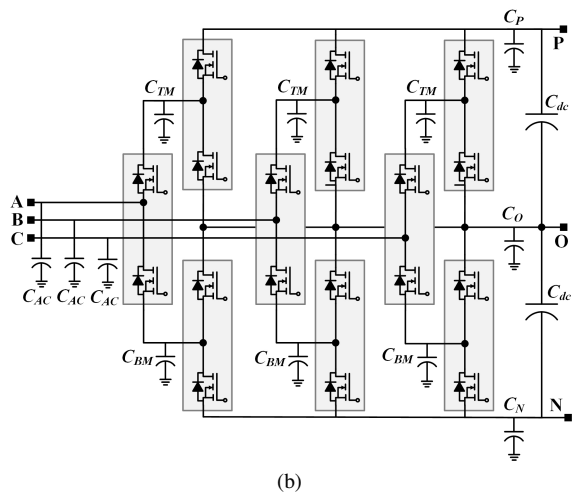
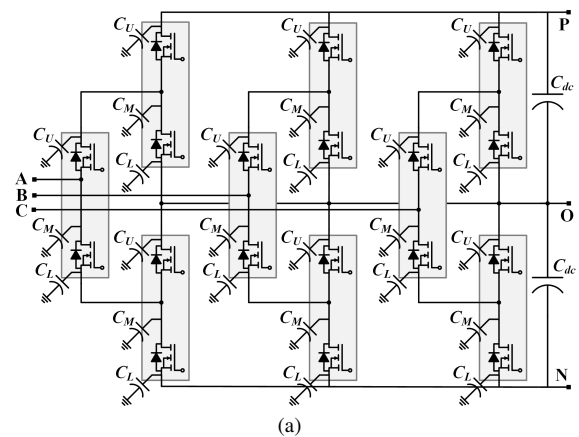


Fig. 3. NPC Converter with baseplate-to-heat sink parasitic capacitances (a) from each module, and (b) simplified.

to the user. The downside of this approach is the user must be proficient in FPGA programming, using the Gigabit protocols, and developed one's own interface on top of the protocol to keep track of signals and their corresponding data.

Fig. 2c shows the solver entity and the protection logic entity on the same FPGA. This approach offers a latency of a few clock cycles between the solver and protection logic. Also, the precision and throughput of signals are limited by the area of the FPGA. This approach removes the downsides of the two methods mentioned above. Another advantage is, once the protection scheme is validated, delays and resolution limitations can be added to determine the amount of compute, allowed latency, and minimum bandwidth. A downside of this approach is that the controls must share FPGA resources with the solver entity. If the power electronic circuit in the solver entity is close to maxing out of one of the resources of the FPGA, then there is not much room to implement the protection scheme. Another drawback is that the FPGA code needs to be recompiled every time.

IV. LINE TO GROUND CAPACITANCES IN DC SYSTEMS

To explore the benefits of this RT simulation approach, an example was chosen of a VSR with a floating (ungrounded) system. Floating grounds or high resistances grounds are used

TABLE II
BASEPLATE-TO-GROUND CAPACITANCE FOR HALF-BRIDGE MODULES

Parameter	CAS120M12BM2	Gen. III Power Module
Device Rating	1.2 kV / 120 A	10 kV / 240 A
Baseplate Dimensions	62 mm x 106 mm	195 mm x 125 mm
Baseplate Area	6,572 mm ²	24,375 mm ²
Area Ratio	1.000	3.709
C_U	191.0 pF	708.4 pF
C_M	255.7 pF	948.4 pF
C_L	102.6 pF	380.5 pF
C_P	(3 C_U)	573.0 pF
C_N	(3 C_L)	307.8 pF
C_O	(3 C_U + 3 C_L)	880.8 pF
C_{AC}	(C_M)	255.7 pF
C_{TM}	(C_U + C_M)	446.7 pF
C_{BM}	(C_L + C_M)	358.3 pF

in mission-critical systems like maritime applications [30] to maintain operability via the LL DM voltage remains constant during a single LG fault. The downside is that ground faults are more difficult to detect due to the much lower, or nonexistent, steady-state fault current compared to hard grounded or low resistance grounded system [31].

Bulk capacitive elements, inductive cabling, and filter drive the fault characteristics in dc power electronics-based systems. For LG faults, the inductive elements of the system are cabling and filters, while the capacitive elements are LG capacitance, which can come from 3 sources:

- 1) parasitic capacitance of the baseplate found in multi-chip power electronic module;
- 2) parasitic capacitance of cabling;
- 3) capacitance of electromagnetic interference (EMI) filters.

A ground fault's characteristics are governed by the equivalent path L inductance and bulk LG capacitance C , which gives a resonant frequency of

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

A. Parasitic Capacitance of a 12 kV NPC

A 12 kV dc bus voltage is a consideration for the MVdc power distribution in shipboard applications [30]. Using a 10 kV / 240 A Silicon Carbide (SiC) MOSFET multi-chip power module in half-bridge configuration [32] and applying 60% voltage and current derating [33] gives 6 kV / 144 A building block. These modules can be configured into a Neutral Point Clamped (NPC) VSR converter to achieve a 12 kV bus. The geometry between the half-bridge module and heat can be represented as three parasitic capacitors at the upper, middle, and lower part of the module, labeled as C_U , C_M , C_L , respectively [34]. Due to lack of availability of the 10 kV power module, the capacitances from a Cree 1.2 kV / 120 A half-bridge module taken from [35], and scaled by the increased area of the module's baseplate, and are tabulated in Table II. Fig. 3a shows a 3 phase NPC converter made

of multi-chip power module half-bridges and the parasitic capacitances. The capacitances can be added in parallel, as shown in Fig. 3b. Table II tabulates these values.

B. Parasitic Capacitance of Cabling

To determine the parasitic capacitance of cabling, some assumptions need to be made about the current and insulation rating. The current rating of the cable is assuming to be the output current rating of the power converter. Given a 3 phase, 6 kVac LL RMS input voltage, and 144 A RMS input current, the input power is about 1.5 MW. A 12 kV dc output at 1.5 MW gives an output dc current of 125 A. Assuming a current density of 3.76 A/mm² for copper cable [36], gives an area of 33.24 mm². Using a 35 mm² single-core, copper cable with polyethylene (XLPE) insulation, conformed to IEC 60502 from [37], the capacitance, inductance and resistance per meter can be found. Table III tabulates these values for different cable lengths and insulation ratings. (1) calculates the resonant frequency of the cable. Dividing the resonant simulation time step by the resonant period gives the amount of simulation time steps per resonant period. The COTS platform assumes a time step of 1 μ s or a frequency of 1 MHz, and the LB-LMC solver assumes a time step of 50 ns, or a frequency of 20 MHz. Columns 6-8 of Table III tabulate these values.

The question then becomes what constitutes as *sufficient resolution*? The resolution of the RT platform should be sufficiently greater than the dynamics of the circuit such that the resolution of the RT simulation does not interfere with the protection solution design, nor drive the design requirements. A conservative amount of samples could be said to be 100. Using the LB-LMC method, the shortest cable length a ground fault would be simulated in RT with sufficient resolution would be 50 m. Using a COTS platform, at 50 m of cabling, there would only be 4-5 samples period, which would be insufficient for any design. For this particular cable, 1 km of cabling is required to achieve 100 time steps per period during an LG fault. With a 20x reduction in time steps, 20x shorter cable lengths can be simulated in RT.

The lengths of potential dc applications are shortening. In essence, the length of a Boeing-777 or Airbus A340 is around 70-75 meters, a US Navy Zumwalt-class destroyer is 183 meters, and a city block varies from 80 to a few hundred meters. The length of the transportation system or microgrid is not an exact unit of measure, but helps to provide an intuition for cable length. Thus, for these emerging applications, cable length will be in term of tens to few hundreds of meters, as opposed to kilometers cabling. The shorter cable length means the LB-LMC solver enables RT simulation of dc protection with *realistic cable lengths* for shipboard, MEA, and microgrid applications. At the same time, the COTS solution is suitable for cable length greater than 1 km for this particle cable.

C. EMI Filter

For this active rectifier, an LC CM filter was used. During an LG fault, the LG capacitors can discharge. However, with an LG fault occurring on the dc side, the current discharging from the CM capacitors are limited by the CM inductor. If an

TABLE III
IEC 60502 SINGLE CORE 35mm^2 COPPER CABLE PARAMETER FOR VARIOUS LENGTHS, CL RESONANT FREQUENCIES, AND TIME STEP PER RESONANT PERIOD IN COTS AND LB-LMC SOLVERS.

Cable Length [m]	V_{LN}/V_{LL} [kV]	Resistance [$\mu\Omega$]	Capacitance [pF]	Inductance, Flat Spaced [nH]	Resonant Frequency [kHz]	Time Steps per Resonant Period	
						COTS (1 MHz)	LB-LMC (20 MHz)
25	3.6 / 6	1,175	15,675	12,000	367.0	2.73	54.50
	6 / 10	1,175	14,025	12,250	384.0	2.60	52.09
	8.7 / 15	1,175	10,975	12,500	429.7	2.33	46.54
	12 / 20	1,175	9,250	12,750	463.4	2.16	43.16
50	3.6 / 6	2,350	31,350	24,000	183.5	5.45	109.00
	6 / 10	2,350	28,050	24,500	192.0	5.21	104.17
	8.7 / 15	2,350	21,950	25,000	214.8	4.65	93.09
	12 / 20	2,350	18,500	25,500	231.7	4.32	86.31
100	3.6 / 6	4,700	62,700	48,000	91.7	10.90	218.00
	6 / 10	4,700	56,100	49,000	96.0	10.42	208.35
	8.7 / 15	4,700	43,900	50,000	107.4	9.31	186.18
	12 / 20	4,700	37,000	51,000	115.9	8.63	172.62
250	3.6 / 6	11,750	156,750	120,000	36.7	27.25	545.01
	6 / 10	11,750	140,250	122,500	38.4	26.04	520.87
	8.7 / 15	11,750	109,750	125,000	43.0	23.27	465.44
	12 / 20	11,750	92,500	127,500	46.3	21.58	431.55

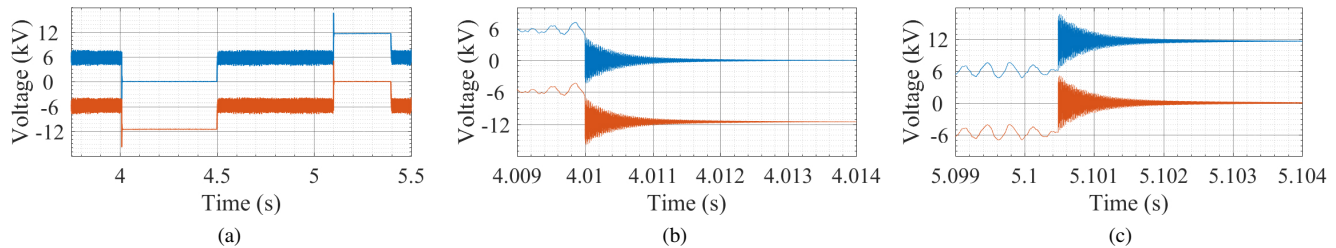


Fig. 4. Offline PLECS Simulation of NPC based VSR: (a) +LG and -LG fault, (b) +LG zoomed, and (c) -LG zoomed

LG fault occurs on the ac side, the fault current contribution of the CM capacitors may be more significant since the CM inductor would not shunt the current. Thus, the placement of EMI filters within the system should be considered in terms of fault current.

D. Offline Simulation of Ground Faults

Fig. 12 shows the VSR circuit simulated in Simulink 2017a 64-bit with PLECS v4.3 blockset, but with the NPC from Fig. 3b. Baseplate-to-heatsink capacitances were used from the Table II, filter parameters from Table IV, and switch parameters from [32]. A positive line-to-ground (+LG) fault and negative line-to-ground (-LG) fault were applied.

When modeling cabling parasitic and performing dc faults, a T model should be used. If a π model were used, then the fault would be applied directly to the parasitic capacitor. Resistors were added in series to the baseplate-to-heatsink capacitances to damping out any resonate simulation artifacts and are used to help set the lower bound of the simulation dynamics when using a variable time step solver.

Fig. 4a shows the dc LG transient voltages from applying +LG and -LG faults. Zoomed views are showing for +LG and

-LG in Fig. 4b and 4c, respectively. As will be seen in Section VII, for RT simulation, this capacitance can be lumped at the midpoint of the dc link to ground to allow for similar fault behavior. Discussion on LG faults in IT systems is carried out in Section VII as well.

V. LB-LMC SOLVER FPGA IMPLEMENTATION

This section provides a brief summary of the LB-LMC simulation method and FPGA implementation used within the proposed approach. A full description and analysis of the LB-LMC method is given in [9] [38] which contains details of the method not presented here, such as stability analysis, computational considerations, and further comparison to traditional simulation methods. Also, a summary of the FPGA implementation is provided and a full description can be found in [9] [10].

A. LB-LMC Method Summary

The LB-LMC method [9] [38] is a transient simulation method for solving of power electronic and generation systems with nonlinear, multi-physics elements. Similar to Electro-Magnetic Transient Program (EMTP) and other Resistive

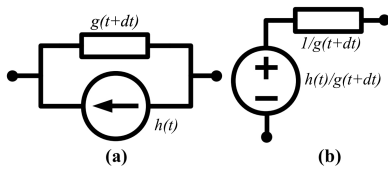


Fig. 5. LB-LMC Component Models; (a) component with current state, (b) component with voltage state

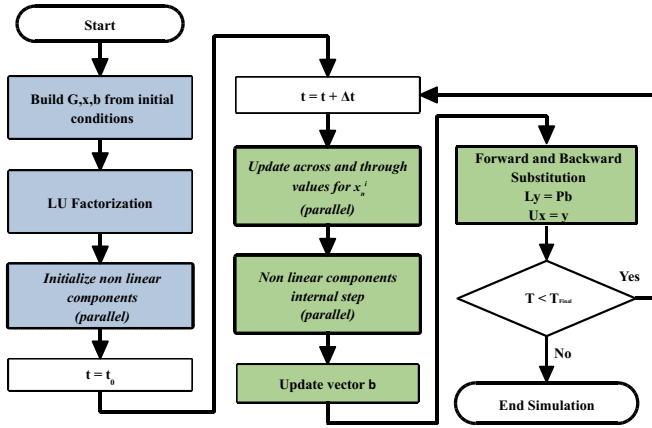


Fig. 6. LB-LMC Solution Flow

Companion (RC) based methods, a given network system under LB-LMC method is defined as a linear set of equations $Gx(t + dt) = b(t)$ for each simulation time step where $x(t + dt)$ is a vector of system solutions at $t + dt$, $b(t)$ is a vector of source contributions solved from linear or nonlinear discretized state equations of components in the system, G is the system conductance and incidence matrix derived from state equations of the components, and dt is fixed length of the time step in seconds. For every time step under the method, these set of equations are solved for $x(t + dt)$ by updating $b(t)$ from (non-)linear state equations and then solving the set by applying numerical linear algebra approaches such as LU factorization or matrix G inversion ($x = G^{-1}b$).

Unlike EMTP and other RC methods, computational cost for solving systems with nonlinear components is significantly reduced by keeping the G term constant and avoiding iterative solving (i.e. Newton-Raphson) often used for nonlinear systems. This setup is achieved by having nonlinear component state equations be discretized using explicit integration, such as Euler Forward or Runge-Kutta methods [39], so that nonlinear equations have no nonlinear variable terms to be updated each time step for G and thereby avoid iterative solving; this topic is elaborated in Subsection V-B.

B. Component Modeling

The LB-LMC method expresses each component of a system as a combination of Resistive Companion (RC) models as depicted in Fig. 5. These RC models are derived from each discretized, zero or first order state equation of an electrical component which can be generally expressed in the form of (2):

$$I(t+dt) = g(t+dt)V(t+dt) + h(x(t), I(t), V(t), u(t)), \quad (2)$$

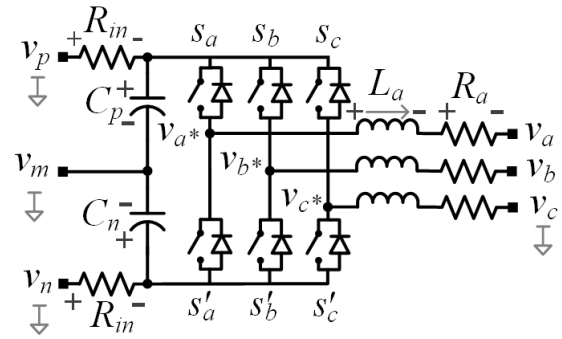


Fig. 7. Voltage Source Converter component in LB-LMC

where $I(t + dt)$ and $V(t + dt)$ are the present through-current and across-voltage of a state element, respectively, h is a current term derived from past states (V, I, x) and inputs u , and $g(t + dt)$ is a conductance that relates V and $I - h$ at $t + dt$. Following classic nodal methods, $g(t + dt)$ is aggregated into matrix G while $h(t)$ is aggregated into $b(t)$ of a system's set of equations.

Linear component state equations are discretized with implicit integration methods [39], such as trapezoidal method, typically providing for fixed linear $g(t + dt)$ for all t , allowing the matrix G to also stay constant. Nonlinear components, on the other hand, are discretized with explicit methods [39], which leads the typical nonlinear variable $g(t + dt)$ term of (2) to equal zero and keeping G untouched. For a single, current-based nonlinear state component discretized with the explicit method Euler Forward, (2) will take the general form of (3) which can be readily solved without iterative approaches.

$$I(t + dt) = h(t) = I(t) + f(t, \dot{I}(t), u(t)) \quad (3)$$

For switching PECs, as presented in this paper, the components are modeled in the same way as other components using state space model equations. Since these converters have switching elements, they are considered nonlinear and therefore their equations are explicitly discretized and RC models of only sources are defined from said equations to be embedded into the overall system's $Gx = b$.

Fig. 7 shows a 3-leg Voltage Source Converter (VSC) component used in Sections VII and VIII. Each power electronic device with anti-parallel diode is modeled as a single ideal switch with an on-state resistance of R_{sw} , and will be referenced to as a "switch" for modeling purposes. Additional logic is added to enable correct behavior of the anti-parallel diodes in the VSC component model. Fig. 7 also shows the signals used in the component's state space model. The state space model of the VSC has 5 states equations: 2 for the upper (C_p) and lower (C_n) capacitors, shown in (4) and (5), respectively, and 3 for each leg inductor (L_j), shown in (6), where $j \in \{a, b, c\}$ for each respective phase-leg.

$$\dot{v}_{cp} = \frac{v_p - v_{pm}}{C_p R_{in}} - \frac{1}{C_p} \left(\sum_j s_j i_{swj} \right) \quad (4)$$

$$\dot{v}_{cn} = \frac{v_n - v_{nm}}{C_n R_{in}} - \frac{1}{C_n} \left(\sum_j s'_j i'_{swj} \right) \quad (5)$$

$$\dot{i}_{Lj} = \frac{1}{L_j} (v_{*j} - v_j - R_j i_{Lj}) \quad (6)$$

Switching functions are embedded in the VSC state space equations to handle the different switching states for the upper (s_j) and lower (s'_j) switches within each j th leg. Depending each switch's conduction state,

$$s_j = \begin{cases} 1 & \text{if upper switch ON} \\ 0 & \text{if upper switch OFF} \end{cases}$$

$$s'_j = \begin{cases} 1 & \text{if lower switch ON} \\ 0 & \text{if lower switch OFF} \end{cases}$$

Upper switch currents (i_{swj}) and lower switch currents (i'_{swj}) are given as:

$$i_{swj} = \frac{v_{pm} - v_{*j}}{R_{sw}} \quad (7)$$

$$i'_{swj} = \frac{v_{nm} - v_{*j}}{R_{sw}} \quad (8)$$

where $v_{pm} = v_m + v_{cp}$, $v_{nm} = v_m + v_{cn}$, v_{*j} is the midpoint leg voltage given by

$$v_{*j} = \frac{s_j v_{pm} + s'_j v_{nm}}{k_j} - \frac{R_{sw}}{k_j} i_{Lj} \quad (9)$$

and k_j is

$$k_j = \begin{cases} 1 & \text{if upper OR lower switch ON} \\ 2 & \text{if upper AND lower switch ON} \end{cases}$$

The VSC component is integrated with Euler Forward [39], as shown in (10).

$$x(t + dt) = x(t) + dt \cdot \dot{x}(t) \quad (10)$$

When $x(t)$ is a current term, as is the case for the inductors at each leg, $h(t) = x(t + dt)$. When $x(t)$ is a voltage term, as in the case for the dc-link capacitors, the Norton equivalent is used to derive the current term, as shown in (11).

$$h(t) = \frac{v_{cp/n}(t + dt)}{R_{in}} \quad (11)$$

where $v_{cp/n}(t + dt)$ is the upper or lower voltage of the dc-link capacitors, respectively, and are integrated with (10).

C. Solution Flow

Fig. 6 shows the solution flow at every time step under LB-LMC simulation method. Before the start of simulation, the system of equations $Gx = b$ and its initial conditions are defined from the RC elements of the components. Then, the simulation goes online, beginning each simulation time step with the solving for component states entirely in parallel to update RC source contributions. Once source contributions

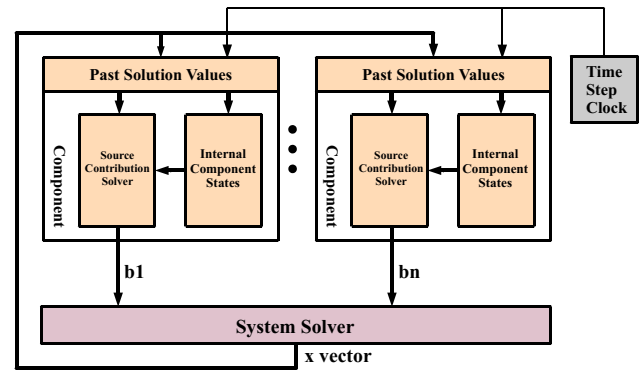


Fig. 8. LB-LMC Solver Engine

are updated, they are aggregated into vector b and the system solutions x are solved from $x = G^{-1}b$. Afterwards, a new time step is executed, should the simulation continue, using solutions from past time step.

D. Component and System Solver Cores

The scheme for the FPGA design of the LB-LMC solver engine is depicted in Fig. 8. Each component of the system to be solved in this scheme is encapsulated as a dataflow execution unit. Within each time step, these units take relevant input signals, their past states, and past system solutions to compute their RC source contributions that are to be aggregated into vector b . To solve the system for solutions x , a system solver unit is defined that takes, as input, the updated vector b and outputs x . All execution units within the solver engine use fixed-point arithmetic instead of floating point to significantly reduce computational cost of FPGA resources and execution latency. This enables the achievement of RT simulation of large system models with very small time steps.

E. Execution Scheduling

The LB-LMC solver engine execution is scheduled using a periodic RT system clock signal provided by the FPGA platform loaded with the engine. Executing in a parallelized dataflow manner, the solver engines updates each time step within a single execution clock cycle, with the rising edge of the clock triggering each time step. To achieve RT execution, the system clock is set to have its period equal to the simulation time step. As seen in [9] [10], the LB-LMC FPGA solvers are capable of executing in RT with ≤ 50 ns time steps.

VI. NI FPGA PLATFORM FOR REAL-TIME SIMULATION AND SOLVE DEVELOPMENT FLOW

This section provides a discussion on how RT simulation can be performed on NI FPGA-based platforms using the LB-LMC solver engines, and how RT LB-LMC solver engine for a power electronic system is developed and then incorporated into a NI platform application. Further material on this subject can be found in [40].

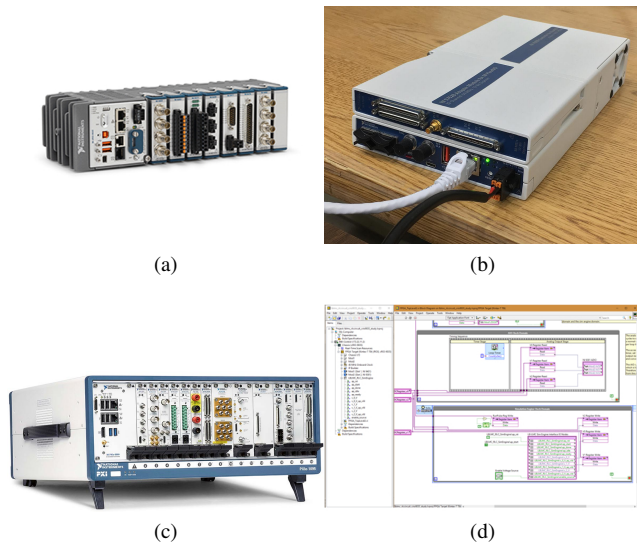


Fig. 9. NI CPU+FPGA Platforms: (a) CompactRIO, (b) Controller for FlexRIO, and (c) PXIe Chassis; (d) LabVIEW FPGA Software.

A. National Instruments Platforms and LabVIEW

NI is a manufacturer of widely used computing and instrumentation platforms often applied in system automation, testing, and control. Within NI's line of products are many FPGA+processor based computing platforms with modular and numerous analog and digital IO capabilities. Such platforms include the CompactRIO, FlexRIO, and PXIe series of products, as depicted in Fig. 9. These platforms often incorporate ARM or x86 (Intel Core i and Xeon) based processors with Xilinx FPGAs such as Kintex-7, Kintex Ultrascale, and Zynq devices. Because these platforms are capable of CPU+FPGA architectures and IO options, RT simulation, HiL testing, and CHiL can be conveniently performed entirely on these platforms. To handle RT simulation, the LB-LMC solver engines can be implemented on the FPGA portions of the NI platforms.

To provide for convenient programming and rapid prototyping, NI platforms utilize LabVIEW, as depicted in Fig. 9d. NI LabVIEW is a graphical software development and hardware configuration application where CPU software, FPGA logic designs, and hardware IO interfacing are developed in graphical signal flow like diagrams called virtual instruments (VI). Multiple VIs can be incorporated together within a single application for NI platforms, with the VIs executing on respective CPU or FPGA portion of the platform. As a result, custom FPGA design cores can be incorporated into FPGA VIs for NI platforms. LabVIEW provides for FPGA core encapsulation to allow these cores to be loaded onto the NI platforms and interface with other logic implemented within the VIs. This FPGA core encapsulation is applied to allow LB-LMC solver engines to execute on NI platform FPGA devices and interact with VIs and IO hardware for HiL testing, control, and networking.

B. LB-LMC Solver Engine Encapsulation

To allow LB-LMC solver engine FPGA cores to run on NI platforms and interface with VIs, these cores are encapsulated into Component Level Intellectual Property (CLIP) core objects that are incorporated into LabVIEW applications, depicted in Fig. 10a. Utilizing CLIP objects, the LB-LMC solver engines execute independently from FPGA/CPU VIs and IO hardware running on the same NI platform. The LB-LMC solver engine, through CLIP encapsulation, can operate with its own clock frequency, data rate, and timing in comparison to VIs and IO hardware, allowing the core to execute appropriately for RT execution. For the solver engine CLIP core to interface with VI logic and I/O, IO node block elements are included in the FPGA VIs, and these blocks are assigned to signal ports of the said core such as simulation solutions and execution status/control signals. From these IO node blocks, signals in VIs can be passed to and from the LB-LMC solver engine CLIP core.

C. Execution and Interface Scheduling

As the LB-LMC solver engine cores execute each time step within a single clock cycle in RT, signal interfacing between the core and VI logic through the IO node blocks must follow the same execution scheduling to stay synchronized to avoid data loss or error. To have the data access to the solver engine core synchronized to the single-cycle scheduling, an Single-Cycle Timed Loop (SCTL) structure in LabVIEW can be applied, as depicted in Fig. 10b. Any VI logic contained within a SCTL structure is executed within a single clock cycle, with the structure configured to be driven by a clock signal selected within the given NI platform. For synchronous data access to the LB-LMC solver engine CLIP object, the assigned IO node blocks are inserted into an SCTL structure driven by the same clock used to drive the solver engine. Then, data can be routed in or out of the SCTL structure to other logic of given VI. If data through the SCTL is accessed outside the SCTL by logic that is operating in different clock (frequency, phase) or data rate (single or multi-cycle) domain, then further synchronization logic is needed to move data between domains safely in a VI without loss or error.

D. Data Synchronization Between Clock Domains

As a result of the LB-LMC solver engine cores running at clock rates to operate in RT, for given time step that can differ from the clock rates used to drive VI logic or IO hardware, synchronization mechanisms may be required to safely pass data between the solver and other logic running on a given NI platform. To provide data synchronization across domains, LabVIEW natively supports various mechanisms such as First-In-First-Out (FIFO) buffers, synchronized registers and global variables, handshaking systems, and more. A straightforward approach to synchronize data between the solver engine core's clock domain and that of VI logic within another domain is the use of the synchronized registers, as shown in Fig. 10c. With this mechanism, a data register with associated read/write node blocks are inserted into a VI, with each node block

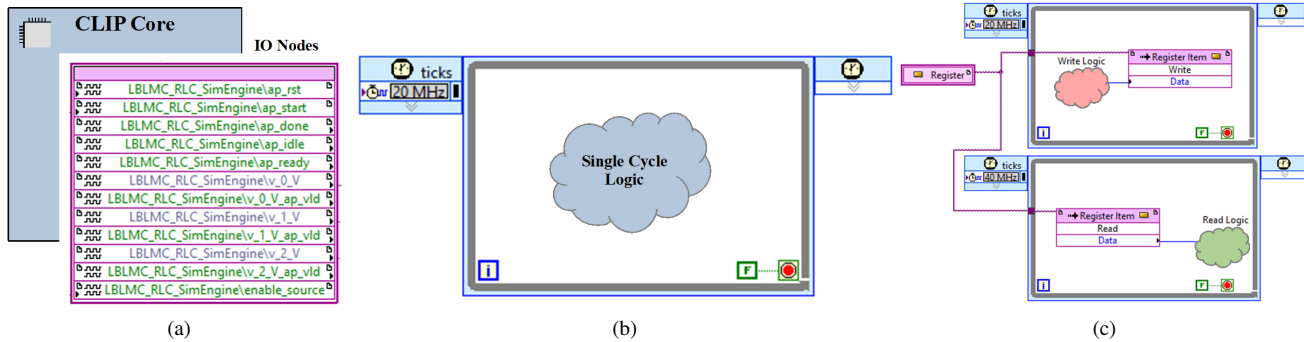


Fig. 10. LabVIEW Simulation Setup: (a) CLIP core with IO Nodes, (b) Single Cycle Timed Loop (SCTL), and (c) Clock Domain Synchronization between Resources with Registers.

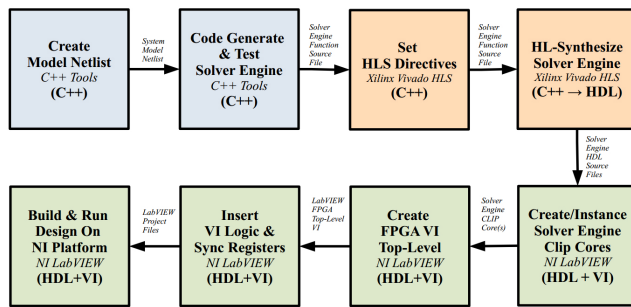


Fig. 11. LB-LMC NI Platform Solver Engine Development Flow

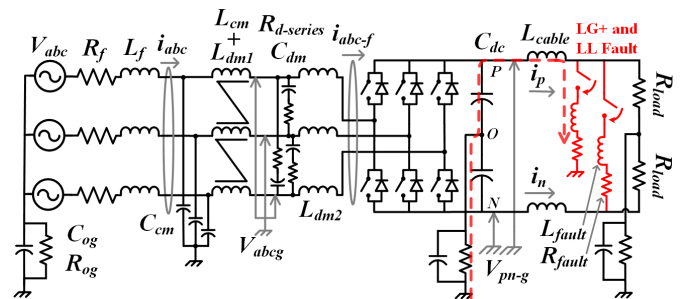


Fig. 12. VSR Circuit with LCL DM filter, LC CM filter, floating ground, measurement points, +LG and LL faults. +LG fault path in light dashed red line.

inserted into the associated domain (or SCTL) and then used to pass data between domains. During compilation or FPGA synthesis of VI, LabVIEW will automatically provide internal logic to synchronize the register access between the domains safely. Due to this internal synchronization, between one to three cycles of data latency in the receiving clock domain is inserted into the data path, depending on the clock rate of the two different domains communicating data.

E. NI FPGA Platform Solver Development Flow

Fig. 11 shows the development flow for creating an LB-LMC solver engine FPGA core and including it into a NI platform. The first step involves defining a netlist for the power electronic system to be simulated, which can be defined directly in C++ language or as a plain-text file. This netlist is then fed through a custom C++ code generation system, presented in [41] and available at [42], which generates optimized C++ source code for the LB-LMC solver engine tailored to the modeled system. This source code is then passed to a high-level synthesis (HLS) tool, such as Xilinx Vivado HLS, which converts the C++ code automatically to code in a hardware description language (HDL; such as VHDL or Verilog) that defines the FPGA core for the solver engine. The FPGA timing, resource usage, and latency requirements for the solver engine core are set using HLS directives given to the tools. With the solver engine FPGA core developed, the core can then be incorporated into a LabVIEW application project. The HDL code of the solver engine core is passed to LabVIEW's CLIP core wrapper helper tool which is used to define the

CLIP object for the core as well as the corresponding clock, signal port data types, and IO node blocks that will be used in LabVIEW FPGA VIs to access the core. With the CLIP object of the solver engine defined, the CLIP object can be incorporated into a LabVIEW project for a given NI platform and interfaced with FPGA VIs that access the CLIP object through the IO node blocks. Logic for HIL testing, control, and IO hardware interfacing can be included directly into the FPGA VIs or be spread across both CPU and FPGA VIs, depending on application design and requirements along with chosen NI platform. If necessary, synchronizing logic, such as registers and FIFOs, are included to pass data safely between the solver engine and other logic. Once the VIs and LB-LMC solver engine CLIP object of an application are created and configured, they can be built (compiled or FPGA synthesized) and then loaded onto chosen NI platform to perform its application (HIL testing, etc.).

VII. REAL-TIME SIMULATION OF COMMON-MODE AND +LG FAULT IN AN UNGROUNDED DC SYSTEM

Fig. 12 shows a VSR with LCL DM filter and LC CM filter and measurement points referred to throughout the paper. The VSR regulates the dc bus voltage to 12 kV. The source is modeled as an ideal 3-phase voltage source of 6 kV_{LL} RMS with a feeder cable. The controls utilize decoupled voltage oriented controls in the rotating dq frame [43].

Fig. 13 shows a block diagram of the top level VI implemented in LabVIEW FPGA. The hardware used was NI

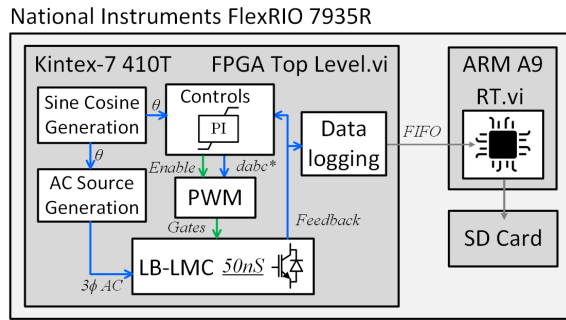


Fig. 13. Block diagram of top level VI in LabVIEW FPGA.

TABLE IV
VSR PARAMETERS

Parameter	Description	Value	Unit
Vdc rated	V_b	12	kV
ac source, V_{LL} RMS	V_{abc}	6	kV
ac source, Frequency	f_e	60	Hz
Switching Frequency	f_{sw}	6.25	kHz
Feeder Cable, Resistance	R_f	0.198	Ω
Feeder Cable, Inductance	L_f	1.8	mH
CM Filter, Inductors	L_{cm}	60	mH
CM Filter, Capacitors	C_{cm}	0.1	μF
DM Filter, Inductor 1	L_{dm1}	0.955	mH
DM Filter, Inductor 2	L_{dm2}	5.6	mH
DM Filter, Capacitor	C_{dm}	16.652	μF
DM Filter, Damping Resistor	$R_{d-series}$	55.1822	Ω
dc Link Capacitance	C_{dc}	20	mF
Cable Inductance	L_{cable}	10	μF
Resistive Load	R_{load}	100	Ω
Floating Ground, Capacitance	C_{og}	0.1	μF
Floating Ground, Resistance	R_{og}	10	k Ω
Fault Inductance	L_{fault}	10	μH
Fault Resistance	R_{fault}	1	m Ω

FlexRIO, model number NI-7935R (Fig. 9b), which contains a Kintex-7 410T FPGA where the LB-LMC solver, controls, and PWM are implemented. Sine and Cosine lookup tables are used to generate the necessary angles for power-variant dq and dq^{-1} transforms used in the controls, and for the 3 phase ac mains input signals to the LB-LMC solver. Registers are used to cross clock domains between the lookup tables, controls and LB-LMC solver. For data logging, LabVIEW FPGA utilized Direct Memory Access (DMA) FIFOs to transfer data between the FPGA and ARM processor. Then, the ARM processor saves the data to an SD card. Due to limitations in data logging ability, longer time data capture occurs at lower resolutions, and the shorter time captures use higher resolution.

IT grounding is modeled with a capacitor (C_{og}) and resistor (R_{og}) in parallel to ground, with values of 0.1 μF and 10 k Ω , respectively. This represents the parasitic capacitance in an ungrounded system [44]. The parallel resistor R_{og} is present to ensure the bus voltages returns to initial conditions. Changing this resistance affects how long the bus voltage takes to recover after a fault is removed, governed by the RC time constant of R_{og} and C_{og} . A list of circuit parameters can be found under Table IV.

The 2 level, 3 phase VSR produces CM voltage of $\pm V_{dc}/2$, and $\pm V_{dc}/6$ depending on the switching state [45]. With a

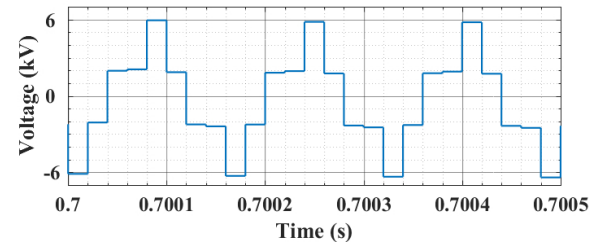


Fig. 14. CM Voltage at V_{abcg} . Data is captured at 50 kHz.

12 kV bus, the CM voltage outputs are ± 6 kV and ± 2 kV, as seen in Fig. 14. This leads to CM currents, as seen at measurement point i_{abc_f} in Fig. 15a. The CM current is reduced after passing through the CM LC filter, Fig. 15b. This shows the LB-LMC solver is able to simulate CM currents and CM filters correctly.

During an LG fault in an ungrounded system, the DM voltage remains constant while the CM shifts [46]. In normal operation, positive Vdc rail to ground (V_{pg}) is +6 kV, and negative Vdc rail to ground (V_{ng}) is -6 kV, giving a DM voltage (V_{dcDM}) of 12 kV. Applying a +LG fault on the positive dc rail forces the positive rail to zero volts. The ungrounded system will keep the 12 kV V_{dcDM} , and shift the negative rail to -12 kV. All the non-electrically isolated parts of the distribution system will shift voltages, including the ac-side LG voltages (V_{abcg}) as shown in Fig. 16a. Fig. 16e and Fig. 16b shows V_{dcDM} and ac-side DM (V_{abcDM}) voltage remains constant during the fault, respectively. While the CM dc (V_{dcCM}) and ac (V_{abcCM}) Voltages shift, as seen in Fig. 16f and Fig. 16c, respectively. This behavior is characteristic of an IT system during LG faults, and shows correct behavior in RT simulation. When the fault is removed, the voltage will return to nominal.

Fig. 12 shows the path of current during an LG fault in the light red dashed line, which forms an equivalent under-damped LC circuit with a resonant frequency of (1). Since C_{og} is in series with much larger dc-link capacitors (C_{dc}), C_{dc} can be ignored. C_{og} represents the lumped sum of cabling capacitance and baseplate-to-heatsink capacitance. Parameters of 20 μH and 0.1 μF give a resonant frequency of 125.4 kHz or a period of 8.89 μs , where this period equates to 100 m cable from Table III. With COTS RT platforms executing at 1 μs time steps, this results in less than 9 samples per period, which is a poor resolution when trying to characterize fault transients to design protection schemes with it.

This under-damped response causes a transient voltage on the dc bus, shown in Fig. 17a via V_{pg} and V_{ng} . V_{pg} 's overshoot peaks around -5kV, and V_{ng} 's overshoot peaks at about -17 kV. This large swing in voltage could exceed the isolation rating of the power electronics module and stress cable insulation. Similar voltage transients can be expected if a -LG fault was applied, just with the opposite voltage direction. Transient peaks in Fig. 16a and Fig. 16i are missed due to the lower sampling resolution of the larger time capture.

The CM dc current (i_{dcCM}) transient is shown in Fig. 17b. If the cable length increases, the transient will increase

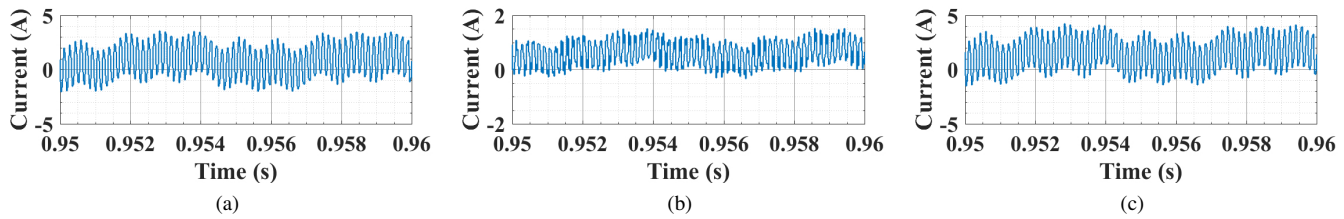


Fig. 15. VSR CM current at (a) $iabc_f$ (b) $iabc$ (c) idc . Data is captured at 50 kHz.

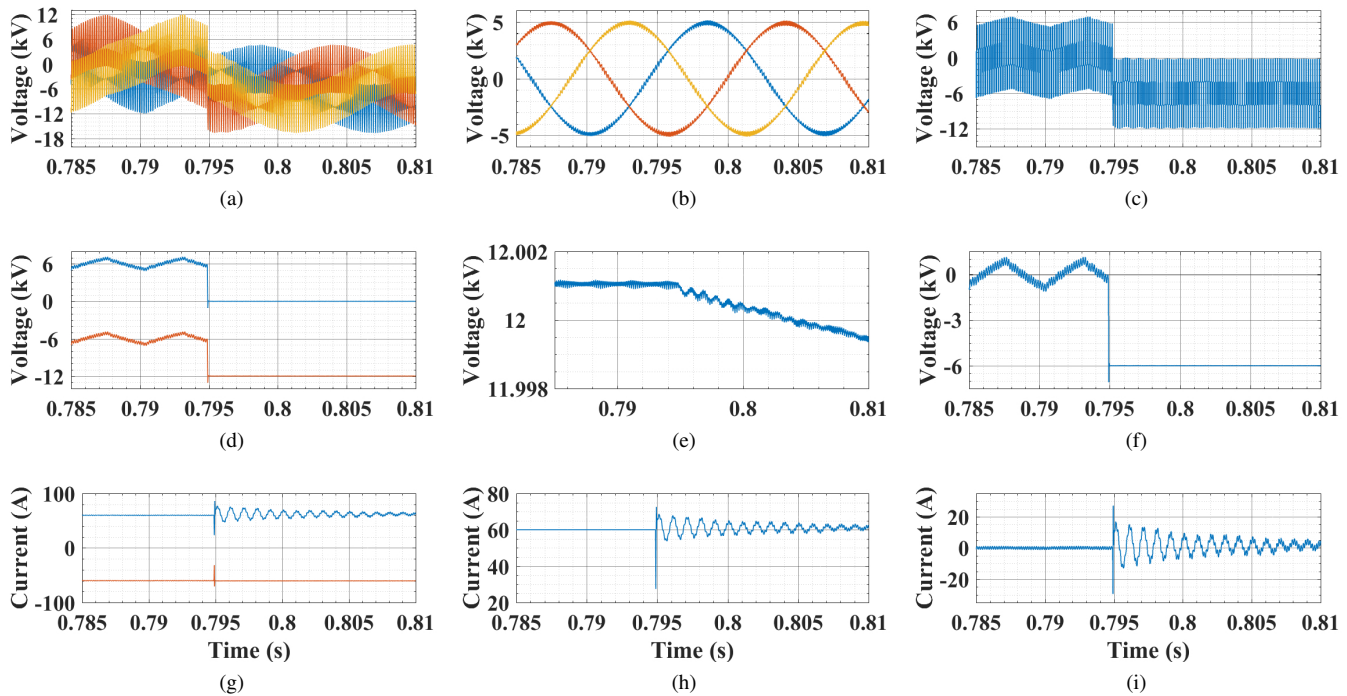


Fig. 16. +LG fault at 0.795 seconds. Data is captured at 50 kHz. Left, Middle and Right Columns are MM, CM, and DM, respectively. $Vabcg$ (a) MM (b) DM (c) CM; $Vpng$ (d) MM (e) DM (f) CM; ipn (g) MM (h) DM (i) CM.

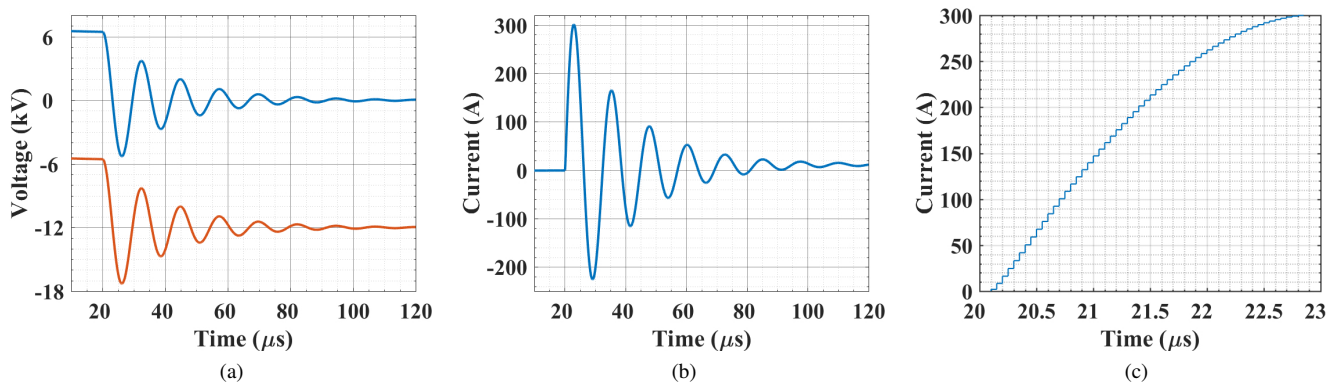


Fig. 17. +LG fault applied at 20 μs . Data is captured at 20 MHz. (a) $Vpng$, (b) idc_{CM} , and (c) idc_{CM} zoomed.

in period and decrease in amplitude. The significance of the idc_{CM} waveform is in a real implementation of power converters in a floating system. The LG voltage measurement may not be viable, leaving only the idc_{CM} transient for ground fault detection and location. For example, one could use high

bandwidth Rogowski coil spread through the network, paired with Wavelet analysis do help detection and locate ground faults [47].

With LB-LMC's 50 ns time step, this example simulates the transient waveform with 177 data points. The resolution of the

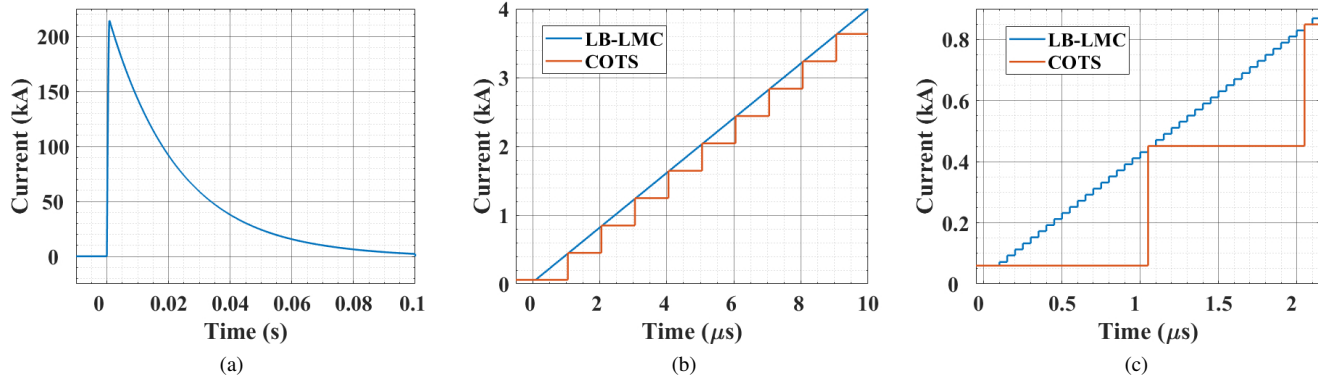


Fig. 18. idc_{DM} during LL fault on dc bus showing (a) whole current transient, (b) current transient at fault inception comparing 50 ns resolution enabled by LB-LMC solver, and 1 μ s resolution if run on COTS, and (c) zoomed.

solver can be seen in Fig. 17c. This significantly increases the resolution of the transient, allowing for accurate fault characterization of high-frequency transient, and testing of fault detection and location algorithms for IT systems with short cable lengths.

VIII. REAL-TIME SIMULATION OF DC LL FAULT WITH VSR INTERFACING CONVERTER

Using the circuit shown in Fig. 12, an LL fault is applied on the dc bus. Analytical derivation of VSR under LL faults can be found in [15]. Fig. 18a shows the idc_{DM} transient during an LL fault. The peak is very high and is a function of vdc_{DM} at fault inception and impedance in the fault path. In [17], a peak fault current of 280 A was reached with only a 17 Vdc bus. In [15], LL faults were characterized for a 270 LVdc system for an aircraft application. A peak fault current of several kA was simulated. In [26], a phase-controlled rectifier (PCR) provided power conversion for a 1 kV high power shipboard distribution system. An LL fault was applied to test the fault detection, isolation, and recovery scheme. The fault current reached a peak of 22 kA. For MVdc systems with a bus voltage of tens of kV and fault impedance of m Ω s, peak fault current of tens or hundreds of kA is possible.

The rise in fault current, di/dt , is a critical feature in LL faults, as coordination upstream and downstream protection equipment must occur before the current exceeds the rating of the protection equipment. Therefore, it is vital to have sufficient resolution during this part of the fault transient to enable fault characterization and coordination between different parts of the distribution system. The di/dt is governed by vdc_{DM}/L , where L is the fault path inductance. MVdc systems can have tens of kV and μ H of inductance, which leads to di/dt of hundreds to thousands of A/ μ s [24], [25]. For this simulation, vdc_{DM} is around 12 kV at fault inception, and L is 30 μ H. Fig. 18b shows idc_{DM} reaching 4 kA in 10 μ s, or 400 A/ μ s.

For MVdc systems with such high di/dt , the protection equipment must detect, coordinate, and begin to arrest the fault current on the μ s time scale. Dynamics this is close to the simulation time steps of COTS platforms can be insufficient

resolution during the early design stage and can lead to sub-optimal protection system design.

Fig. 18b shows idc_{dm} at fault inception and compares the 50 ns time steps of LB-LMC with 1 μ s sampling if executed on COTS platforms. Fig. 18c shows the critical information missed between the two platforms.

IX. CONCLUSION

In this paper, the gap between the requirements for RT HiL simulation of dc protection design for LL and LG fault and COTS RT simulation is demonstrated. A detailed analysis is performed of an ungrounded (or floating ground) system where the ground reference is established through LG capacitances, of a 1.5 MW, 12 kV NPC VSR and dc side cabling. It is shown that the parasitic capacitance of the cabling contributes more to the system's aggregate LG capacitance than the LG capacitance of the NPC VSR. It is also shown that the time step of the LB-LMC RT simulator is sufficient for simulation of the impacts of limited cable lengths during LG fault scenarios, which enables fault characterization of much shorter cable lengths when compared with COTS RT solvers.

Additionally, CM voltage and current behaviors are simulated in RT for the 12 kV VSR in an ungrounded system, but any grounding system can be applied. The ungrounded system presents a challenging corner case for RT simulations. As LG faults are applied, the approach emulates overvoltage stresses and CM current transients upon sudden zero-ohm fault applications with a sufficiently high resolution of 50 ns—a level currently not present in the COTS RT simulators. Moreover, superior resolution during LL fault is demonstrated, which will enable the design and coordination of LL fault protection schemes in dc systems. In conclusion, the resultant CHiL system will enable the development of new protective schemes for dc systems where high-resolution data-capture upon fault incidence and subsequent high-speed data processing and communications are necessary.

REFERENCES

- [1] Z. Jin, G. Sulligoi, R. Cuzner, L. Meng, J. C. Vasquez, and J. M. Guerrero, "Next-generation shipboard dc power system: Introduction smart

- grid and dc microgrid technologies into maritime electrical networks,” *IEEE Electrification Magazine*, vol. 4, no. 2, pp. 45–57, 2016.
- [2] J. G. Ciezki and R. W. Ashton, “Selection and stability issues associated with a navy shipboard dc zonal electric distribution system,” *IEEE Transactions on power delivery*, vol. 15, no. 2, pp. 665–669, 2000.
- [3] B. Sarlioglu and C. T. Morris, “More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft,” *IEEE transactions on Transportation Electrification*, vol. 1, no. 1, pp. 54–64, 2015.
- [4] H. Lotfi and A. Khodaei, “Ac versus dc microgrid planning,” *IEEE Transactions on Smart Grid*, vol. 8, no. 1, pp. 296–304, 2015.
- [5] R. M. Cuzner and G. Venkataramanan, “The status of dc micro-grid protection,” in *2008 IEEE Industry Applications Society Annual Meeting*, IEEE, 2008, pp. 1–8.
- [6] S. Beheshtaein, R. M. Cuzner, M. Forouzes, M. Savaghebi, and J. M. Guerrero, “Dc microgrid protection: A comprehensive review,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2019.
- [7] S. D. Fletcher, P. J. Norman, S. J. Galloway, P. Crolla, and G. M. Burt, “Optimizing the roles of unit and non-unit protection methods within dc microgrids,” *IEEE transactions on Smart Grid*, vol. 3, no. 4, pp. 2079–2087, 2012.
- [8] K. Palaniappan, W. Sedano, N. Hoeft, R. Cuzner, and Z. J. Shen, “Fault discrimination using SiC JFET based self-powered solid state circuit breakers in a residential dc community microgrid,” in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2017, pp. 3747–3753.
- [9] M. Milton, A. Benigni, and J. Bakos, “System-level, FPGA-based, real-time simulation of ship power systems,” *IEEE Transactions on Energy Conversion*, vol. 32, no. 2, pp. 737–747, 2017.
- [10] M. Difronzo, M. Milton, M. Davidson, and A. Benigni, “Hardware-in-the-loop testing of high switching frequency power electronics converters,” in *2017 IEEE Electric Ship Technologies Symposium (ESTS)*. IEEE, 2017, pp. 299–304.
- [11] M. Milton, A. Benigni, and A. Monti, “Real-time multi-fpga simulation of energy conversion systems,” *IEEE Transactions on Energy Conversion*, vol. 34, no. 4, pp. 2198–2208, 2019.
- [12] J. C. Mankins, “Technology readiness levels,” *White Paper, April*, vol. 6, p. 1995, 1995.
- [13] M. O. Faruque, T. Strasser, G. Lauss, V. Jalili-Marandi, P. Forsyth, C. Dufour, V. Dinavahi, A. Monti, P. Kotsampopoulos, J. A. Martinez *et al.*, “Real-time simulation technologies for power systems design, testing, and analysis,” *IEEE Power and Energy Technology Systems Journal*, vol. 2, no. 2, pp. 63–73, 2015.
- [14] X. Guillaud, M. O. Faruque, A. Teninge, A. H. Hariri, L. Vanfretti, M. Paolone, V. Dinavahi, P. Mitra, G. Lauss, C. Dufour *et al.*, “Applications of real-time simulation technologies in power and energy systems,” *IEEE Power and Energy Technology Systems Journal*, vol. 2, no. 3, pp. 103–115, 2015.
- [15] S. Fletcher, P. Norman, S. Galloway, and G. Burt, “Solid state circuit breakers enabling optimised protection of dc aircraft power systems,” in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*. IEEE, 2011, pp. 1–10.
- [16] K. A. Saleh, A. Hooshyar, and E. F. El-Saadany, “Hybrid passive-overcurrent relay for detection of faults in low-voltage dc grids,” *IEEE Transactions on smart grid*, vol. 8, no. 3, pp. 1129–1138, 2015.
- [17] S. D. Fletcher, P. J. Norman, K. Fong, S. J. Galloway, and G. M. Burt, “High-speed differential protection for smart dc distribution systems,” *IEEE Transactions on Smart Grid*, vol. 5, no. 5, pp. 2610–2617, 2014.
- [18] N. Geddada, Y. M. Yeap, and A. Ukil, “Experimental validation of fault identification in vsc-based dc grid system,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4799–4809, 2017.
- [19] P. Cairol, R. A. Dougal, and K. Lentijo, “Coordination between supply power converters and contactors for fault protection in multi-terminal mvdc distribution systems,” in *2013 IEEE Electric Ship Technologies Symposium (ESTS)*. IEEE, 2013, pp. 493–499.
- [20] P. Mitra, C. Wikström, N. Johannesson, and T. Larsson, “First real-time implementation of dc grid protection strategy,” 2015.
- [21] R. Bertho, V. A. Lacerda, R. M. Monaro, J. C. Vieira, and D. V. Coury, “Selective nonunit protection technique for multiterminal vsc-hvdc grids,” *IEEE Transactions on Power Delivery*, vol. 33, no. 5, pp. 2106–2114, 2017.
- [22] A. Vijay, S. Doolla, and M. C. Chandorkar, “Real-time testing approaches for microgrids,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 1356–1376, 2017.
- [23] C. S. Edrington, M. Steurer, J. Langston, T. El-Mezayani, and K. Schoder, “Role of power hardware in the loop in modeling and simulation for experimentation in power and energy systems,” *Proceedings of the IEEE*, vol. 103, no. 12, pp. 2401–2409, 2015.
- [24] J. Langston, K. Schoder, M. Sloderbeck, M. Steurer, and A. Rockhill, “Testing operation and coordination of dc solid state circuit breakers,” in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, Oct 2018, pp. 3445–3452.
- [25] R. Schmerda, R. Cuzner, R. Clark, D. Nowak, and S. Bunzel, “Shipboard solid-state protection: Overview and applications,” *IEEE Electrification Magazine*, vol. 1, no. 1, pp. 32–39, 2013.
- [26] M. W. Rose and R. M. Cuzner, “Fault isolation and reconfiguration in a three-zone system,” in *2015 IEEE Electric Ship Technologies Symposium (ESTS)*. IEEE, 2015, pp. 409–414.
- [27] P. Cairol, L. Qi, C. Tschida, V. Ramanan, L. Raciti, and A. Antoniazzi, “High current solid state circuit breaker for dc shipboard power systems,” in *2019 IEEE Electric Ship Technologies Symposium (ESTS)*. IEEE, 2019, pp. 468–476.
- [28] R. M. Cuzner, A. R. Bendre, J. D. Widmann, K. A. Stonger, S. M. Peshman, J. S. Carlton, and J. A. Fischer, “Considerations when diode auctioneering multiple dc buses in a non-isolated dc distribution system,” in *2011 IEEE Electric Ship Technologies Symposium*. IEEE, 2011, pp. 277–282.
- [29] R. M. Cuzner, K. Palaniappan, W. Sedano, N. Hoeft, and M. Qi, “Fault characterization and protective system design for a residential dc microgrid,” in *2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA)*, Nov 2017, pp. 642–647.
- [30] “Ieee recommended practice for 1 kv to 35 kv medium-voltage dc power systems on ships,” *IEEE Std 1709-2018 (Revision of IEEE Std 1709-2010)*, pp. 1–54, Dec 2018.
- [31] J. Mohammadi, F. Badrkhani Ajaei, and G. Stevens, “Grounding the dc microgrid,” *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 4490–4499, Sep. 2019.
- [32] B. Passmore, Z. Cole, B. McGee, M. Wells, J. Stabach, J. Bradshaw, R. Shaw, D. Martin, T. McNutt, E. VanBrunt *et al.*, “The next generation of high voltage (10 kv) silicon carbide power modules,” in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE, 2016, pp. 1–4.
- [33] “Ieee recommended practice for the design and application of power electronics in electrical power systems,” *IEEE Std 1662-2016 (Revision of IEEE Std 1662-2008)*, pp. 1–68, March 2017.
- [34] A. N. Lemmon, R. Cuzner, J. Gafford, R. Hosseini, A. D. Brovont, and M. S. Mazzola, “Methodology for characterization of common-mode conducted electromagnetic emissions in wide-bandgap converters for ungrounded shipboard applications,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 300–314, 2017.
- [35] A. D. Brovont, A. Lemmon, C. New, B. W. Nelson, and B. T. DeBoi, “Analysis and cancellation of leakage current through power module baseplate capacitance,” *IEEE Transactions on Power Electronics*, pp. 1–1, 2019.
- [36] M. McCandless, C. Cooke, J. Chalfant, C. Chrysostomidis, A. Colavitto, A. Vicenzutti, A. Contin, and G. Sulligoi, “Thermal analysis of mvdc power corridor,” in *2019 IEEE Electric Ship Technologies Symposium (ESTS)*. IEEE, 2019, pp. 106–112.
- [37] *Medium Voltage Cable*, Caledonain.
- [38] A. Benigni and A. Monti, “A parallel approach to real-time simulation of power electronics systems,” *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 5192–5206, 2014.
- [39] J. Lambert, *Numerical Methods for Ordinary Differential Systems: The Initial Value Problem*, 1st ed. United States: Wiley, 1992.
- [40] M. Milton, A. Benigni, M. Vygoder, J. Gudex, and R. Cuzner, “Power electronic system real-time simulation on national instruments FPGA platforms,” in *2019 IEEE Electric Ship Technologies Symposium (ESTS)*. IEEE, 2019, pp. 32–38.
- [41] M. Milton and A. Benigni, “Software and synthesis development libraries for power electronic system real-time simulation,” in *2019 IEEE Electric Ship Technologies Symposium (ESTS)*, Aug 2019, pp. 368–376.
- [42] “ORTIS Solver Code Generation Tools,” <https://github.com/OpenRealTimeSimulation>, 2020.
- [43] B. Wu, Y. Lang, N. Zargari, and S. Kouro, *Power conversion and control of wind energy systems*. John Wiley & Sons, 2011, vol. 76.
- [44] A. L. Julian, G. Oriti, and T. A. Lipo, “Elimination of common-mode voltage in three-phase sinusoidal power converters,” *IEEE Transactions on Power Electronics*, vol. 14, no. 5, pp. 982–989, 1999.
- [45] D. Han, Y. Wu, S. Li, and B. Sarlioglu, “Zero state common mode voltage control in motor drives through inverter topology,” in *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*. IEEE, 2017, pp. 556–560.

- [46] L. V. Dusang, "A ground fault protection method for ungrounded systems," in *2008 IEEE Canada Electric Power Conference*. IEEE, 2008, pp. 1–6.
- [47] S. Beheshtaein, J. Yu, and R. M. Cuzner, "A novel wavelet-based feature extraction from common mode currents for fault location in a residential dc microgrid," in *2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA)*. IEEE, 2017, pp. 706–711.



Mark Vygoder (S'17) received his B.S. in Electrical Engineering and Physics, and M.S. in Electrical Engineering from the University of Wisconsin - Milwaukee, WI, USA, in 2017 and 2020, respectively. He is currently a doctoral student and graduate research assistant in electrical engineering at the same university. During his undergraduate studies, he has interned at various companies including Tesla Motors, Inc. in the summer of 2015.

His current goal is help humanity achieve zero carbon emissions. To this end, his research interests include ac, dc, and hybrid ac-dc microgrids, power electronics based distribution system, their associated protection and real-time simulation, and electrified transportation.



Matthew Milton received his B.S. and M.S. degrees in Electrical Engineering from the University of South Carolina, Columbia, SC, USA, in 2015 and 2016 respectively. Since 2017, he is a Doctoral Student and Graduate Research Assistant in the Department of Electrical Engineering at same university.

His current research focus is on real-time high-performance software- and FPGA-based simulation solvers of power electronic systems, including real-time probabilistic digital twinning and modeling of

such systems.



Jacob Gudex (S'18) received his B.S. and M.S. degrees in electrical engineering from the University of Wisconsin - Milwaukee, WI, USA, in 2017 and 2019, respectfully. He is currently a doctoral student and graduate research assistant in electrical engineering from the same university.

His current research include real-time simulation of power electronics, power conversion, MVdc protection, and their application towards shipboard electrification and microgrids. He is a prior service U.S. Marine with multiple previous combat deployments.



Robert Cuzner (M'90-SM'03) received the B.S. degree in electrical and computer engineering from Brigham Young University, Provo, UT, USA, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Wisconsin-Madison, Madison, WI, USA. In 1990, he joined Miller Electric Manufacturing Company, Appleton, WI, USA, where he designed the generators for engine-driven welders. From 1993 to 2002, he was at the Eaton Corporation, Milwaukee, WI, USA.

From 2002 to 2014, he was a designer of power conversion systems for Navy shipboard applications with DRS Power and Control Technologies, Inc. and Leonardo DRS in Milwaukee. He is currently an Associate Professor with the Department of Electrical Engineering and Computer Science, University of Wisconsin-Milwaukee, Milwaukee.

He has over 30 years of experience working in power generation, power conversion, and drive system controls and packaging for both Navy and industrial applications. He has authored over 80 publications, including IEEE journal and conference papers and tutorials, and he holds four U.S. patents. His current research interests include microgrid protection, distributed generation, power electronics for power distribution and drive systems, electromagnetic compatibility, low- and medium-voltage power conversion system design and power electronic converter system packaging.



Andrea Benigni (S'09-M'14-SM'20) received the B.Sc. and M.Sc. degrees from Politecnico di Milano, Milano, Italy, in 2005 and 2008, respectively, and the Ph.D. degree from RWTH-Aachen University, Aachen, Germany, in 2013. From 2014 to 2019, he was an Assistant Professor with the Department of Electrical Engineering, University of South Carolina, Columbia, SC, USA. In 2019, he joined RWTH-Aachen as professor of "Methods for Simulating Energy Systems" and FZ-Juelich as director of the institute for "Institute of Energy and Climate Research: Energy Systems Engineering (IEK-10)".