A Fault-Tolerant Hybrid Cascaded H-Bridge Topology

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Abstract— This paper presents the fault-tolerant operation for a cascaded H-bridge (CHB) inverter. The added features ensure reliable and robust operation in the event of a fault. The proposed strategy uses an additional cross-coupled CHB (X-CHB) unit in companion with the existing CHB to support the output voltage and ensure continuity of operation in case of an open/short circuit fault. The operation of the proposed X-CHB inverter is described in detail. Simulation and experimental verification of the proposed concept is demonstrated using a seven-level CHB. Both simulation and experimental results validate the fault-tolerant operation of the CHB for a battery energy storage system (BESS) in case of switch faults such as open/short-circuit switch faults or dc-source or battery failure.

Keywords— cascaded H-bridge (CHB), Fault reconfiguration

I. INTRODUCTION

Nowadays multilevel topologies are considered a promising technology for integrating renewable and clean energy resources, such as battery energy storage systems, solar photovoltaics and wind turbine generators to the electric power grid. The reasons behind the rapid adoption of the multilevel converters are due to improved output power quality, scalable/modular configuration, and the possibility of implementing low voltage rated components. Several multilevel topologies have been published in the quest for making the system cost-effective, reliable and less complex in control from both the hardware and software perspectives. Among them, the major multilevel topologies are: Modular Multilevel Converter (MMC), Flying Capacitor (FC), Cascaded H-Bridge (CHB), and Neutral Point Clamped (NPC) inverters [1]-[5]. Even though there are very different types of multilevel topologies, they share the same issue of reliability due to a relatively higher probability of semiconductor device failures [6]-[9].

In other words, reliability is a major concern among conventional multilevel topologies due to the higher number of switches and their driving circuitry. Additionally, in cases of open/short-circuit faults, the multilevel output voltage becomes distorted, which results in a malfunction of the inverter that may propagate upstream to the grid and cause subsequent failures [10]- [12].

The degree of switch failure is also different depending on the circuit topology and application. For instance, in the case of open-circuit faults in CHB inverters, one voltage level is skipped in that particular phase; however, the other two phases continue generating the same output voltage. In the case of a motor drive application, the system can survive for several periods, and a basic controller can reduce the voltage of the healthy phases as well. Reducing the voltage level in a motor drive application does not damage the motor. However, in the case of a grid-tied multilevel inverter, losing one voltage level results in an unbalanced output voltage, which subsequently can shut down the overall system.

In summary, prior methods fall into one of two categories. The first is to detect and isolate a faulty cell. However, isolation of one cell results in reduced functionality and degraded operation as in [13]. The structures in [14]-[15] use a strategy of bypassing the faulty cell in case a fault occurs. Then, two more cells are bypassed from the other phases, which results in an inverter operating with less voltage levels. In other words, it ensures the output voltage is same as before the fault occurs, but with fewer voltage levels. This is possible by boosting the voltage in each healthy H-bridge cell in the case of STATCOM applications. However, it is not practical in the case of BESS. Methods in [16]-17] also isolate the faulty switch, and have the ability to compensate for the fault to maintain the same output voltage. However, these methods are designed only for inverters that have boost stages. There are several other methods proposed for fault-tolerance and reconfiguration when a switch fault occurs [18]-[27]. However, the fault-tolerant strategies presented for the dc-dc converters [18]-[21], flying capacitor inverter [22], two-stage converter [23], T-type inverter [24], mutli-phase inverter [25], and NPC [26]-[27], cannot be implemented for a CHB inverter for BESS.

The structure presented in [28] adds four switches to bypass the faulty cell. Two of these switches are normally open and two
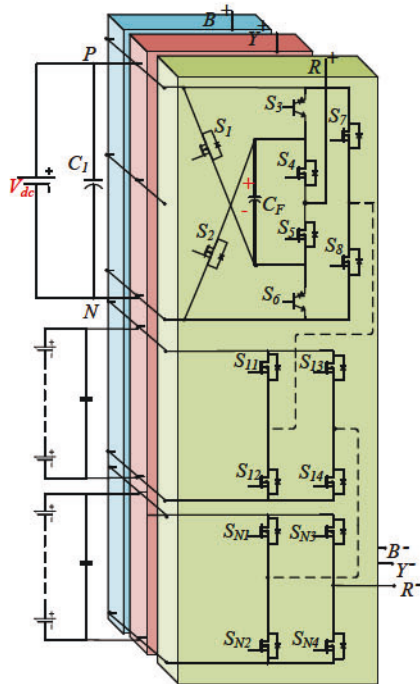
Fig. 1. Proposed *n*-level three phase hybrid CHB inverter.

Fig. 2. A 7-level three phase hybrid CHB inverter.

normally closed. The switches used in [28] are conductors (electromagnetic switches) that are really slow to respond compared with semiconductor devices. Also, this method results in high conduction losses since two switches per H-bridge are always turned-on during normal operation, which produces more losses and heat. The method described in [29] adds four switches to bypass the faulty cell and connect its batteries to the healthy cell. Adding batteries to another cell may damage switches because the input voltage gets doubled, which may exceed the breakdown voltage of the semiconductors. Secondly, in the case of BESS and photovoltaic systems, they will typically have a controller to balance the charging and discharging process. Adding a battery from a faulty cell to a healthy cell may affect the state of charge (SoC), which could result in controller malfunction.

The second solution involves installing a redundant back-up system; however, that significantly increases the overall cost of the system. Redundancy can be achieved when a faulty cell is bypassed and isolated to compensate for the missing voltage level using back-up systems (an extra H-bridge, or batteries). This method can maintain the continuity of the inverter, while producing the same output voltage level. However, using an additional dc source increases the price of the system and the control complexity [30], [31].

Considering the above aspects in the development of fault tolerant and robust CHB systems, a novel hybrid CHB is proposed by adding a novel X-CHB inverter to provide smooth and reliable operation in case of semiconductor device failure. The proposed X-CHB is a five-level inverter with a voltage gain of two. One flying capacitor is integrated into the proposed
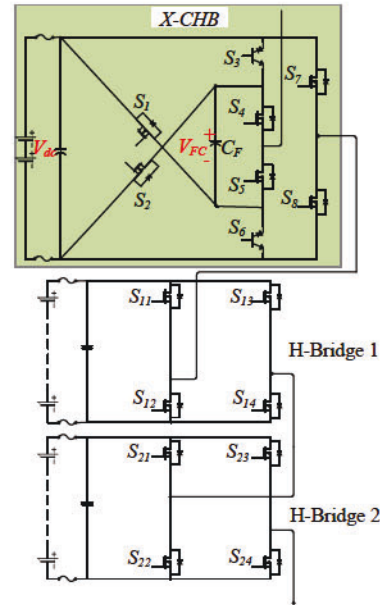
structure that provides voltage boost to have the self-voltage balancing ability in the new system. Even though the application of the proposed topology has been demonstrated with CHB for BESS, it can also be integrated with any type of multilevel topology to achieve fault-tolerant capability.

II. PROPOSED X-CHB

The circuit of the proposed topology is shown in Fig. 1. The circuit is a combination of X-CHB (upper cell) and *n* levels of CHB. The proposed X-CHB inverter can produce five levels. The voltage levels that the X-CHB produces are $2V_{dc}$, V_{dc}, 0, -V_{dc}, and -2 V_{dc}. The proposed X-CHB consists of eight switches; $S_1 - S_8$ that are standard semiconductor devices, such as either IGBTs or MOSFETs. It also requires an additional flying capacitor C_F, to boost the voltage up to 2x. In every switching cycle, the flying capacitor charges to V_{dc} from

TABLE I

SWITCHING STATES OF THE X-CHB INVERTER UNDER FAULT

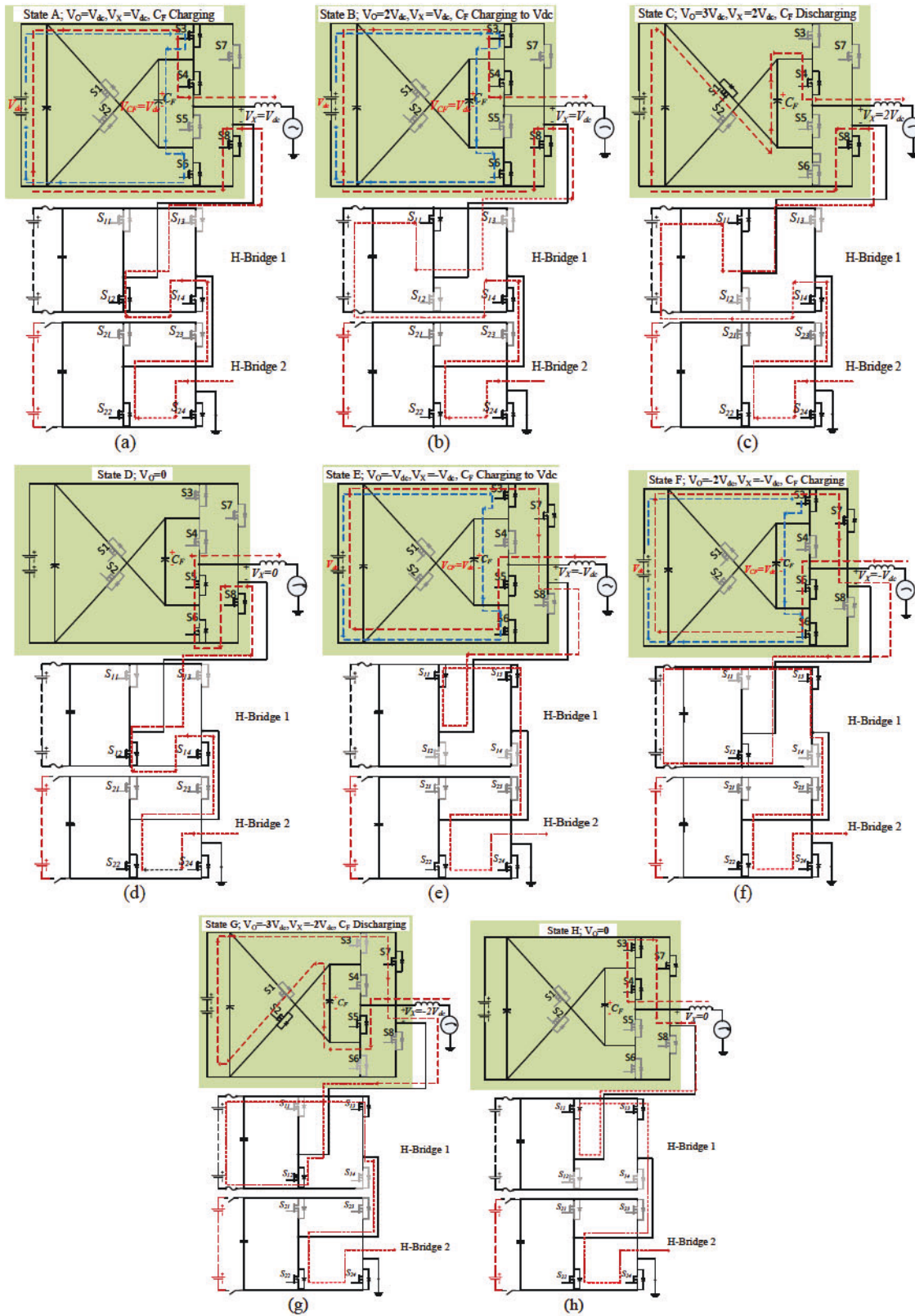| Switching States	A	B	C	D	E	F	G	H
S_1	0	0	1	0	0	0	0	0
S_2	0	0	0	0	0	0	1	0
S_3	1	1	0	0	1	1	0	1
S_4	1	1	1	0	0	0	0	1
S_5	0	0	0	1	1	1	0	0
S_6	1	1	0	1	1	1	1	0
S_7	0	0	0	0	1	1	1	1
S_8	1	1	1	0	0	0	0	0
S_{11}	0	1	1	0	1	0	0	1
S_{12}	1	0	0	1	0	1	1	0
S_{13}	0	0	0	0	1	1	1	1
S_{14}	1	1	1	1	0	0	0	0
V_X	$+V_{dc}$	$+2V_{dc}$	$+3V_{dc}$	0	$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$	0

Fig. 3. Switching states analysis of the hybrid CHB (a) State A: V_{dc}, (b) State B: $2V_{dc}$, (c) State C: $3V_{dc}$, (d) State D: 0, (e) State E: $-V_{dc}$, (f) State F: $-2V_{dc}$, (g) State G: $-3V_{dc}$, (h) State H: 0

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its input dc supply through S_3 and S_6. The X-switches (S_1 and S_2) are employed to create the second voltage level by connecting the dc supply with the flying capacitor and also to boost the voltage up to 2x. Under normal operating conditions, the X-CHB works as a three level inverter producing V_{dc}, 0, -V_{dc} from the dc source. However, during a fault condition such as open/short-circuit fault or battery fault, the system loses one voltage level. During that time, the X-CHB operates as a five level boost inverter compensating for the missing voltage level. This ensures continuity of operation without any disturbance. Therefore, this topology brings a high degree of reliability to the overall system under different fault scenarios.

Overall, this paper presents a novel power converter topology with improved features, such as: 1) continuity of operation in case of a fault (open/short circuit switch fault), 2) low implementation cost compared to existing solutions, 3) full reactive power operation due to its capability of operation in any power factor (lagging/leading), and 4) boosting the voltage level by factor of 2 without the need of an extra boost stage (inductorless voltage boost).

III. OPERATION MODES FOR THE PROPOSED HYBRID CHB SYSTEM

A 7-level hybrid cascaded H-Bridge for fault-tolerant operation is shown in Fig. 2. It consists of the X-CHB (the upper highlighted cell) with two cascaded H-bridge cells. During normal operation, no fault, the inverter is producing seven voltage levels, where the X-CHB operates as an H-bridge inverter producing V_{dc}, 0, -V_{dc}. In other words, the inverter consists of three H-bridge cells and operates as the conventional 7-level CHB inverter.

During a fault condition such as open/short-circuit fault or battery fault, the system loses one voltage level. To detect the faulty cell and the switch, a method similar to [5] can be adopted. Once the faulty cell/switch is detected, the faulty H-bridge should be bypassed by turning ON its upper and lower switches. During that time, the X-CHB operates as a five level boost inverter producing $2V_{dc}$, V_{dc}, 0, -V_{dc}, and -$2V_{dc}$ voltage levels to compensate for the missing voltage level to ensure seven voltage levels at the output of the inverter.

The operation and analysis of the proposed hybrid cascaded H-Bridge is illustrated in Fig. 3. The inverter is assumed to have a fault in the second H-bridge, and the faulty cell is bypassed by turning ON both of the lower switches, S_{22} and S_{24}, of the faulty cell (software bypassing). The operational analysis adopted eight different switching modes (A to H). The red dotted line in Fig. 3 represents the current path, and the blue indicates the capacitor charging current path. Table I lists all possible switching states with its corresponding output voltage for the proposed X-CHB inverter. The output voltage of the X-CHB and the inverter are defined as V_X, and V_o, respectively.

The flying capacitor (C_F) is clamped to the dc power supply through switches S_3 and S_6 as shown in Figs. 3(a), (b), (e), and (f), where the flying capacitor voltage (V_X) is equal to the input voltage V_{dc}. To compensate for the voltage level during the fault, the voltage across C_F gets discharged, and the output voltage of the X-CHB V_X is equal to $2V_{dc}$ and as shown in Fig.

3(c) and (g). By discharging C_F during the positive cycle in series with the input voltage (when S_1, S_4 and S_8 are ON), the output voltage of the X-CHB is $2V_{dc}$ ($V_X = 2V_{dc}$) as shown in Fig. 3(c). Similarly, during the negative cycle, X-CHB can generate -2 V_{dc} by discharging the flying capacitor and connecting it in series with input voltage through S_2, S_5 and S_7 as illustrated in Fig. 3(g).

Thus, the proposed X-CHB has the ability to boost the voltage up to 2x, and increase the voltage levels by using only eight additional switches and one capacitor in the X-CHB without the need of an inductor. These features make the X-CHB applicable to any type of multilevel inverter to achieve fault tolerant operation.

IV. SIMULATION AND EXPERIMENTAL RESULTS

To verify the concept of the proposed hybrid CHB inverter, a detailed MATLAB/Simulink® model for a circuit similar to Fig. 2 was modeled for 7-level inverter. The input voltage was set to 100 V with a 40 Ω resistive load. Fig. 4 shows the output voltage (unfiltered and filtered) and line current waveforms.
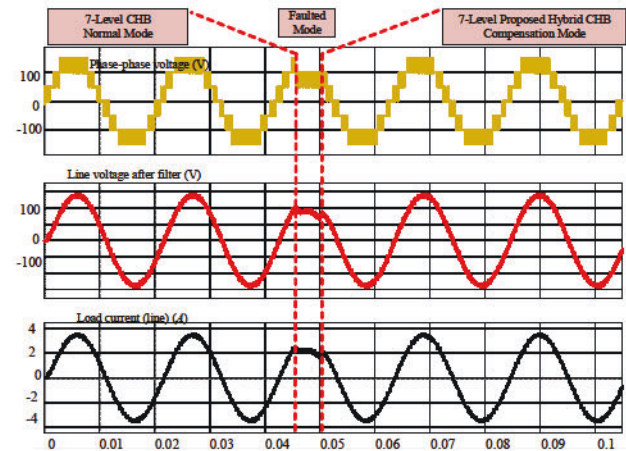

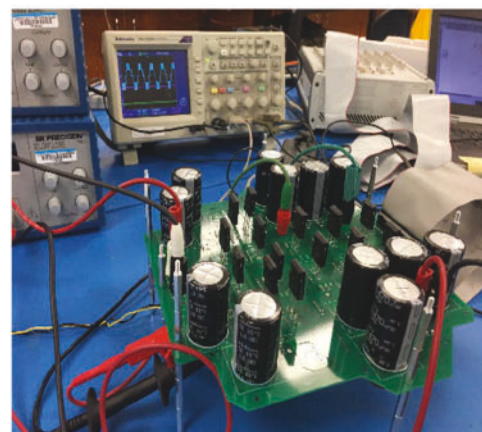Fig. 4. Simulation results of the proposed 7LX-BANPC inverter.

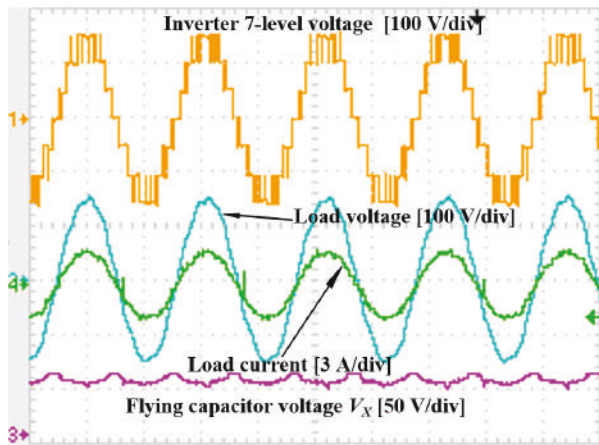Fig. 5. Experimental setup of the proposed 7LX-BANPC inverter

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Fig. 6. Some preliminary measured waveforms.

An open-circuit fault scenario has been created as shown in Fig. 4 at time $t = 0.054$ s. As shown in Fig. 4, the three different modes are: normal operation mode (where the inverter functions as a normal CHB before $t = 0.05$ s), faulted mode (a fault is induced and one voltage is lost from $t = 0.045$ s to $t = 0.05$ s), and compensation mode (where the proposed hybrid CHB operation starts at $t = 0.05$ s). From $t = 0.045$ s to $t = 0.05$ s, the output voltage loses one voltage level. The fault is detected and isolated at $t = 0.05$ s using the method proposed in [5]. The X-CHB compensates for the lost output voltage and restores the output voltage to normal levels within a half power cycle without affecting the system connected downstream.

A scaled down 7-level hybrid CHB low-power prototype has been built and tested in the laboratory as shown in Fig. 5 to validate the concept and performance of the new circuit. The output voltage, output current, and the flying capacitor voltage waveforms are shown in Fig. 6 for the input voltage of 100 V.

V. CONCLUSIONS

This paper presents a novel hybrid CHB for fault-tolerant operation to ensure seamless operation of the system under an open/short circuit switching fault or dc supply fault using a novel X-CHB circuit. In addition to the fault tolerant ability, the proposed inverter has the ability to boost the voltage by a factor of two, which compensates for the missing voltage level in the case of open/short circuit faults. Simulation and experimental results validate the performance of the proposed topology.

ACKNOWLEDGMENT

REFERENCES

[1] S. Kouro et al., "Recent Advances and Industrial Applications of Multilevel Converters," IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[2] S. Rivera et al., "Multilevel Direct Power Control—A Generalized Approach for Grid-Tied Multilevel Converter Applications," IEEE Transactions on Power Electronics, vol. 29, no. 10, pp. 5592-5604, Oct. 2014.

[3] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[4] H. Abu-Rub, J. Holtz, J. Rodriguez and G. Baoming, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2581-2596, Aug. 2010.

[5] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo and M. A. M. Prats, "The age of multilevel converters arrives," in IEEE Industrial Electronics Magazine, vol. 2, no. 2, pp. 28-39, June 2008.

[6] B. Mirafzal, "Survey of Fault-Tolerance Techniques for Three-Phase Voltage Source Inverters," IEEE Transactions on Industrial Electronics, vol. 61, no. 10, pp. 5192-5202, Oct. 2014.

[7] P. Lezana, J. Pou, T. A. Meynard, J. Rodriguez, S. Ceballos and F. Richardeau, "Survey on Fault Operation on Multilevel Inverters," IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2207-2218, July 2010.

[8] H. Wang et al., "Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 1, pp. 97-114, March 2014.

[9] P. Tu, S. Yang and P. Wang, "Reliability- and Cost-Based Redundancy Design for Modular Multilevel Converter," IEEE Transactions on Industrial Electronics, vol. 66, no. 3, pp. 2333-2342, March 2019

[10] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran and P. Tavner, "An Industry-Based Survey of Reliability in Power Electronic Converters," IEEE Transactions on Industry Applications, vol. 47, no. 3, pp. 1441-1451, May-June 2011.

[11] A. Hanif, Y. Yu, D. DeVoto and F. Khan, "A Comprehensive Review Toward the State-of-the-Art in Failure and Lifetime Predictions of Power Electronic Devices," IEEE Transactions on Power Electronics, vol. 34, no. 5, pp. 4729-4746, May 2019.

[12] T. Peng et al., "A Uniform Modeling Method Based on Open-Circuit Faults Analysis for NPC-Three-Level Converter," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 3, pp. 457-461, March 2019.

[13] J. Zhang, Z. Liu, T. Wang, M. E. H. Benbouzid and Y. Wang, "An Arm Isolation and Reconfiguration Fault Tolerant Control Method Based on Data-driven Methodology for Cascaded Seven-level Inverter," 2018 IEEE 7th Data Driven Control and Learning Systems Conference (DDCLS), pp. 939-943, Enshi, 2018.

[14] W. Song, A. Q. Huang, "Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM", IEEE Transactions on Industrial Electronic., vol. 57, no. 8, pp. 2700-2708, Aug. 2010

[15] A. Yazdani, H. Sepahvand, M. L. Crow and M. Ferdowsi, "Fault Detection and Mitigation in Multilevel Converter STATCOMs," IEEE Transactions on Industrial Electronics, vol. 58, no. 4, pp. 1307-1315, April 2011.

[16] S. Rahman, M. Meraj, A. Iqbal and L. Ben-Brahim, "Novel voltage balancing algorithm for single-phase cascaded multilevel inverter for post-module failure operation in solar photovoltaic applications," in IET Renewable Power Generation, vol. 13, no. 3, pp. 427-437, 25 2 2019.

[17] M. Jalhotra, L. K. Sahu, S. P. Gautam and S. Gupta, "Reliability and energy sharing analysis of a fault-tolerant multilevel inverter topology," in IET Power Electronics, vol. 12, no. 4, pp. 759-768, 10 4 2019.

[18] E. Jamshidpour, P. Poure and S. Saadate, "Photovoltaic Systems Reliability Improvement by Real-Time FPGA-Based Switch Failure Diagnosis and Fault-Tolerant DC–DC Converter," IEEE Transactions on Industrial Electronics, vol. 62, no. 11, pp. 7247-7255, Nov. 2015.

[19] S. Siouane, S. Jovanović, P. Poure and E. Jamshidpour, "An Efficient Fault Tolerant Cascaded Step-Up Step-Down Converter for Solar PV Modules," 2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), Palermo, 2018, pp. 1-5.

[20] M. M. Haji-Esmaeili, M. Naseri, H. Khoun-Jahan and M. Abapour, "Fault-Tolerant and Reliable Structure for a Cascaded Quasi-Z-Source DC–DC Converter," IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 6455-6467, Aug. 2017.

[21] K. Ambusaidi, V. Pickert and B. Zahawi, "New Circuit Topology for Fault Tolerant H-Bridge DC–DC Converter," IEEE Transactions on Power Electronics, vol. 25, no. 6, pp. 1509-1516, June 2010.

[22] J. Amini and M. Moallem, "A Fault-Diagnosis and Fault-Tolerant Control Scheme for Flying Capacitor Multilevel Inverters," IEEE Transactions on Industrial Electronics, vol. 64, no. 3, pp. 1818-1826, March 2017.

[23] M. Farhadi, M. T. Fard, M. Abapour and M. T. Hagh, "DC–AC Converter-Fed Induction Motor Drive With Fault-Tolerant Capability Under Open- and Short-Circuit Switch Failures," IEEE Transactions on Power Electronics, vol. 33, no. 2, pp. 1609-1621, Feb. 2018.

[24] R. V. Nemade, J. K. Pandit and M. V. Aware, "Reconfiguration of T-Type Inverter for Direct Torque Controlled Induction Motor Drives Under Open-Switch Faults," IEEE Transactions on Industry Applications, vol. 53, no. 3, pp. 2936-2947, May-June 2017.

[25] B. P. Reddy, M. Rao A, M. Sahoo and S. Keerthipati, "A Fault-Tolerant Multilevel Inverter for Improving the Performance of a Pole–Phase Modulated Nine-Phase Induction Motor Drive," IEEE Transactions on Industrial Electronics, vol. 65, no. 2, pp. 1107-1116, Feb. 2018.

[26] W. Chen, E. Hotchkiss and A. Bazzi, "Reconfiguration of NPC multilevel inverters to mitigate short circuit faults using back-to-back switches," CPSS Transactions on Power Electronics and Applications, vol. 3, no. 1, pp. 46-55, March 2018.

[27] M. Aly, E. M. Ahmed and M. Shoyama, "A New Single-Phase Five-Level Inverter Topology for Single and Multiple Switches Fault Tolerance," IEEE Transactions on Power Electronics, vol. 33, no. 11, pp. 9198-9208, Nov. 2018.

[28] M. M. Haji-Esmaeili, M. Naseri, H. Khoun-Jahan and M. Abapour, "Fault-tolerant structure for cascaded H-bridge multilevel inverter and reliability evaluation," IET Power Electronics, vol. 10, no. 1, pp. 59-70, 1 20 2017.

[29] H. K. Jahan, F. Panahandeh, M. Abapour and S. Tohidi, "Reconfigurable Multilevel Inverter With Fault-Tolerant Ability," in IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 7880-7893, Sept. 2018.

[30] M. Aleenejad, H. Iman-Eini and S. Farhangi, "Modified space vector modulation for fault-tolerant operation of multilevel cascaded H-bridge inverters," IET Power Electronics, vol. 6, no. 4, pp. 742-751, April 2013.

[31] P. Moamaei, H. Mahmoudi and R. Ahmadi, "Fault-tolerant operation of cascaded H-Bridge inverters using one redundant cell," 2015 IEEE Power and Energy Conference at Illinois (PECI), Champaign, IL, pp. 1 5, 2015.