Variable-Switching Constant-Sampling Frequency Critical Soft Switching Model Predictive Control for DC/DC Converters

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***Abstract*—A variable-switching constant-sampling frequency critical soft switching model predictive control (VSCS-MPC) method is proposed in this paper to improve the dynamic behavior, efficiency and power density of the DC/DC power converters. Firstly, this paper analyzes the boundary constraints of critical soft switching that are derived with the key parameters of the interlock time and threshold current for typical SiC and GaN devices. Then, the VSCS-MPC method is proposed for synchronous DC/DC converter. Both the current source load and resistive load converters are validated with the proposed MPC method. VSCS-MPC includes two controlling parts. First is the frequency controller to maintain the critical soft switching operation by adjusting the switching frequency based on the predefined boundary conditions with a constant sampling frequency. A discretized frequency controller is developed to improve the stability of the system by maintaining a fixed sampling frequency. Second part is the model predictive controller to track the output voltage/current and maintain critical soft switching during dynamic periods. The explicit optimization and oversampling methods are applied in the MPC controller to meet the high frequency demand. A large current ripple ($\triangle i_L \geq$ 200 %) is introduced to achieve the critical soft switching and reduce the inductance. The switching losses are decreased by the frequency controller and the critical soft switching is maintained especially in dynamic periods due to the fast response of MPC.**

***Index Terms*—Model predictive control, critical soft switching, variable switching frequency control, constant sampling frequency.**

I. Introduction

WIDE-bandgap devices (WBG) are attracting more and more attention in the field of power conversion system. Silicon carbide (SiC) and Gallium Nitride (GaN) MOSFETs are two types of semiconductor that have been widely used in industrial applications due to the superior characteristics in high power and high frequency behaviors [1]. Applying wide-bandgap devices in power converters can achieve high switching frequency with high power level [2]. This characteristic could decrease the inductance/capacitance values to improve the power density [3]. One issue that should be carefully considered is the switching losses which are mainly caused by the overlapping voltage and current waveforms during turn-on and turn-off switching periods [4]. The switching losses could be influenced by many factors such as the device intrinsic features, peripheral circuits, gate driver behavior, soft switching design, controlling strategy, etc [5]. For the generality point of view, an effective way to decrease the switching losses is by combining the last two parts: soft switching design and controlling strategy. Firstly, soft switching is a key technique to reduce the switching losses in power converters [6]. The principle of soft switching is to avoid the overlapping area of switch voltage and current waveforms [7]. It can be divided into zero-voltage soft switching (ZVS) and zero-current soft switching (ZCS). ZVS aims at minimizing the voltage across the switch during switching transients and ZCS deals with the switching tail current to minimize the losses during transient periods. To realize the soft switching operation, auxiliary circuits can be added to handle the turn-on and turn-off instants for switching losses minimization [8]. However, the active auxiliary circuits will induce more cost and controlling complexity. Another way to implement soft switching is by designing the passive component values, such as filtering inductance and capacitance, and power converter operating parameters, such as current ripple, switching frequency, dead time, etc [9]. The passive soft switching methods could be implemented based on a common characteristic of the MOSFETs: turn-on losses of the most MOSFETs are much greater than the turn-off losses. So, the soft switching strategy can be designed to replace the higher turn-on losses with lower turn-off losses [10]. For the state of the art of passive soft switching techniques in DC/DC buck modules, the primary method is to enlarge the inductor current ripple with bidirectional flowing paths at peak/valley points. This operating mode can be implemented by synthesizing the filtering inductor design, switching frequency configuration, power rating requirement and MOSFET characteristic analysis. [11] studied the passive soft switching technique without adding active auxiliary circuit or passive snubbers and implemented the soft switching on a bidirectional three-phase paralleled buck converter to achieve high efficiency and power-density specifically in IGBT devices. [12] focused on the passive soft switching analysis for interleaved multi-phase DC/DC converter specifically in the application of energy storage systems. The current ripple balancing issue is studied for efficiency improvement. The forementioned techniques have developed convincing methods to achieve ZVS operation. However, the transient performance of soft switching is another key topic that merits attention. A steadily fast control method can avoid the oscillation or overshoot issues during the dynamic period to further improve the soft switching losses. Specifically, the second part is the controlling strategy: a better controlling method can achieve

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superior dynamic performance and accurate tracking behavior. A fast and stable controller will cause less oscillation on the output waveforms which means the soft switching operation can be achieved accurately and maintained steadily, especially during the transient period. Thus, the switching losses induced by the hard switching will be decreased accordingly. The most commonly used controlling method is PI controller. It is simple to design and implement with good performance. However, the overshoot and dynamic oscillation issues are the main drawbacks due to the integral process. Another more advanced controlling method that has better dynamic performance is model predictive control (MPC) [13], [14]. It can generate the optimal input values for the system by predicting multiple steps based on the state space equations and cost function [15]. Compared to PI controller, MPC has been validated to have faster tracking speed and better transient behavior if designed properly [16].

This paper proposes a controlling method based on the above mentioned two aspects to improve the efficiency and power density of the DC/DC converter. Firstly, a critical soft switching method is designed to achieve the soft switching operation without auxiliary circuits. The boundary constraints of typical WBG devices are derived according to the dead time and peak/valley inductor currents. The controlling method is designed based on the critical soft switching boundary constraints. Then, the variable-switching constant-sampling frequency critical-soft-switching model-predictive-control (VSCS-MPC) method is proposed. For the general purpose, both the current source load and resistive load converters are validated with the proposed MPC method. The controlling method mainly includes two parts: frequency controller and MPC controller. Frequency controller is designed to reduce the switching losses of the converter under critical soft switching by controlling the inductor current ripple. The expected switching frequency is calculated according to the measured inductor current, output voltage and duty cycle. For the consideration of system stability to generate the PWM signals, the switching frequency are discretized into equally segmented bandwidth for the purpose of maintaining a constant sampling frequency. If the calculated frequency belongs to certain range of the bandwidth, a fixed switching frequency will be delivered to the PWM. And the MPC controller will receive the measured output voltage and inductor current to generate the optimal duty cycle for tracking the voltage/current references. In order to alleviate the calculation burden in high frequency application, an oversampling method is designed based on the segmented frequency controller. Specifically, the MPC, frequency controller and sampling will be updated based on a constant fundamental frequency, $f_{s,base}$, and the PWM switching frequency will be determined by the discretized frequency controller according to the equally segmented bandwidth range. Thus, the switching frequency will be adjusted steadily at a certain integral multiple, n, times of the fundamental frequency to achieve the soft switching operation when the calculated frequency is within certain bandwidth range. The system oscillation will be mitigated by avoiding a time-varying sampling frequency and instantaneously changed switching frequency. By combining the two controllers, the proposed VSCS-MPC can achieve high efficiency and superior dynamic performance robustly. The analytical tests are implemented on a SiC testbench to verify the proposed controlling method.

II. Critical Soft Switching Principles for DC/DC Converter

In this section, the critical soft switching technique is introduced with the derived boundary conditions of dead time and peak/valley inductor current by datasheet and integral equations. The main purpose of the critical soft switching method is to replace the large turn-on loss of upper switch with small turn-off loss of lower switch [17], [18]. Fig. 1 shows the current paths of DC/DC converter during lower switch turn-off period. For the critical soft switching, a large current ripple is required to ensure negative valley inductor current to be lower than a threshold current level as is shown in Fig. 2. In the turn-off transient period of lower switch, the negative inductor current will discharge the upper switch output capacitor, $C_{oss,m1}$. The ZVS of upper switch can be achieved if the $C_{oss,m1}$ is fully discharged before it turns on. The ZVS operation depends on the interlock time between two switches and the value of inductor valley current. The inductor valley current is expressed as:

$$I_{L,min} = -I_{DS,M2} + I_{CDS,M1} - I_{CDS,M2} \tag{1}$$

$I_{DS,M1}$ and $I_{DS,M2}$ are the drain current through the upper and lower switches, $I_{CDS,M1}$ and $I_{CDS,M2}$ are the current through the upper and lower switch output capacitance, respectively. Because:

$$I_{CDS,M1} = C_{DS,M1}\frac{dU_{DS,M1}}{dt} \tag{2}$$

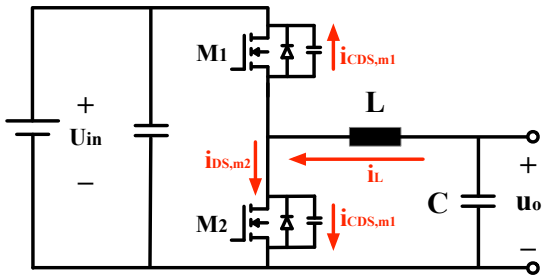


Fig. 1. The negative inductor current paths of DC/DC Buck converter.

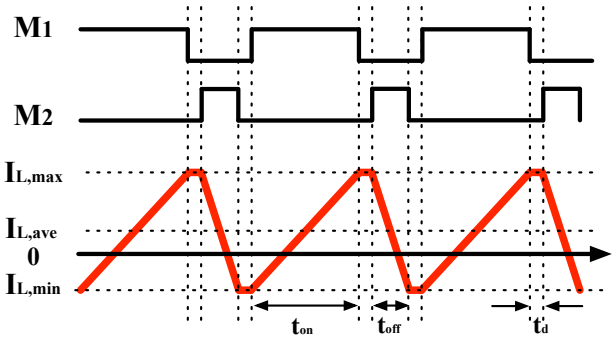


Fig. 2. Gate signals and inductor current for critical soft switching.

$$I_{CDS,M2} = C_{DS,M2}\frac{dU_{DS,M2}}{dt} \tag{3}$$

And ($U_{DS,M1}$+$U_{DS,M2}$) equals to the input source voltage, U_{in}, which is a constant value, then $I_{L,min}$ is expressed as:

$$I_{L,min} = -I_{DS,M2} - (C_{DS,M1} + C_{DS,M2})\frac{dU_{DS,M2}}{dt} \tag{4}$$

Similarly, the maximum positive value is:

$$I_{L,max} = I_{DS,M1} + (C_{DS,M1} + C_{DS,M2})\frac{dU_{DS,M2}}{dt} \tag{5}$$

The above current equations can be further analyzed by the integral calculation over interlock time, T_d, and drain-source voltage, U_{ds}, respectively.

$$\int_0^{T_d} [I_{L,min} - I_{DS,M2}(t)]\, dt = Q_{min} = \tag{6a}$$
$$\int_0^{U_{in}} -[C_{DS,M1}(U_{DS,M2}) + C_{DS,M2}(U_{DS,M2})]\, dU_{DS,M2};$$
$$\int_0^{T_d} [I_{L,max} - I_{DS,M1}(t)]\, dt = Q_{max} = \tag{6b}$$
$$\int_{U_{in}}^{0} [C_{DS,M1}(U_{DS,M2}) + C_{DS,M2}(U_{DS,M2})]\, dU_{DS,M2}.$$

where $Q_{min} \leq 0$ and $Q_{max} \geq 0$ are the total charge moved in the output capacitors. Assuming that I_{ds} is varying linearly with time, the left side of the two equations in equation (6) can be calculated as:

$$\int_0^{T_d} [I_{L,min} - I_{DS,M2}(t)]\, dt = \tag{7a}$$
$$\int_0^{T_d} [I_{L,min} - (I_{L,min} - \frac{I_{L,min}}{T_d}t)]\, dt = \frac{1}{2}I_{L,min}T_d;$$
$$\int_0^{T_d} [I_{L,max} - I_{DS,M1}(t)]\, dt = \tag{7b}$$
$$\int_0^{T_d} [I_{L,max} - (I_{L,max} - \frac{I_{L,max}}{T_d}t)]\, dt = \frac{1}{2}I_{L,max}T_d.$$

So, the critical soft switching can be achieved with the inequalities of $I_{L,min(L,max)}$ and T_d:

$$\tfrac{1}{2}I_{L,min}T_d \leq Q_{min} \leq 0; \tag{8a}$$
$$\tfrac{1}{2}I_{L,max}T_d \geq Q_{max} \geq 0. \tag{8b}$$

Thus, the minimum negative and maximum positive inductor current can be derived with the variables of dead time, T_d, and the integration of output capacitors with drain-source voltages. The design of the converter should satisfy the two inequalities to guarantee the critical soft switching operation. The integral of switch output capacitance to drain-source voltages can be calculated based on the datasheet provided by the device manufacturer. So the integrations of equation can be calculated by tracing several discrete voltage intervals multiplied by the corresponding capacitance value and then accumulating together. According to the relation waveform of switch output capacitance and drain-source voltage, the right side of inequalities (8) can be derived by tracing n points on the curve of switch output capacitance, C_{oss}, and summing up the n intervals together.

Then, the model of critical soft switching method can be expressed with the function image in Fig. 3. It can be shown that the blue regions are the feasible soft switching range according to the constraints of inequalities (8) with the maximum and minimum dead time requirement. Also, the soft switching ranges of typical GaN and SiC devices are given in Fig. 3. During controlling part in the following sections, the dead time and peak/valley inductor currents can be controlled within the critical soft switching region to reduce the switching losses with optimal frequency.

III. Control

This section gives the detailed controlling method of the proposed variable-switching constant-sampling frequency critical-soft-switching model-predictive-control strategy. The VSCS-MPC includes two parts: frequency controller to achieve the critical soft switching operation; MPC controller to track the output voltage/current and improve the dynamic performance. The implementation of MPC controller has large computation burden. So, an explicit MPC method is applied to solve the optimization problem offline. And due to the characteristic of MPC, a fixed sampling time period is required. Thus, to combine the MPC and variable frequency controller, the switching frequency is equally segmented based on a fundamental frequency, $f_{s,base}$. The MPC and freqeuncy controller is updated with $f_{s,base}$ to guarantee enough computation time. And the frequency controller will calculate the expected soft switching frequency and transfer it into a discrete value for PWM based on the pre-designed bandwidth ranges. Thus, the switching frequency for PWM is discretized to be n times larger than the fundamental frequency, $f_{s,base}$, which avoids the oscillation of the time-varying switching frequency.

A. Frequency Controller

For the frequency controller, the main purpose is to operate the converter in critical soft switching region and reduce the switching losses. In every fundamental time period, the frequency controller receives the duty cycle and inductor

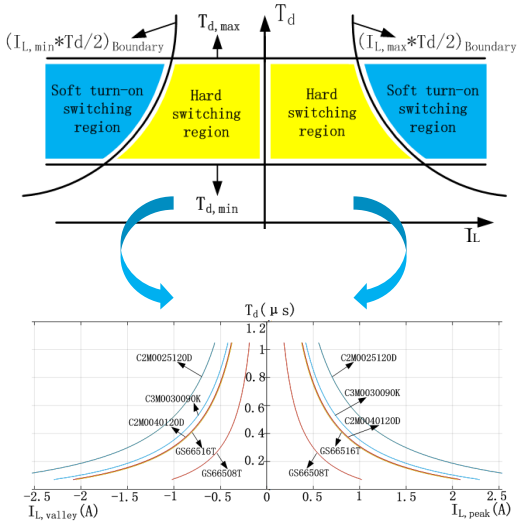


Fig. 3. The critical soft switching operation regions for different devices.

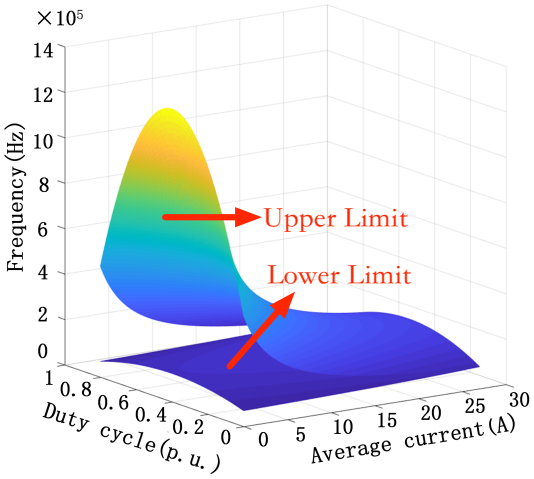


Fig. 4. The thermal, soft switching, frequency and device current constraints of f_{sw} with the function of duty and $I_{L,ave}$.

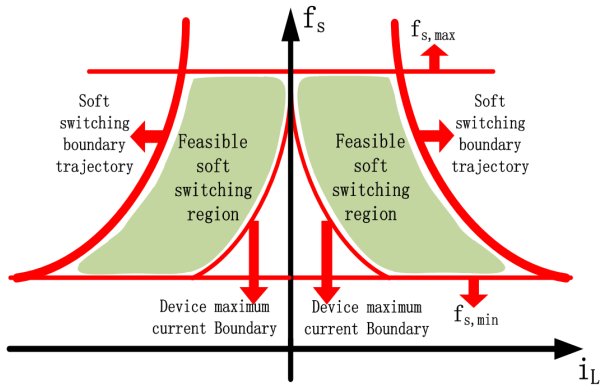


Fig. 5. The feasible trajectories of maximum frequency control method with certain duty.

current values from the MPC controller to calculate the desired switching frequency. Then, the switching frequency is discretized based on the bandwidth ranges to derive a fixed value for the PWM. The calculation of the switching frequency is based on the critical soft switching constraints which have been derived in section II. The design of the frequency controller includes the constraints and methodology which have been shown as following.

1) Constraints: The principle of the frequency controller is to generate the feasible switching frequency based on the critical soft switching boundary conditions. In every calculating period, the frequency controller receives the information of duty cycle and inductor current from the MPC controller. Then an expected switching frequency is pre-calculated for discretization based on the bandwidth ranges and send to the PWM module. During the calculation of the expected switching frequency, four parts of constraints need to be taken into consideration: critical soft switching threshold current, I_{th}, maximum device current, I_{max}, maximum thermal rising, $P_{thermal,max}$ and frequency ranges:

$$I_{th} \leq I_{peak} = I_{L,ave} + \frac{\triangle i_L}{2} \leq I_{max} \tag{9}$$

$$-I_{max} \leq I_{valley} = I_{L,ave} - \frac{\triangle i_L}{2} \leq -I_{th} \tag{10}$$

$$P_{sw} + P_{con} \leq P_{thermal,max} = \frac{T_{j,max} - T_{case}}{R_{th,J-C}} \tag{11}$$

$$f_{sw,min} \leq f_{sw} \leq f_{sw,max} \tag{12}$$

where I_{peak}, I_{valley}, $T_{j,max}$, T_{case} and $R_{th,J-C}$ are the peak, valley points of inductor current, junction, case temperatures and thermal resistance, respectively. The inductor current ripple is the function of three variables, ($I_{L,ave}$, d, f_{sw}):

$$\Delta i_L = \frac{d(1-d)U_{in}}{f_s L} \tag{13}$$

So the derived constraints (9)-(12) can also be expressed as the function of ($I_{L,ave}$, d, f_{sw}) with the help of the substitution in (13). Thus, the constraints of f_{sw} with respect to $(I_{L,ave}, d)$ can be plotted in the 3D coordinate system as is shown in Fig.4 where the two surfaces represent the upper and lower limits of the frequency controller, respectively. The calculation of expected switching frequency is based on the boundaries of the constraints to mainly satisfy the critical soft switching.

2) Methodology: The operating trajectories of the frequency controller can be illustrated in Fig. 5. With the variation of inductor current and duty cycle, the maximum feasible frequency under the critical soft switching constraints can be derived by the function of f_{sw} with respect to $(I_{L,ave}, d)$ (bold red lines in Fig. 5). Based on the derived critical soft switching boundary conditions, the maximum frequency controller trajectories are divided by positive/negative inductor current conditions and the expected switching frequency can be expressed as:

$$f_{s,cal} = \frac{(1-d)dU_{in}}{2(I_{L,ave} + I_{th})L}, \ I_{L,ave} \geq 0 \tag{14a}$$

$$f_{s,cal} = \frac{(1-d)dU_{in}}{2(I_{th} - I_{L,ave})L}, \ I_{L,ave} \leq 0 \tag{14b}$$

where the threshold current of critical soft switching constraints, I_{th}, is based on the results derived in section II.

After the calculation of the expected switching frequency, the values are then discretized by a pre-designed bandwidth ranges which are the integral multiple of the fundamental frequency, $f_{s,base}$. The fundamental frequency for MPC and frequency controller is set to be 30kHz, thus the discretized frequency for PWM signals could be n times of $f_{s,base}$. It should be noted that when a certain discrete bandwidth range of the switching frequency is derived, the integral multiple value of n is rounded down to guarantee the soft switching is maintained by choosing a relatively lower switching frequency. The implementation of the frequency controller is shown in Fig. 6. Also, to make a better explanation of the discrete frequency controller, the function curve of calculated switching frequency with duty cycle is drawn in Fig. 7 under the rated current load. It can be seen that the vertical axis of the switching frequency is equally segmented with the bandwidth of 30kHz. The PWM frequency is discretized and assigned as the lowest value at each range of duty cycle. The relationship

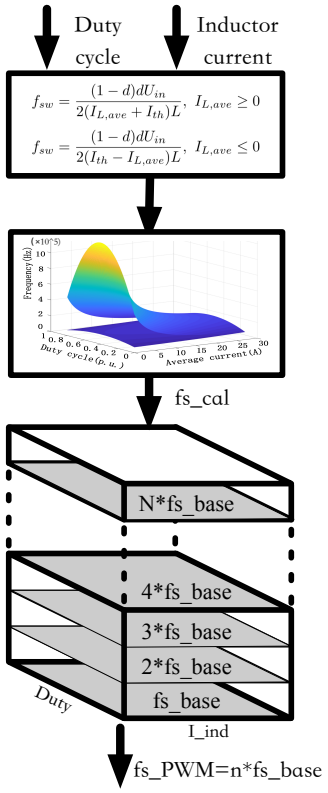


Fig. 6. Discrete frequency controller with equally segmented bandwidth.

of PWM carrier signals and sampling signals are shown in Fig. 8 with a varying switching frequency from $4f_{s,base}$ to $f_{s,base}$. And the algorithm of the frequency controller is shown in Algorithm 1 where u_s, u_o and i_L represent the input, output voltages and inductor current, respectively.

Algorithm 1 Frequency Controller

1: at each sampling period, $T_{s,base}$.
2: $ADCs \leftarrow i_L, u_o, u_s$
3: **while** FreqCTRL=1 **do**
4: obtain duty cycle from MPC Controller
5: obtain $f_{s,cal}$ by (9)-(14b)
6: $n \leftarrow \text{floor}(f_{s,cal}/f_{s,base})$
7: $f_{s,PWM} \leftarrow nf_{s,base}$
8: **end while**

B. Model Predictive Controller

MPC aims at tracking the output voltage/current according to the pre-defined references. In every calculating period of fundamental frequency, $f_{s,base}$, the MPC controller receives the measured inductor current, input/output voltage values and generates the optimal duty cycle for both PWM module and frequency controller. The MPC formulations for both current source load and resistive load are shown in this section.

Firstly, the state equations of the DC/DC converter with LC filters and current source load is

$$i_L(k+1) = i_L(k) - \frac{T_s}{L}u_o(k) + \frac{U_{in}T_s}{L}d(k), \tag{15a}$$

$$u_o(k+1) = \frac{T_s}{C}i_L(k) + u_o(k) - \frac{T_s}{C}i_o(k). \tag{15b}$$

For the resistive load, the term $i_o(k)$ in (15) can be replaced with $u_o(t)/R_{load}$ and $u_o(k)/R_{load}$, respectively, where R_{load} is the output resistor. For the flexibility of implementing the explicit MPC and the convenience of experimentally adjusting the input voltage during test, the last term of (15), $U_{in}d(k)$, can be replaced by the phase leg output voltage, $u_x(k)$. The state-space model with current source load are in standard matrix format:

$$X_{k+1} = A_iX_k + B_iu_{ik}, \tag{16a}$$

$$A_i = \begin{bmatrix} 1 & -\frac{T_s}{L} \\ \frac{T_s}{C} & 1 \end{bmatrix},\ B_i = \begin{bmatrix} \frac{T_s}{L} & 0 \\ 0 & -\frac{T_s}{C} \end{bmatrix}, \tag{16b}$$

$$X_k = \begin{bmatrix} i_L(k) \\ u_o(k) \end{bmatrix},\ u_{ik} = \begin{bmatrix} U_{in}d(k) \\ i_o(k) \end{bmatrix}. \tag{16c}$$

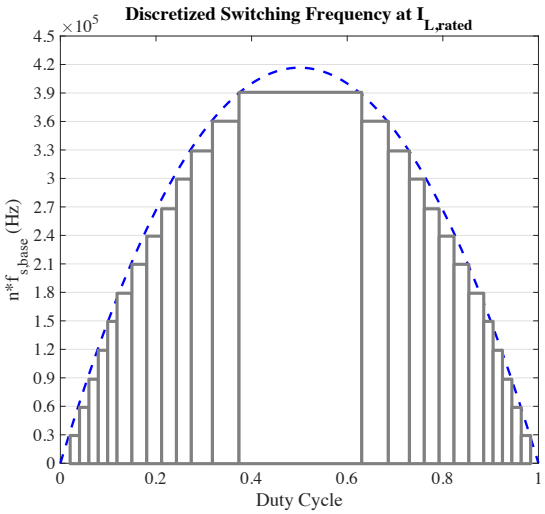


Fig. 7. Equally segmented switching frequency with the function of duty cycle at the rated load current.

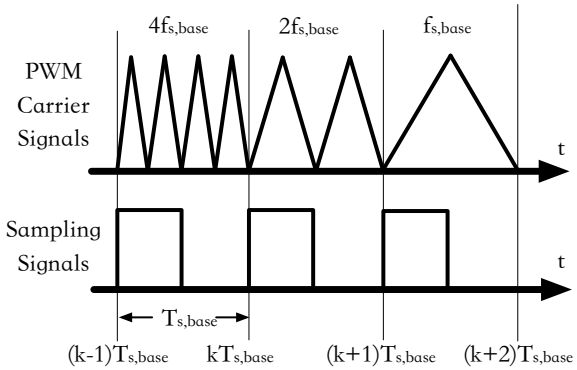


Fig. 8. Variable PWM carrier signals and constant sampling signals of the VSCS-MPC method.

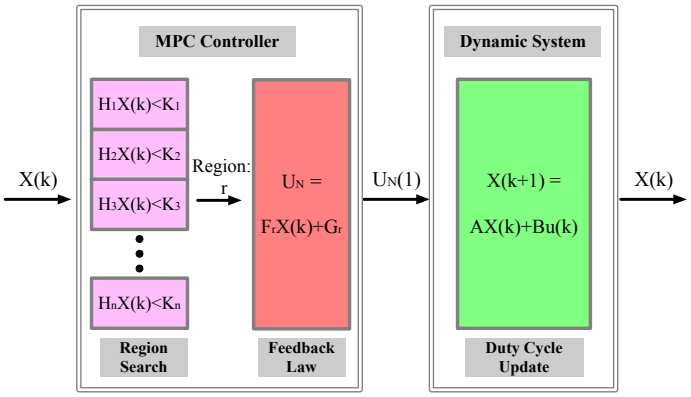


Fig. 9. MPC optimization search tree implementing process.

The state-space model with resistive load is:

$$X_{k+1} = A_r X_k + B_r u_{rk}, \tag{17a}$$

$$A_r = \begin{bmatrix} 1 & -\frac{T_s}{L} \\ \frac{T_s}{C} & 1 - \frac{T_s}{RC} \end{bmatrix}, B_r = \begin{bmatrix} \frac{T_s}{L} \\ 0 \end{bmatrix}, \tag{17b}$$

$$X_k = \begin{bmatrix} i_L(k) \\ u_o(k) \end{bmatrix}, u_{rk} = \begin{bmatrix} U_{in} d(k) \end{bmatrix}. \tag{17c}$$

To derive the state matrix for MPC formulation, the output current is regarded as the input variable. So, in the implementation of the control, the current load can be measured and adjusted as a constraints for the input vector. In the standardized state matrix, the voltage/current references can be defined as $\bar{X}$ and the tracking errors between the measurement and the references are expressed as $\tilde{X}$.

$$\bar{X}_k = \begin{bmatrix} i_{Lr} \\ u_{or} \end{bmatrix}, \tilde{X}_k = \begin{bmatrix} i_{Lr} - i_L(k) \\ u_{or} - u(k) \end{bmatrix} \tag{18}$$

Thus, the cost function includes two terms:

$$min \sum_{k=0}^{N_c} \tilde{X}_k^T Q \tilde{X}_k + \sum_{k=0}^{N_p - 1} \triangle u_k^T R \triangle u_k \tag{19}$$

For the penalties of the cost function, Q and R represent the weighing factor matrices that are implemented on the state values and input values, respectively. For the state value part, more weight is addressed on output voltage in current source load converter because the inductor current is restricted by the current load. For the input value part, more weight is addressed on duty cycle to stabilize the system behavior. Typical values for Q and R are [1, 0; 0, 1000] and [1000, 0; 0, 1], respectively.

The constraints of the MPC controller can be expressed as:

$$\tilde{X}_{k+1} = A\tilde{X}_k + Bu_k \in \mathcal{X} \tag{20}$$

$$\triangle u_k = u_k - u_{k-1} \in \mathcal{U} \tag{21}$$

$$\begin{bmatrix} -I_{L,max} \\ 0 \end{bmatrix} \leq X_k \leq \begin{bmatrix} I_{L,max} \\ U_{in} \end{bmatrix} \tag{22}$$

With current source load, the input constraint is

$$\begin{bmatrix} 0 \\ i_o(k) \end{bmatrix} \leq u_{ik} \leq \begin{bmatrix} U_{in} \\ i_o(k) \end{bmatrix} \tag{23}$$

The second term of u_{ik} is the output current from the known current source load. The controller assigns the measured value by setting the constraints as is shown in (23). This configuration allows a real-time adjustment of the output current that is compatible with explicit MPC. With resistive loads, the input constraint simplifies to:

$$\begin{bmatrix} 0 \end{bmatrix} \leq u_{rk} \leq \begin{bmatrix} U_{in} \end{bmatrix} \tag{24}$$

To achieve a high frequency for the DC/DC converter and reduce the calculation load of the controller, the MPC problem is solved explicitly by generating a piecewise affine feedback law [19]. Fig. 9 shows the mechanism of explicit MPC implementation process. The state model and constraints of the dynamic system are built offline to generate an online search tree and feedback law for optimization. In each controlling time period, the active region, r, is searched with the matrices H_r and K_r. Then, in each of the specific active region, the corresponding feedback law matrices, F_r and G_r, are applied to calculate the optimal input values with the prediction horizon. Only the first value of the input matrix is applied to the dynamic system for MPC control.

In every fundamental time period, the pre-designed search tree can find the optimal duty cycle based on the updated state values of inductor current/output voltage. Explicit MPC avoids the time-consuming online optimization process, thus it is suitable for high frequency control. A generated piecewise affine region block with one input variable of phase leg output

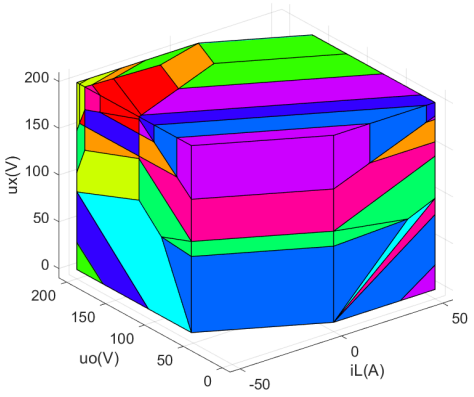


Fig. 10. Explicit MPC piecewise affine regions with prediction horizon of 5.

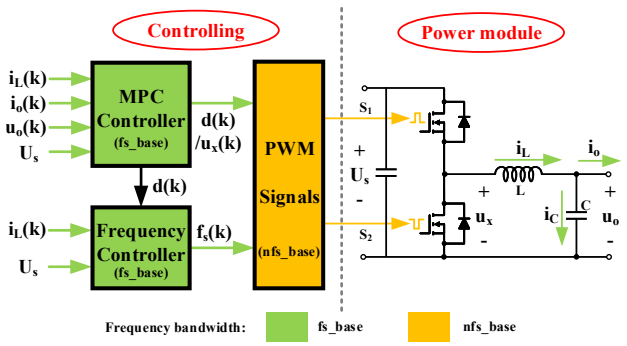
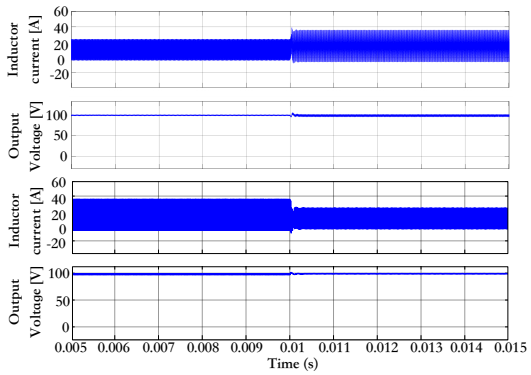
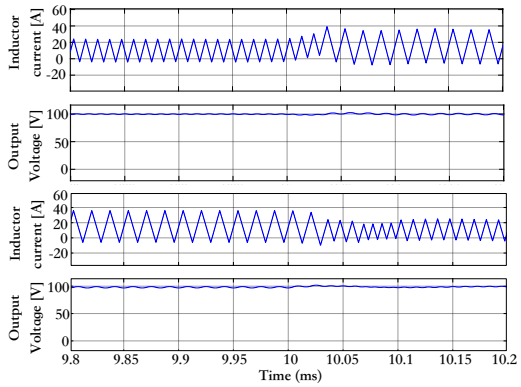


Fig. 11. Proposed variable-switching constant-sampling frequency critical-soft-switching Model-predictive control diagram.

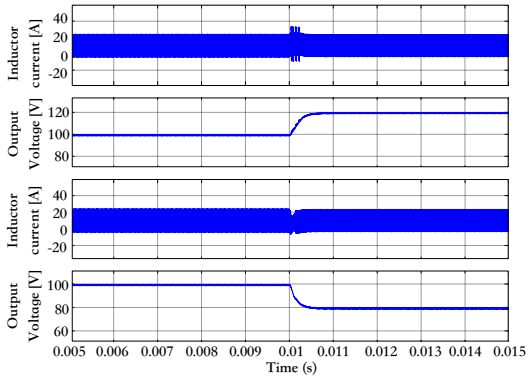


(a) Inductor current and output voltage waveforms

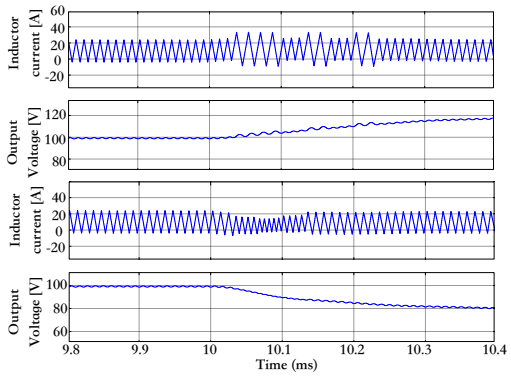


(b) Zoomed waveforms during transient period

Fig. 12. VSCS-MPC of current load: inductor current and output voltage waveforms with output current load step from 10A to 15A and 15A to 10A.



(a) Inductor current and output voltage waveforms



(b) Zoomed waveforms during transient period

Fig. 13. VSCS-MPC of current load: inductor current and output voltage waveforms with output voltage reference step from 100V to 120V and 100V to 80V.

voltage, u_x, and two state variables of output voltage, u_o, and inductor current, i_L, are shown in Fig. 10 with a prediction horizon of 5. Based on the implementing process of Fig. 9, the colored areas represent the n regions for MPC to search and optimize according to the feedback law. Specifically, the matrices H_r and K_r will lead to an active region. The matrices F_r and G_r will help calculate the optimal duty cycle for the PWM signals.

The whole controlling diagram of VSCS-MPC is shown in Fig. 11. At each sampling period of $T_{s,base}$, the frequency controller receives the measurement of inductor current from ADC and duty cycle from MPC controller. The discretized frequency (n times of $f_{s,base}$) will be generated from the frequency controller and delivered to update the carrier for the PWM signals. This mechanism will guarantee the consistency of sampling, triggering of the control and updating of the PWM. Thus, the discrete frequency bandwidth could avoid a time-varying switching frequency and improve the system stability. Also, the algorithm of the proposed VSCS-MPC method is shown in Algorithm 2.

Algorithm 2 VSCS-MPC

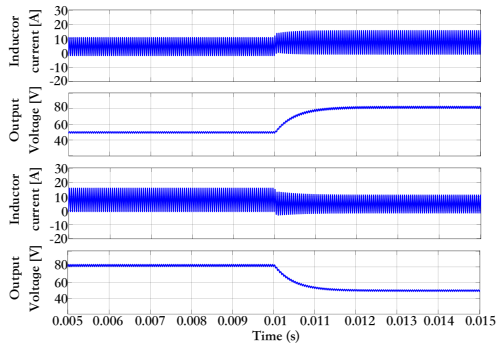
1: at each sampling period, $T_{s,base}$.
2: **while** CTRL=1 **do**
3: $ADCs \leftarrow i_L, u_o, i_o, u_s$
4: obtain U^* by solving (19)
5: $u[k] \leftarrow {u_0}^*$
6: obtain $f_{s,cal}$ by (9)-(14b)
7: obtain n by frequency algorithm 1
8: $f_{s,PWM} \leftarrow n f_{s,base}$
9: **end while**

IV. Results

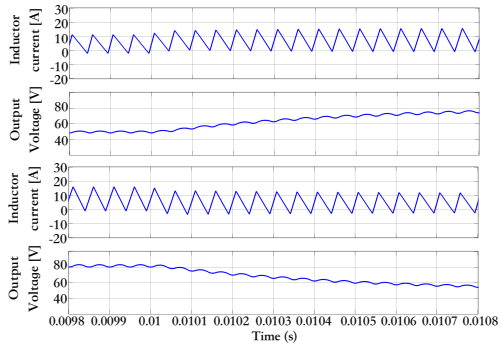
Analytical tests are implemented to verify the proposed controlling method. The simulated and experimental waveforms of VSCS-MPC and PI results are shown in this section to verify the better dynamic performance of MPC in maintaining the soft switching operation. Firstly, the VSCS-MPC is tested

TABLE I
System Parameters

Input voltage	100-200 V
Output voltage	0-200 V
Output current	0-20 A
Resistive load	11 Ω
Capacitor	36 μ F
Inductor	20, 110 μ H
Switching frequency	10-100 kHz

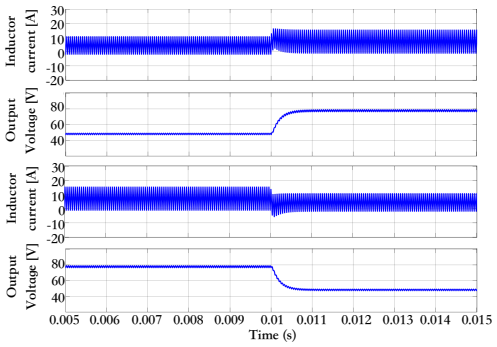


(a) Inductor current and output voltage waveforms

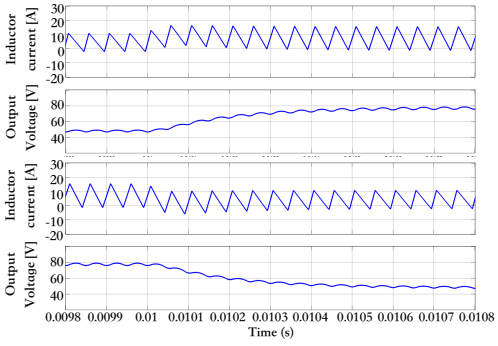


(b) Zoomed waveforms during transient period

Fig. 14. VSCS-MPC of resistive load: inductor current and output voltage with inductor current reference step from 5A to 8A and 8A to 5A.



(a) Inductor current and output voltage waveforms



(b) Zoomed waveforms during transient period

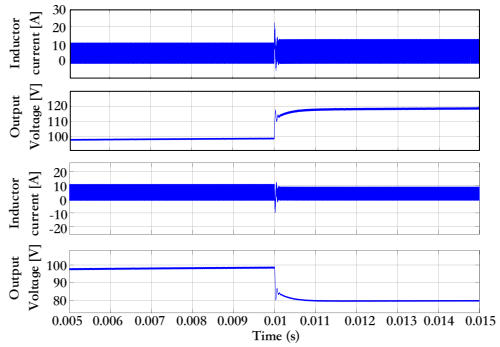
Fig. 15. VSCS-MPC of resistive load: inductor current and output voltage with output voltage reference step from 50V to 80V and 80V to 50V.

with current source load. And the simulation results are shown in Fig. 12 to Fig. 15. The parameters of the converter are: L=20μH, C=36μF, load=5-20A, U_{in}=100-200V, u_o=0-200V. And the switching frequency ranges are 30k-600kHz. The MPT tool box is used for generating the piece wise affine search tree [20]. Fig. 12 shows the inductor currents and output voltages with the current load variations from 10A to 15A and 15A to 10A, respectively. From the zoomed inductor waveforms, it can be seen that the critical soft switching operation is maintained during the transient period since the ripple currents are remained negative for soft switching turning on the upper switch. Fig. 13 shows the inductor currents and output voltages with the output voltage reference variations from 100V to 120V and 100V to 80V, respectively. Also the zoomed inductor waveforms show that the critical soft switching operation can be maintained during the transient period.

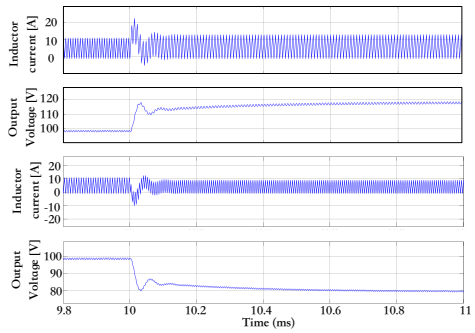
Besides the current source load, the resistive load case is also verified with simulated and experimental tests. As is shown in Table I, the parameters of the converter are: L=110μH, C=36μF, load=1-10A, U_{in}=100-200V, u_o=0-200V. And the switching frequency ranges are 10k-100kHz with 10kHz of fundamental frequency. Fig. 14 and Fig. 15 show the simulated results of inductor current control and output voltage control with VSCS-MPC. Fig. 17 to Fig. 21 represent the experimental results of inductor current and output voltage control under various testing conditions. For the inductor current control, Fig. 14 shows the inductor current reference steps from 5A to 8A and 8A to 5A in simulation. And Fig. 17, 18, 19, 20 give the experimental results of inductor current reference step from 1A to 4A, 4A to 1A, 6A to 9A and 9A to 6A, respectively. For the output voltage control, Fig. 15 shows the output voltage reference steps from 50V to 80V and 80V to 50V in simulation. Fig. 21 represents the output voltage reference steps from 80V to 50V, experimentally.

Besides the proposed VSCS-MPC results, the traditional PI controlling method is also tested for comparison. Fig. 16 shows the simulated results of output voltage reference steps from 100V to 120V and 100V to 80V with PI controller. Fig. 22 represents the experimental results of output voltage reference steps from 80V to 50V with PI controller.

It can be seen from the VSCS-MPC and PI comparison that there exists oscillation during the transient period of PI results which means the soft switching is lost. Thus, more hard switching losses will be generated. Also, the dynamic period of VSCS-MPC is shorter than the PI method. The transient period of VSCS-MPC is 0.4ms to track the references while PI is 1.8ms. And the overshoot of PI in transient is higher than VSCS-MPC. The typical soft switching performance of the upper switch is captured with drain-source voltage and gate-source voltage. The turn-on and turn-off periods in Fig. 23 show that the upper switch is zero voltage turned on. The test bench is shown in Fig. 24 for the validation of the proposed controlling method. The hardware is designed as a three-phase

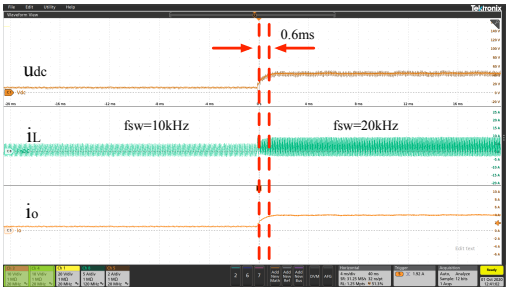


(a) Inductor current and output voltage waveforms

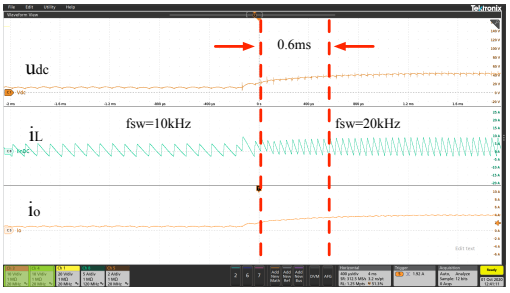


(b) Zoomed waveforms during transient period

Fig. 16. PI control (benchmark reference): Inductor current and output voltage with output voltage reference step from 100V to 120V and 100V to 80V.

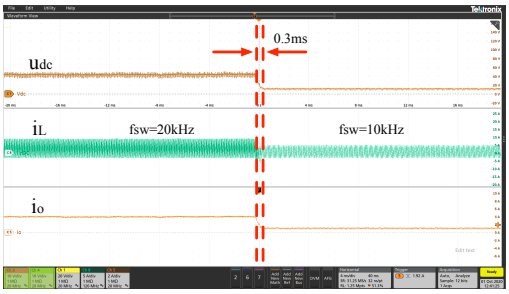


(a) Output voltage, inductor current and output current waveforms

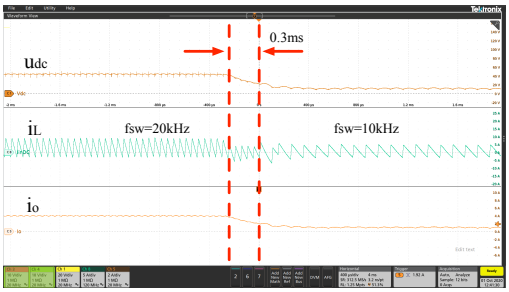


(b) Zoomed waveforms during transient period

Fig. 17. VSCS-MPC of resistive load: output voltage, inductor current and output current experimental waveforms with inductor current reference step from 1A to 4A.

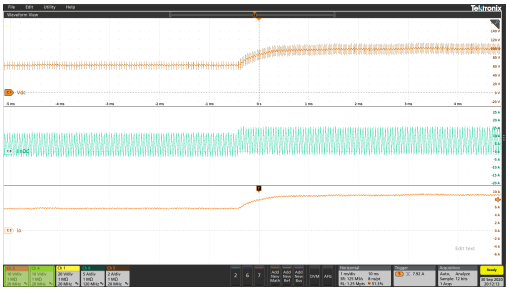


(a) Output voltage, inductor current and output current

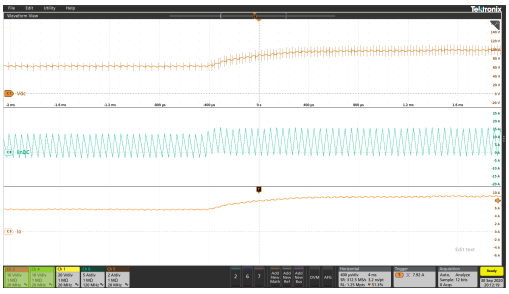


(b) Zoomed waveforms during transient period

Fig. 18. VSCS-MPC of resistive load: output voltage, inductor current and output current experimental waveforms with inductor current reference step from 4A to 1A.

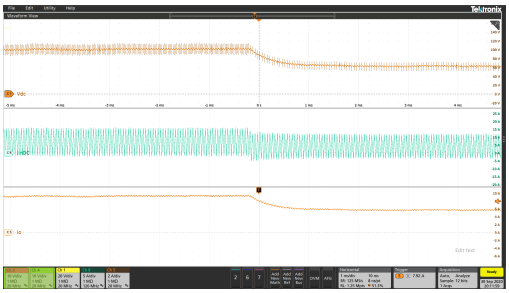


(a) Output voltage, inductor current and output current

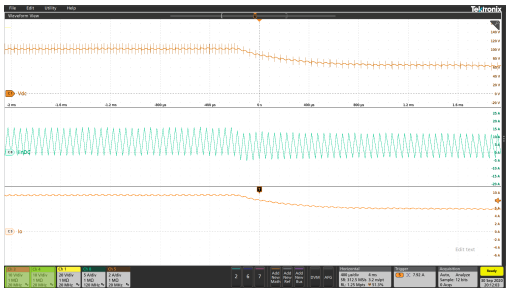


(b) Zoomed waveforms during transient period

Fig. 19. VSCS-MPC of resistive load: output voltage, inductor current and output current experimental waveforms with inductor current reference step from 6A to 9A.

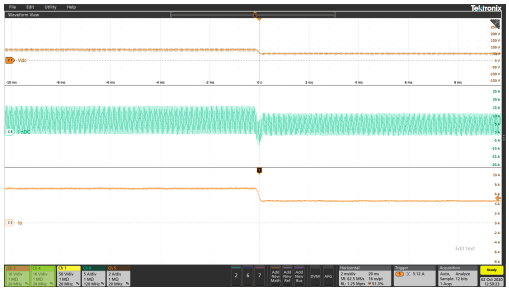


(a) Output voltage, inductor current and output current

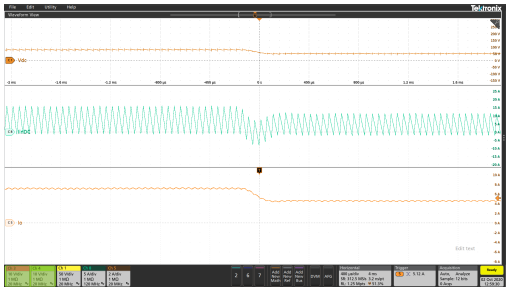


(b) Zoomed waveforms during transient period

Fig. 20. VSCS-MPC of resistive load: Output voltage, inductor current and output current experimental waveforms with inductor current reference step from 9A to 6A.

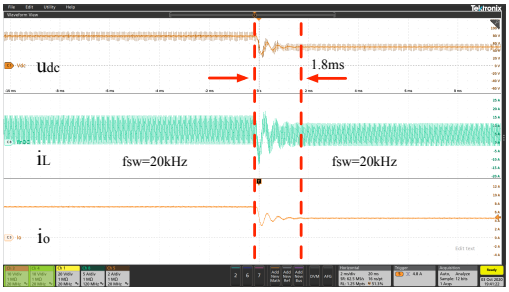


(a) Output voltage, inductor current and output current

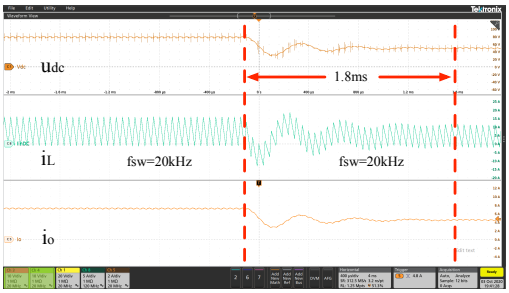


(b) Zoomed waveforms during transient period

Fig. 21. VSCS-MPC of resistive load: output voltage, inductor current and output current experimental waveforms with output voltage reference step from 80V to 50V.



(a) Output voltage, inductor current and output current



(b) Zoomed waveforms during transient period

Fig. 22. PI of resistive load: output voltage, inductor current and output current experimental waveforms with output voltage reference step from 80V to 50V.

power converter. Each phase has 2×Wolfspeed C2M0025120D SiC devices with 25mΩ $R_{ds,on}$, 2×gate drivers, one phase leg output current sensor. Also, for testing DC/DC with LC filter, a component board is connected between the converter board and the load. It includes three phase capacitors, 3 capacitor output voltage sensors and 3 output current sensors. And the

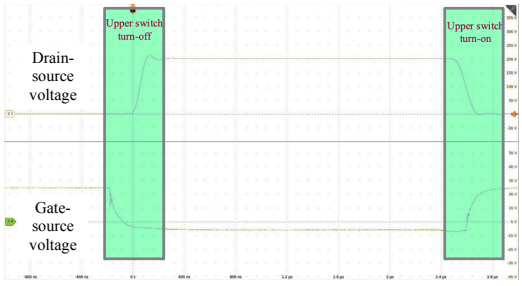


Fig. 23. Soft switching performance of upper switch during turn-on and turn-off transients.

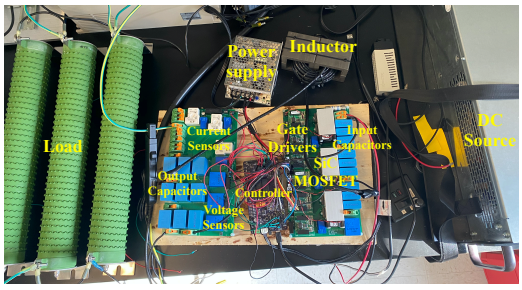


Fig. 24. Testbench of multi-phase DC/DC converter.

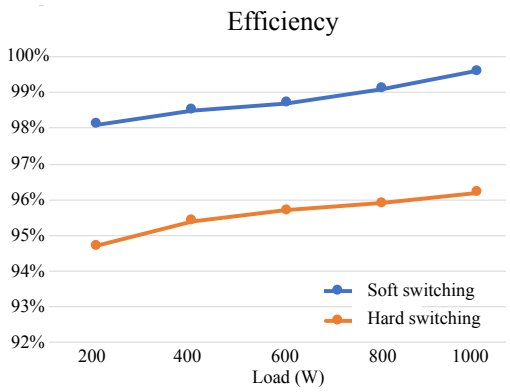
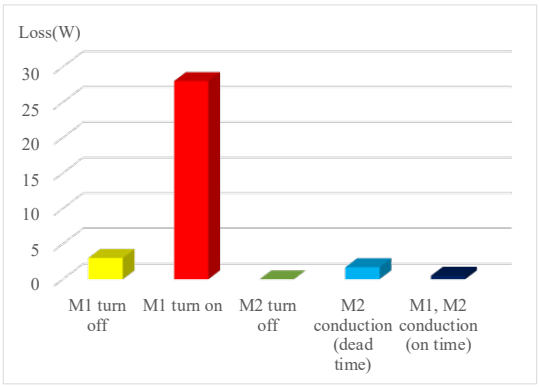
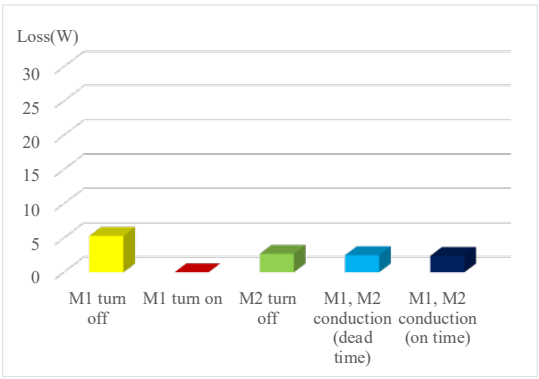


Fig. 25. Efficiency curve comparison of critical soft switching and hard switching.



(a) Hard switching break down loss distribution



(b) Soft switching break down loss distribution

Fig. 26. The switching loss break down distribution comparison of hard switching and soft switching at 1kW.

resistive load is composed of three paralleled power resistors, TE1500B33RJ. Each has 33Ω, 1.5kW. Finally, the efficiency curve comparison between critical soft switching and hard switching is drawn in Fig. 25. It can be seen that with the proposed VSCS-MPC method, the efficiency of the DC/DC converter can reach up to 99%. For further detailed analysis, the comparison of break down switching loss distribution between soft switching and hard switching is shown in Fig. 26. It can be seen the turn-on loss is much larger than other types of switching losses and dominates the hard switching which could be avoided by soft switching.

V. Conclusion

This paper proposes a VSCS-MPC method for DC/DC converter. The critical soft switching boundary conditions are derived. The switching losses are reduced under critical soft switching operation through discrete frequency controller. An equally segmented frequency bandwidth range is designed to steadily adjust the switching frequency with constant sampling period. The system stability is improved due to a fixed sampling frequency. Explicit MPC controller is designed for tracking the output voltage/current. Because of the fast response and better dynamic behavior of MPC, the hard switching is avoided during transient period compared to the traditional PI controller and the efficiency is further improved. The system volume is reduced with small inductor by applying a high switching frequency.

Acknowledgement

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