Maximizing Performance of Microelectronic Thermoelectric Generators With Parasitic Thermal and Electrical Resistances

Ruchika Dhawan, Prabuddha Madusanka, Gangyi Hu, Kenneth Maggio, *Member, IEEE*, Hal Edwards, *Member, IEEE*, and Mark Lee

***Abstract*— Microelectronic thermoelectric (TE) generators (μTEGs), which are one potential solution to powering energy autonomous integrated circuits (ICs), are often performance limited because of parasitic electrical and thermal resistances in the μTEG circuit. Parasitic performance loss can be particularly severe for μTEGs using materials with relatively low TE figure-of-merit, such as silicon (Si). In such cases, careful attention must be paid to optimizing the entire μTEG circuit, not just the TE material properties. Here, a quantitative model of μTEG device performance is developed that includes all significant electrical and thermal parasitics commonly encountered in IC-compatible μTEGs. The model gives a pair of coupled quadratic equations that can be analytically or numerically solved to determine power generation and efficiency. For given parasitic resistance and material property values, the model shows that the ratio (called here the packing fraction) of cross-sectional area occupied by TE elements to total cross-sectional area for heat flow per thermopile can be designed to maximize either power or efficiency, but not both simultaneously. For realistic material and device parameters, the optimum packing fraction is often only 1%–10%, lower than what is used in many μTEG designs. The model accounts for the reported power generation of some example μTEGs and provides guidance toward significant performance improvement.**

***Index Terms*— Energy harvesting, thermoelectric (TE), TE generators.**

I. Introduction

MANY of the miniature, low-power integrated circuit (IC) devices that form the Internet-of-Things (IoT) are meant to be deployed in difficult-to-access environments, such as *in vivo* [1] or buried in pavement [2], and so must be energy autonomous or autarkic. That is, such ICs must be energy self-sufficient by carrying their own reliable, sustainable energy source. Energy autonomy presents special difficulties for IoT devices in situations where insufficient light exists for photovoltaics and changing batteries is impractical. As a result, microelectronic thermoelectric generators (μTEGs) are being investigated [3]–[7] as one potential solution to IC energy autonomy wherever a thermal gradient is available.

Because the vast majority of commercial ICs are produced using silicon (Si) complementary metal–oxide–semiconductor (CMOS) technology, it is highly desirable for a μTEG supporting an IoT device to be integrated with the IC using the same standard Si CMOS process flow. Doped Si, however, has a low TE material figure-of-merit, $zT \sim 0.01$ near room temperature [8], which limits the TE efficiency and power generated by a Si-based thermopile. Here, $z = S^2/\rho\kappa$, where S, ρ, and κ are a material's Seebeck coefficient, electrical resistivity, and thermal conductivity, respectively, and T is the mean operating temperature (in K). The discovery that Si nanowires (SiNWs) can have zT up to 0.6 [9], [10] led to renewed interest in nanostructured Si-based μTEGs [11]–[15] that could be integrated directly with Si CMOS ICs.

Modern discrete TEGs use materials that have a high $zT \sim 1$, such as PbTe or the $(Bi,Sb)_2(Se,Te)_3$ system. However, these materials are not normally permitted in Si CMOS production lines because of concerns these elements can cross-contaminate other devices fabricated on the same wafer. While there are successful wafer-scale efforts to make discrete TEGs by growing thin-film high zT materials on Si substrates [16], [17], the methods employed are outside standard CMOS process flows and so would add difficulty and expense in any attempt to integrate high zT material-based TEGs with Si-based ICs.

Existing Si CMOS ICs designed for low-power IoT applications require voltage $\geq$1.8 V and several μW of power (i.e., current ≥ 2 μA) to operate [18]. Discrete TEGs using high zT materials can generate these voltage and power levels using heat flow cross-sectional areas of order $\sim$1 cm^2 [16], [17], [19]. However, most modern commercially available IoT ICs have a total footprint area of only a few mm^2 when fully packaged. Thus, the ideal μTEG for energy autonomy should have cross-sectional area small enough (i.e., $<$1 mm^2) to be integrated on-chip in the same process flow with the IC chip it supports. Until recently, no μTEG with area $<$1 mm^2 has met these voltage and power thresholds operating from temperature differences $\Delta T \leq 25$ K with cold-side temperature $T_C \approx 300$ K [4]–[6].

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We recently reported Si [20] and $Si_{0.97}Ge_{0.03}$ [21] μTEGs, fabricated on an industrial CMOS process line, capable of meeting these operational voltage and power thresholds using $\Delta T = 20$–24 K with $T_C = 295$ K. These μTEGs had footprint areas ≤ 0.2 mm^2, small enough to be easily integrated on a Si IC chip or within a chip package without significantly increasing the size of the packaged device. Very high voltage and power generation per unit area were obtained despite the fact that the Si and $Si_{0.98}Ge_{0.03}$ TE elements had low $zT \sim 0.01$ [22] and thus poor thermodynamic efficiency. The high voltage and power generation densities were instead achieved by optimizing the circuit-level design of the thermopile in relation to the relatively high parasitic electrical and thermal resistances inevitably encountered in small μTEG devices.

There is much existing work on how TEG device design affects performance, primarily aimed at discrete component TEGs made from bulk high zT TE materials [23]–[31]. In bulk TEGs, the electrical and thermal leads and cross-sectional areas for heat flow are large enough that parasitic series electrical and thermal resistances can often be made much smaller than the thermopile's intrinsic resistances. In addition, air is often used as the dielectric filler in a bulk thermopile, resulting in very low parallel or leakage heat flow. For bulk TEGs, this allows the use of simplifying small parameter approximations that may not be applicable to μTEGs, especially to Si-based devices.

References [27]–[31] explicitly addressed the effects of large parasitic series thermal resistances to hot and cold reservoirs in TEGs and found that power generation could be maximized by proper matching of the thermopile's intrinsic thermal resistance to the device's parasitic resistances. In particular, references [27] and [29]–[31] found that power generation at a given ΔT could be maximized using an optimal value of the packing fraction, f (also referred to as fill factor), defined as the ratio of the combined heat flow cross-sectional areas of all TE elements to the total cross-sectional area of the thermopile. Reference [27] did not also incorporate the effects of parasitic electrical resistances, while references [29]–[31] each discussed optimum f for a specific TEG design. It is, therefore, not straightforward to generalize these methods or results to generic μTEGs.

μTEGs use electrical and thermal contacts and leads having much smaller cross-sectional areas for current and heat flow compared with bulk devices. For processing and structural stability reasons, μTEGS often must use a material other than air as the dielectric filler in the thermopile. Consequently, parasitic series electrical and thermal resistances can exceed the intrinsic thermopile resistances, while thermal leakage via the dielectric spacer in the thermopile can be significant.

In this article, we adapt standard TEG heat flow equations to develop a straightforward physics-based analytic model of μTEG performance that includes all parasitic resistances relevant to most μTEG devices. This model is quite general; it can be applied to μTEGs of various geometric layouts and made with different constituent materials. The model produces a pair of coupled quadratic equations whose solution yields the power generation and efficiency. In the presence of significant parasitic series resistances and thermal leakage, we calculate the optimal packing fraction, f_{opt}, based on μTEG design layout and the physical properties of the materials used for some example Si-based μTEGs reported in the literature. Consistent with [29]–[31], we find an $f_{\text{opt}} < 1$ that maximizes generated power to a load, but we also find that a different value of f_{opt} is needed to maximize efficiency, so that power generation and efficiency cannot both be maximized by the same μTEG design.

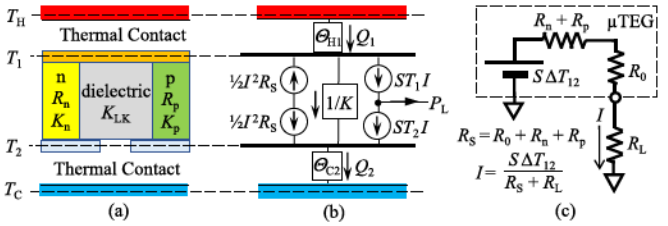

Fig. 1. (a) Block diagram illustrating a generic thermopile in a μTEG. (b) Thermal circuit model. Heat flow is indicated by arrows, heat sources by circles, and thermal impedances by rectangles. The output power to the load, P_L, is also indicated. (c) Electrical circuit model.

For Si-based μTEGs, we find f_{opt} is often between 1% and 10% for common material property and device parameter values. Many μTEG devices reported in the literature are designed with much larger values of f to boost current output, but our results indicate substantial improvement in maximum power generated or efficiency can sometimes be gained by decreasing f. In such cases, a more effective design strategy to boost current would be to connect in parallel multiple thermopiles each having optimal f, rather than using a single thermopile with nonoptimal f.

II. Model Equation With Parasitics

Fig. 1 shows (a) a block diagram, (b) a thermal circuit, and (c) an electrical circuit model of a generic μTEG thermopile. Fig. 1(a) and (b) could represent a cross-sectional view of the vertically oriented n- and p-doped TE legs of a π geometry μTEG where heat flows vertically down to a substrate acting as the cold reservoir, or a plan view of a planar geometry μTEG where heat flows horizontally through TE legs parallel to the surface of a substrate plane.

Thermally, the hot reservoir (at temperature T_H) connects to the hot side of the thermopile (at $T_1 < T_H$) via a parasitic series thermal contact resistance Θ_{H1}. The cold reservoir (T_C) connects to the cold side of the thermopile (at $T_2 > T_C$) via parasitic thermal contact resistance Θ_{C2}. Within the thermopile, heat flows from T_1 to T_2 in parallel through the n- and p-type TE legs (with thermal conductances K_n and K_p) and through the dielectric filler, which gives a parasitic parallel thermal leakage path with conductance K_{LK}.

Electrically, the n-type TE leg has resistance R_n, the p-type TE leg has resistance R_p, and there is a parasitic series resistance R_0 consisting of all electrical lead and contact resistances. The total electrical source resistance is then $R_S = R_0 + R_n + R_p$. The thermopile generates a current $I = S\Delta T_{12}/(R_S + R_L)$ flowing in series through the n- and p-type TE legs and the external load resistance R_L, where $S = S_p - S_n$ is the net thermopower of the TE legs and $\Delta T_{12} = T_1 - T_2$ is the temperature difference across the thermopile. In all real cases, the thermal resistances Θ_{H1} and Θ_{C2} are both > 0, so that $\Delta T_{12} < T_H - T_C = \Delta T$.

As shown in Fig. 1(b), the current I produces an ohmic heat flow $I^2 R_S$ inside the thermopile. Solving the Laplace heat

diffusion equation [32] shows 1/2 I^2R_S diffuses to the hot side and 1/2 I^2R_S diffuses to the cold side when the series thermal resistances $\Theta_{H1} = \Theta_{C2}$. (When $\Theta_{H1} \neq \Theta_{C2}$, I^2R_S will divide following a standard resistive current divider, but our model calculations indicate that for constant $\Theta_{\text{tot}} = \Theta_{H1} + \Theta_{C2}$, power generation and efficiency change by $< 0.5\%$ between the balanced case $\Theta_{H1} = 1/2\Theta_{\text{tot}}$ and the highly imbalanced cases $\Theta_{H1} = 0.1\Theta_{\text{tot}}$ or $\Theta_{H1} = 0.9\Theta_{\text{tot}}$.)

The standard equations for the heat flows Q_1 and Q_2 through the thermopile shown in Fig. 1(b) are derived in [32] and [33]

$$Q_1 = K\Delta T_{12} + ST_1I - \tfrac{1}{2}I^2R_S = \left[K + \frac{S^2}{R_S + R_L}T_1\right]\Delta T_{12} - \frac{1}{2}\left(\frac{S\Delta T_{12}}{R_S + R_L}\right)^2 R_S \quad (1a)$$

and

$$Q_2 = K\Delta T_{12} + ST_2I + \tfrac{1}{2}I^2R_S = \left[K + \frac{S^2}{R_S + R_L}T_2\right]\Delta T_{12} + \frac{1}{2}\left(\frac{S\Delta T_{12}}{R_S + R_L}\right)^2 R_S. \quad (1b)$$

In (1), a positive heat flow is from hot to cold and a negative heat flow from cold to hot, and the thermopile's total thermal conductance $K = K_n + K_p + K_{\text{LK}}$. The first law of thermodynamics requires the power to the load, P_L, illustrated in Fig. 1(b), to equal $Q_1 - Q_2$. It is straightforward to verify using (1) that

$$Q_1 - Q_2 = \left(\frac{S\Delta T_{12}}{R_S + R_L}\right)^2 R_L = I^2R_L = P_L \quad (2)$$

as required by energy conservation.

In steady-state operation, T_1 = constant so (1a) must equal the heat flow $(T_H - T_1)/\Theta_{H1}$ from T_H to T_1, giving

$$\frac{T_H - T_1}{\Theta_{H1}} = K\Delta T_{12}\left[(1 + Z_{\text{eff}}T_1) - \frac{1}{2}\frac{R_S}{R_S + R_L}Z_{\text{eff}}\Delta T_{12}\right] \quad (3a)$$

where $Z_{\text{eff}} = S^2/[K(R_S + R_L)]$ is the effective TE Z-parameter of the TE circuit attached to the load. The same condition applied to the cold side gives

$$\frac{T_2 - T_C}{\Theta_{C2}} = K\Delta T_{12}\left[(1 + Z_{\text{eff}}T_2) + \frac{1}{2}\frac{R_S}{R_S + R_L}Z_{\text{eff}}\Delta T_{12}\right]. \quad (3b)$$

Equations (3) are coupled quadratic equations for T_1 and T_2 in terms of the applied temperatures T_H and T_C. Given the electrical and thermal properties of all constituent materials and the geometry of the μTEG layout, solving (3) for T_1 and T_2 then determines the power generation via (2) and the thermodynamic efficiency $\eta = P_L/Q_1$ from (1a) and (2).

In several existing analyses [24]–[26], (3) are uncoupled by treating I in (1) as an independent variable. This is appropriate for TE cooler operation and for determining current–voltage response of a TEG because both measurements are usually current biased. However, when a TEG is used to generate power, the independent variables are T_H and T_C, not I. For power generation, I is explicitly determined by the solutions T_1 and T_2 to (3) for given T_H and T_C, so taking I as an independent variable is not appropriate to analyzing TEG power generation operation.

Equations (3) can in principle be solved either analytically or numerically. In our experience, the general analytic solution is mathematically awkward, while numerical solvers are straightforward, accurate, and fast because the physically relevant solutions are bounded by $T_C < T_2 < T_1 < T_H$. In what follows, we use the vpasolve function in MATLAB to solve (3) for T_1 and T_2 given values for all other parameters.

III. Example Solution of the Model

Applying (3) to any particular μTEG design involves determining the values of all extensive parameters (Θ_{H1}, Θ_{C2}, K, R_S, R_L) in terms of the intensive properties of the material sets used (i.e., κ of the TE, dielectric filler, and thermal contact materials, and ρ and S of the n- and p-type TE materials) and the geometry and dimensions of the μTEG device layout. Equations (3) show that overall μTEG performance depends on the circuit-level parameter Z_{eff}, which includes parasitic, geometric, and load contributions in addition to the TE material parameter z, which is independent of device details.

In this section, we give an example setup and solution of this model using typical parameter values from our own Si [20], [22] and $Si_{0.97}Ge_{0.03}$ [21] μTEG work. Details of these μTEG designs, fabrication, and measured performance are given in [20]–[22]. Briefly, all were "π geometry" μTEGs (i.e., vertical TE elements relative to substrate) industrially fabricated on standard 300-mm diameter Si wafers using the same process flows used to manufacture standard Si CMOS ICs. These μTEGs used n- and p-doped Si or $Si_{0.97}Ge_{0.03}$ "blade" TE legs, each individual blade having cross-sectional area of 80 nm × 750 nm and length $L = 350$ nm for electrical and thermal current flow. Multiple parallel blade elements were grouped to form a thermopile having total cross-sectional area $A = 48\ \mu\text{m} \times 36\ \mu\text{m}$ for heat flow, using SiO_2 as the filler between blades.

For Si and SiO_2, we use values of thermopowers (S_p, S_n), electrical resistivities (ρ_p, ρ_n), and thermal conductivities (κ_p, κ_n, κ_{ox}) based on literature values [21]. For $Si_{0.97}Ge_{0.03}$, $\kappa_{p,n}$ is roughly half that of Si, $\kappa_{p,n}$ is about 10% higher than that of Si, and $S_{p,n}$ is essentially equal to that of Si [22], [34]. To describe the thermopile layout geometry, we define the n- and p-type packing fractions $f_n = A_n/A$ and $f_p = A_p/A$ where A_n, A_p = total cross-sectional area of all n- or p-type TE blades in a thermopile. Our μTEGs used $f_p = 2f_n$ to roughly even out the electrical resistances on p- and n-sides of the thermopile. The total packing fraction is $f = f_n + f_p$. Then,

$$K = K_n + K_p + K_{\text{LK}} = \left[f_n\kappa_n + f_p\kappa_p + (1 - f)\kappa_{\text{ox}}\right](A/L) \quad (4)$$

and

$$R_n + R_p = \left[\rho_n/f_n + \rho_p/f_p\right](L/A). \quad (5)$$

The parasitic series resistance R_0 is determined as the difference between the measured μTEG device resistance R_S and (5); R_0 varied between 2 and 4 Ω from device-to-device. The series parasitic thermal resistance $\Theta_{H1} + \Theta_{C2}$ is determined as the difference between the measured total device thermal resistance and K^{-1} from (4). Separate values of Θ_{H1} and Θ_{C2} were modeled from layout dimensions and literature thermal conductivities of the materials used for heat exchange

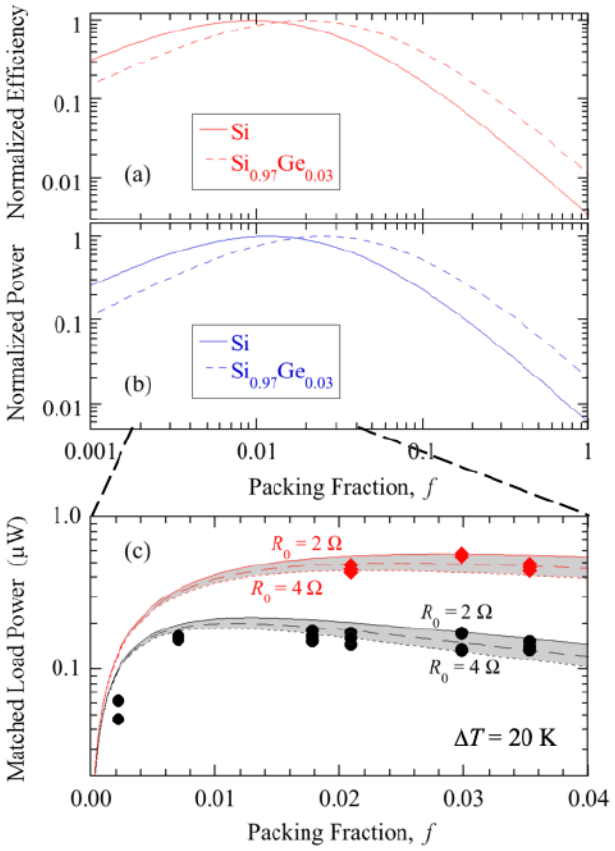

Fig. 2. Modeled matched load (a) efficiency and (b) power at $\Delta T = 20$ K, normalized to maximum versus packing fraction using representative parameters for our Si (solid curve) and $Si_{0.97}Ge_{0.03}$ (dashed curve) μTEGs as described in [20]–[22]. (c) Detail of power results for $f \leq 0.04$, comparing modeled matched load powers (curves) to measured data on Si (black circles) and $Si_{0.97}Ge_{0.03}$ (red diamonds) μTEGs. The gray-shaded regions represent modeled results lying within the 2–4-Ω spread of lead resistance values typically found in these devices.

between the T_H and T_C reservoirs and the thermopile, subject to the constraint that their sum matched the measured value of $\Theta_{H1} + \Theta_{C2}$ [20]. Because the TE blades on the cold side of the thermopile are monolithically etched from the Si wafer substrate, we found that Θ_{C2} is best modeled using a spreading resistance inversely proportional to square root of TE blade-to-substrate contact area, i.e., to $f^{1/2}$ [35].

Fig. 2 shows an example of calculated (a) efficiency η and (b) matched load power P_L (i.e., power delivered to a load resistance $R_L = R_S$, which delivers maximum power to the load), both normalized to their maximum values versus total packing fraction f for Si and $Si_{0.97}Ge_{0.03}$ μTEG devices using the device layout geometry detailed in [20]–[22]. In Fig. 2(a), the actual maximum efficiencies are $(0.8 \times 10^{-4})\eta_C$ for the Si device and $(1.7 \times 10^{-4})\eta_C$ for the $Si_{0.97}Ge_{0.03}$ device, where $\eta_C = 0.0635$ is the ideal Carnot efficiency of a heat engine operating between 315 and 295 K. Fig. 2(a) and (b) shows that the model predicts an optimal packing fraction f_{opt} near 0.01 for the Si μTEGs that maximizes either P_L or η. Because η of $Si_{0.97}Ge_{0.03}$ is a factor of two lower than that of Si, the calculated f_{opt} for $Si_{0.97}Ge_{0.03}$ μTEGs is closer to 0.03. For both materials, f_{opt} that maximizes P_L is slightly higher than f_{opt} that maximizes η, meaning that P_L and η cannot be simultaneously maximized with the same design.

Fig. 2(c) shows a comparison of the modeled P_L versus f to original data taken by us on several Si and $Si_{0.97}Ge_{0.03}$ μTEG devices. All of these devices having the same layout geometry and dimensions, differing only in number of TE blade elements per thermopile and hence f. Multiple data points at the same f represent data from separate but nominally identical μTEG devices and represent the typical spread in measured power. The gray-shaded regions indicate computed results lying within the 2–4-Ω spread of parasitic R_0 encountered in these devices. This plot shows that the measured P_L values are consistent with the model's calculation and with an optimal packing fraction of a few percent for power generation.

The results reported in [20] and [21] showed area power generation densities (P_L/A) at given ΔT substantially higher than reported for any other Si-based μTEGs and comparable with the best reported $(Bi,Sb)_2(Se,Te)_3$-based μTEGs. This is despite Si having a much lower TE figure-of-merit zT. One reason for the enhanced power performance of our Si-based μTEGs is that our designs used unconventionally low packing fractions $f \sim 0.01$ that are close to the calculated f_{opt} for power generation. If our μTEGs used the larger packing fraction values $f \sim 0.5$ commonly seen in other reported works, then Fig. 2(b) indicates power performance would degrade by a factor of 20–50×.

When Θ_{H1}, $\Theta_{C2} > 0$ and $\kappa_n + \kappa_p > \kappa_{LK}$, a maximum in P_L at some $f_{opt} < 1$ may be expected physically for the following reason. As $f \to 0$, the area for TE current vanishes so $I \to 0$ and $P_L = I^2 R_L \to 0$. However, as $f \to 1$, more heat is conducted through the TE elements, decreasing ΔT_{12} whenever Θ_{H1} or $\Theta_{C2} > 0$. This decreases the TE voltage $S\Delta T_{12}$ and again brings down $P_L = (S\Delta T_{12})^2/R_L$. Thus, P_L versus f should go through a maximum at some $0 < f < 1$. From this physical picture, μTEG devices using higher κ_n and κ_p (and hence lower zT) TE materials will have lower f_{opt} to prevent a rapid collapse of ΔT_{12} at high f.

IV. Implications for Other μTEGs

Given that parasitic resistances may not be reduced to negligible levels in real μTEGs, our model describes a path toward improving performance by calculating the optimum f for any given device layout geometry and dimension. This is especially important in Si-based μTEGs that are CMOS process compatible because Si's relatively high $\kappa_{n,p}$ may result in the parasitic series thermal resistances dominating the thermal resistance of the μTEG device. However, as pointed out in [31], these conclusions are also relevant for any TEG having high series thermal resistance.

Li *et al.* [11] reported μTEGs using lithographically etched 1-μm-long SiNW arrays. They gave detailed information on device geometry and dimensions, quoted standard thermal device geometry and dimensions, and quoted standard thermal and electrical material property values for the constituent materials used. They reported generating a matched load power of 0.47 μW at an applied temperature difference of $\Delta T = 70$ K using 162 thermopiles connected in series covering a total cross-sectional area for heat flow of 5 mm × 5 mm. Their devices had parasitic series thermal resistances that were significantly higher than a thermopile's intrinsic resistance, causing only a small fraction of the applied ΔT to appear across the thermopile itself, thus degrading their power

generation performance. Using the parameter values given in [11], our model computes a matched load power generation of 0.6 μW using $T_C = 295$ K and $T_H = 365$ K, reasonably close to their measured value especially considering possible variances between the stated and actual material property values.

Using our model, we further computed both P_L and η as a function of packing fraction f for 1-μm length SiNWs used in [11]. The results for computed P_L and η, normalized to their maximum values, are shown in Fig. 3(a). The calculation gives f_{opt} near 0.001 for both P_L and η. This is much smaller than the $f = 0.6$ used. Interestingly, the expected performance gain from reducing f so that it becomes closer to f_{opt} is very large: a $\sim 400\times$ increase in P_L and $\sim 700\times$ increase in η. This result emphasizes the importance of optimizing f, given the length of TE element used, to match the thermal resistance of the TE elements to the parasitic leakage and series thermal resistances.

More recently, Elyamny *et al.* [15] reported μTEGs using metal-assisted chemically etched SiNW forests having very low intrinsic thermal conductivity and with air as the dielectric filler so as to minimize K_{LK} and increase the thermopile's thermal resistance K^{-1}. Using 13.5-μm-long SiNWs with reported thermal conductivity $\kappa_{NW} = 1.8 \pm 0.3$ W·m^{-1}·K^{-1}, they generated a matched load power of about 9 μW at an applied temperature difference of $\Delta T = 20$ K over a total cross-sectional area for heat flow of 0.077 cm^2. They measured the total thermal resistance of the device to be $\Theta_{tot} = 9.2$ K·W^{-1}. Using their given geometry and dimensions and imposing the requirement $\Theta_{tot} = 9.2$ K·W^{-1}, our model matches their 9-μW power generation with $T_C = 295$ K and $T_H = 315$ K if we use $\kappa_{NW} = 2.1$ W·m^{-1}·K^{-1}, which is within their reported measurement uncertainty.

Using our model, we further computed both P_L and η as a function of packing fraction f for the 13.5-μm length SiNWs used in [15]. The results for modeled P_L and η, normalized to their maximum values, are shown in Fig. 3(b). The calculation gives f_{opt} near 0.18 for P_L and 0.09 for η. These values of f_{opt} are much larger than for [11] or for our μTEGs from Section III because Elyamny *et al.* [15] used a thermopile having thermal resistance K^{-1} much higher relative to the parasitic Θ_{tot} and have negligible leakage heat loss. f_{opt} here is comparable with the $f = 0.14$ actually used. Our model predicts that increasing f to 0.18 will result in about an 8% improvement in matched load power generated, and decreasing f to 0.09 will result in about an 8% improvement in efficiency.

While this model is most useful for μTEGs either using low zT materials or having high parasitic resistances, it is applicable to devices using any TE material given knowledge of the material set's properties as well as the device geometry and parasitics. μTEGs using high zT materials can have larger f_{opt} values due to the low $\kappa_{n,p}$ of the TE materials, so a thermopile's thermal resistance K^{-1} is less likely to be dominated by a given parasitic Θ_{tot}.

For example, using the device and material parameters from Böttner *et al.* [36] for a π geometry $Bi_2Te_3/(Bi,Sb)_2Te_3$ μTEG, our model gives $f_{opt} \approx 0.1$ for P_L and ≈ 0.04 for η [see Fig. 3(c)]. This is lower than the $f \approx 0.5$ actually used. Our model shows that P_L could double and η could increase by $\sim 6\times$ if f were decreased from 0.5 to f_{opt} in their thermocouple design. (Because Böttner *et al.* [36] lacked information on Θ_{tot}, we first used our model to determine what matched load power they would ideally generate at $\Delta T = 9$ K using the parasitic R_0 and K_{LK} given in [36] but with $\Theta_{tot} = 0$. We then determined what Θ_{tot} value would be necessary to reduce the power to a level equal to their measured power per thermopile.)

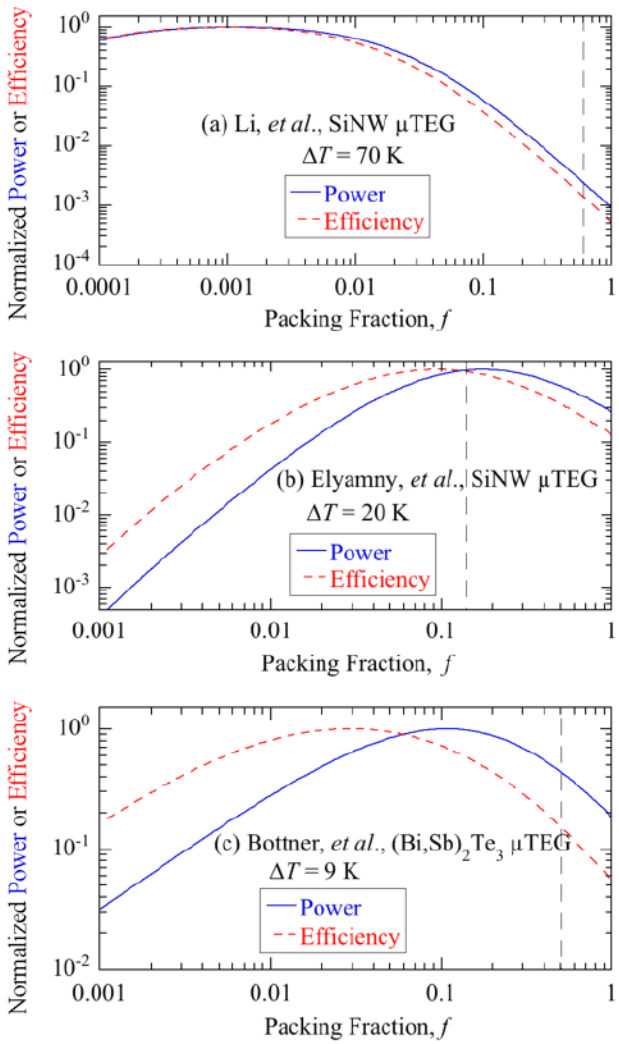

Fig. 3. Modeled matched load powers and efficiencies, normalized to maximum values, versus packing fraction for (a) SiNW μTEG, using parameters from [11], (b) SiNW μTEG, using parameters from [15], and (c) (Bi,Sb)2Te3 μTEG, using parameters from [36]. Black vertical dashed lines indicate packing fraction used in [11], [15], and [36].

V. Conclusion

A quantitative model has been developed for μTEG power generation and efficiency performance including all parasitic electrical and thermal resistances important to real μTEGs. This model shows that for μTEGs using relatively high thermal conductance TE elements such as Si, or having high series thermal resistance, there exists an optimal packing fraction $f < 1$ that maximizes either matched load power or efficiency. Many μTEGs reported in the literature use f significantly larger than optimal. Modeling results suggest that in these cases, P_L or η could be improved substantially by simply going to a thermocouple layout with lower packing fraction.

Thermocouple designs with lower f may improve P_L and η but decreasing f always generates smaller current per

thermocouple. For many applications, a minimum current output is required. Historically, the conventional way to boost current output has been to use thermocouple designs with higher f. Our model suggests that in many, though not all, cases, a superior way to boost current while maximizing power or efficiency in a μTEG is to use a smaller f thermocouple layout and increase current by connecting multiple such thermocouples in parallel.

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