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Mechanics of crack path selection in microtransfer printing: Challenges and opportunities for process control

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ABSTRACT

Microtransfer printing is a manufacturing technique that relies on controlled selective delamination between two interfaces to transfer thin solid films and chips. Stamps in these processes are often designed to leverage strategies that modify the interfacial stress distribution at the stamp interface to achieve a specific adhesion response, however the effect of a modified stress distribution at the stamp interface on crack path selection between the two interfaces in the system is unclear. This paper investigates how the stress distribution beneath the stamp can affect the delamination path between the two interfaces in a microtransfer printing process using mechanics modeling. In general, altering the stress distribution at the stamp/chip interface also alters the stress distribution at the chip/substrate interface. For a sufficiently thin chip with no or small initial defects at the interfaces, the common approach of tuning adhesion by reducing the strength of stress singularity near the edge of the stamp does not provide a robust route to control the delamination path. An alternative stamp design strategy, guided by the singularity order of the stress distribution, is proposed and analyzed. In the proposed stamp design, the delamination path can be controlled through the stamp thickness and the application of a shear displacement. This work provides a fundamental understanding of the mechanics of the microtransfer printing process as well as guidance for designing successful microtransfer printing processes.

1. Introduction

Microtransfer printing is a manufacturing technique in which solid thin films, semiconductor chips, and microstructures are retrieved from a donor substrate and subsequently printed onto a receiver substrate using a stamp. The most common implementation of microtransfer printing uses a compliant elastomer stamp to retrieve and print thin components. Microtransfer printing allows microstructures and devices fabricated in different processes to be integrated with one another or onto unconventional substrates, enabling the fabrication of flexible electronics (Meitl et al., 2006; Kim et al., 2010; Carlson et al., 2012), advanced photovoltaic cells (Sen et al., 2018) and 3D microstructures (Ahn et al., 2006). Mechanics plays a central role in the success of microtransfer printing processes as delamination at specific interfaces must be realized in different steps of the process. During the retrieval step, the stamp-chip interface must be "stronger" than the chip-substrate interface, thus allowing for delamination of the chip from the donor substrate when the stamp is retracted. The opposite must be true in the printing step to transfer the chip from the stamp to the receiver substrate.

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Various strategies have been developed to realize delamination along specific interfaces in microtransfer printing process. One of the most common strategies is the use of loading rate to *modify the critical energy release rate* at the stamp-chip interface. As described in Meitl et al. (2006) and Feng et al. (2007), the rate-dependent critical energy release rate of a soft elastomer stamp is leveraged by fast peeling in the retrieval step to achieve high critical energy release rate at the stamp-chip interface and conversely, in the printing step, the stamp is peeled slowly such that the critical energy release rate at the stamp-chip interface is low. The second strategy that has been used is *tuning the elastic modulus* of the stamp. An elementary fracture mechanics analysis shows that the effective failure strength of an adhered contact scales with the critical energy release rate and the elastic modulus (Anderson, 2005). As a result, a stamp with tunable modulus can be used for retrieval in its stiff state, and for printing when in its soft state. The modulus of shape memory polymers can change by ~1000 times due to external stimulus such as heat and several studies have demonstrated the use of shape memory polymer stamps for high-yield microtransfer printing (Eisenhaure et al., 2015; Eisenhaure and Kim, 2016; Huang et al., 2016). The third primary strategy is *modification of the contact area* between retrieval and printing via structured stamps (Kim et al., 2010; Wu et al., 2011). In this approach, a compressive force presses the regions between the microtips into contact with the chip in the retrieval step, resulting in a large contact area and high adhesion between the stamp and chip. Then, prior to the printing step, the stamp elastically retracts to its original shape and only contacts the chip at the microtips, allowing for printing to low adhesive surfaces.

In addition to the three approaches discussed above, another important strategy for controlling adhesion is *modification of the interfacial stress distribution* via stamp geometry or loading configuration. When an adhered interface between two dissimilar materials is loaded, there is a singular stress field at the edge of the contact. The stress singularity in this region plays a key role in determining the load at which interface failure occurs (Akisanya and Fleck, 1997; Khaderi et al., 2015; Balijepalli et al., 2016 and R.G. 2017). Approaches to modify the interfacial stress distribution to reduce the stress in the edge singularity zone have been investigated in the design of dry bioinspired adhesives. Notably, mushroom-shaped pillars have a reduced stress concentration near the edge of the pillar and result in enhanced adhesion compared to simple cylindrical pillars (Kim and Sitti, 2006; del Campo et al., 2007; Greiner et al., 2007; Carbone et al., 2011; Balijepalli et al., 2016; Hensel et al., 2018). Kim et al. (2012) exploited the high adhesion strength of mushroom-shaped pillars to increase retrieval yield in microtransfer printing. Similarly, a composite pillar with a stiff core and compliant shell (Minsky and Turner, 2015, 2017) or a stiff pillar terminated with a compliant tip (Fischer et al., 2016; Balijepalli et al., 2017) reduces the stress concentration in the vicinity of the pillar edge and increases the effective adhesion strength. The thickness of the soft tip layer relative to the pillar radius is critical in determining the interfacial stress distribution and thus adhesion strength. Minsky and Turner (2017) used 200 μm wide composite square pillars in a microtransfer printing process to retrieve and print thin Si membranes. On a larger scale, Bartlett and Crosby (2014) exploited the dependence of adhesion strength on the soft layer thickness and demonstrated the reliable transfer of stiff chips from a soft layer of given thickness to a thinner soft layer due to the difference in stress distribution at the two interfaces. Besides tailoring the shape or composition of the pillar, the interfacial stress distribution can also be modified by introducing subsurface pressure or applying different types of loads. Inflatable stamps and subsurface pressure have been applied to deform the stamp and induce an interfacial stress distribution that facilitates printing (Carlson et al., 2012; Linghu et al., 2019). Finally, Carlson et al. (2011), Minsky and Turner (2017) and Sen et al. (2018) exploited a different loading configuration, namely an applied lateral (i.e. shear) load on the top of the stamp, which produces a moment on the interface and generates a large stress at one edge of the stamp-chip interface to facilitate detachment in the printing step.

As described above, the enhancement and tuning of adhesion through modification of the interfacial stress distribution has been widely pursued in microtransfer printing and the mechanics have been studied. However, most of the analyses to date have only focused on the stress distribution and the adhesion at the stamp-chip interface and have assumed that enhanced adhesion at this interface facilitates retrieval while reduced adhesion facilitates printing (Carlson et al., 2011 and 2012; Cheng et al., 2012; Kim et al., 2012; Minsky and Turner, 2017; Linghu et al., 2019). However, microtransfer printing is often used to transfer thin and flexible components and the stress distribution at the stamp-chip interface also affects the stress distribution at the chip-substrate interface. Microtransfer printing processes are controlled by a competition between delamination along the stamp-chip and chip-substrate interfaces and, in general, the adhesion of both interfaces must be considered simultaneously when designing strategies to improve microtransfer printing processes through adhesion tuning. Tucker et al. (2009) and Kim-Lee et al. (2014) analyzed the competing delamination along the two interfaces for a system consisting of a thin chip sandwiched between a stamp and a substrate. While these studies examined the mechanics of crack path selection in this system from a fracture perspective, they did not specifically investigate how the interfacial stress distribution could be altered through stamp design or loading to create favorable retrieval or printing conditions.

In this paper, the effect of modifying the interfacial stress distribution on the delamination path between two interfaces in a microtransfer printing process is investigated. Cases with perfectly-bonded interfaces and pre-cracked interfaces are studied. The system studied is schematically shown in Fig. 1(a), a thin chip is sandwiched between a soft stamp and a stiff substrate. It is found that, in general, altering the stress distribution at the stamp-chip interface (referred to as the "upper interface") also alters the stress distribution at the chip-substrate interface (referred to as the "lower interface"). For a sufficiently thin chip with no or small defects at the interfaces, modifying the interfacial stress distribution at the stamp interface affects the overall adhesion, but does not provide a path to control the delamination path as both the upper and lower interfaces are affected similarly by the altered stress distribution. In order to control the delamination path, we propose and analyze a stamp design strategy guided by the leading order of the stress singularity at the stamp edge.

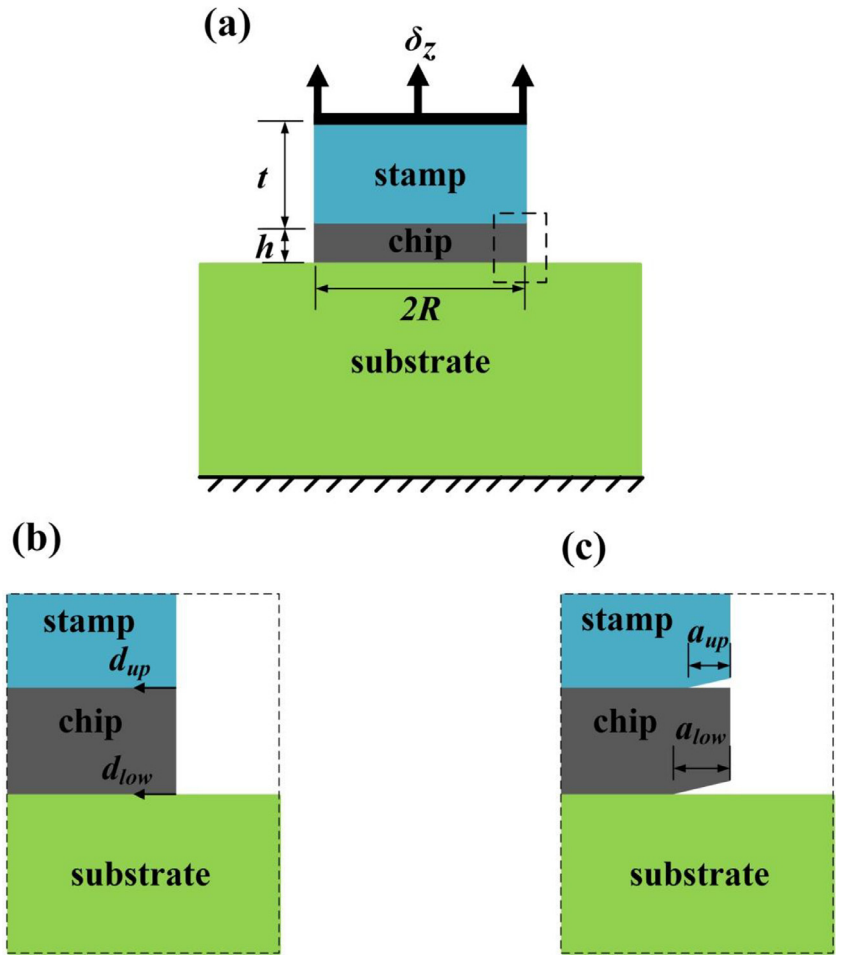

Fig. 1. (a) Schematic of the microtransfer printing process. A thin chip is sandwiched between a compliant stamp and a stiff substrate with displacement applied at the top of the stamp. Two different cases for the edge geometry, noted with a dashed box in (a), are considered: (b) Perfectly-bonded interfaces. (c) Interfaces with pre-cracks (i.e. defects) at the edge.

2. Mechanics framework

A microtransfer printing process with a Si chip (Young's modulus E_c=150 GPa and Poisson's ratio v_c=0.18), a Si substrate (Young's modulus E_{su}=150 GPa and Poisson's ratio v_{su}=0.18), and an elastomer stamp (Young's modulus E_{st}=2 MPa and Poisson's ratio v_{st}=0.49), as shown in Fig. 1(a), is considered. There are two interfaces in the system and which interfaces delaminates first determines whether it is a printing or retrieval process. At the upper interface, a nearly incompressible elastomer is in contact with much stiffer Si (~7.5 $\times$ 10^4 times stiffer); and at the lower interface, a Si chip is in contact with a Si substrate. All the materials studied in this work are assumed to be isotropic and linear elastic and the process is analyzed using a framework based on linear elastic interface fracture mechanics. Though a microtransfer printing process can be modeled as a 2D plane strain problem (representative of microtransfer printing rectangular chips), most of the cases examined in this work are for a 2D axisymmetric geometry (representative of transferring circular chips) in which a crack initiates from the edge. Because the stress field in the vicinity of the edge (or in the center) of the interface is in a state of plane strain for both axisymmetric and plane strain, the mechanics and equations developed in this section are identical for both axisymmetric and plane strain conditions (Khaderi et al., 2015; R.G. Balijepalli et al., 2017).

For the analysis of interfaces between dissimilar materials, it is convenient to describe the elastic mismatch between the two adherends (denoted with subscripts 1, 2) in terms of the Dundur's parameters (Dundurs, 1969)

$$\alpha = \frac{\mu_1(\kappa_2+1)-\mu_2(\kappa_1+1)}{\mu_1(\kappa_2+1)+\mu_2(\kappa_1+1)}, \quad \beta = \frac{\mu_1(\kappa_2-1)-\mu_2(\kappa_1-1)}{\mu_1(\kappa_2+1)+\mu_2(\kappa_1+1)} \tag{1}$$

where κ_i=3–4v_i and v_i is the Poisson's ratio and μ_i is the shear moduli with i = 1, 2. Generally, $-1<\alpha<1$ and $-1+4\alpha<\beta<1+4\alpha$ (Hutchinson and Suo, 1991). For the specific system studied in this work, $\alpha\approx-1$ and $\beta\approx0$ for the upper interface, and $\alpha=\beta=0$ for the lower interface.

2.1. Wedge singularity

In microtransfer printing, delamination often initiates at edge of the interfaces and propagates inwards (Tucker et al., 2009; Carlson et al., 2011; Kim-Lee et al., 2014). Analysis of the delamination at the edges is therefore essential to understand crack path selection in a microtransfer printing. The upper and lower interfaces (Fig. 1(b)) can be viewed as two wedge contacts. In a perfectly bonded wedge contact, a singular stress field exists at the edge of the interface and is given as (Khaderi et al., 2015)

$$\begin{aligned}\sigma_{zz} &= H_1 d^{\lambda_1 - 1} + H_2 d^{\lambda_2 - 1} \\ \sigma_{rz} &= H_1 d^{\lambda_1 - 1} f_{rz}(\lambda_1) + H_2 d^{\lambda_2 - 1} f_{rz}(\lambda_2)\end{aligned} \tag{2}$$

where λ_1 and λ_2 is the *order of the stress singularity at edge* whose values depends on the α, β and the wedge angle of the contact; H_1 and H_2 are the *magnitudes of the edge singularity* corresponding to λ_1 and λ_2 that depend on the external boundary condition and the entire geometry; d is the distance from the wedge and $f_{rz}(\lambda_1)$ and $f_{rz}(\lambda_2)$ describe the ratio of σ_{rz}/σ_{zz}. λ_1 and λ_2 lie within the interval [0.5, 1] and $\lambda_1 \leq \lambda_2$. Since λ_1 is the leading order singularity, we only keep λ_1 and the stress field associated with λ_1: $\sigma_{zz}=H_1 d^{\lambda_1 - 1}$ and $\sigma_{rz}=H_1 d^{\lambda_1 - 1} f_{rz}(\lambda_1)$ as the singular stress field; and λ_1 is defined as the *leading order of stress singularity at edge*. The singular stress field dominant region at the edge is defined as the *edge singularity zone* and its length along the interface is defined as the *length of the edge singularity zone, d_{len}*. For the specific upper interface and lower interface wedges considered in this work (Fig. 1(b)), λ_1 is found to be 0.60 for the upper interface and 0.54 for the lower interface by solving the characteristic equations of a wedge contact problem (Khaderi et al., 2015). Thus, from Eq. (2), the stress distribution within the edge singularity zone at the upper interface is

$$\begin{aligned}\sigma_{zz} &= H_{up} d_{up}^{-0.40} \\ \sigma_{rz} &= 0.51 H_{up} d_{low}^{-0.40}\end{aligned} \tag{3}$$

and the stress distribution within the edge singularity zone at the lower interface is

$$\begin{aligned}\sigma_{zz} &= H_{low} d_{low}^{-0.46} \\ \sigma_{rz} &= 0.54 H_{low} d_{low}^{-0.46}\end{aligned} \tag{4}$$

where H_{up} is the magnitude of the edge singularity at upper interface and H_{low} is the magnitude of the edge singularity at the lower interface. The values of H_{up} and H_{low} can be determined from finite element (FE) calculations. d_{up} is the distance from the upper interface wedge and d_{low} is the distance from the lower interface wedge as shown in Fig. 1(b).

Generally, interfaces are not perfectly bonded and defects result in pre-cracks at the edge as shown in Fig. 1(c). When an edge crack with length a is embedded in this edge singularity zone (i.e. $a < d_{len}$), the stress intensity factor K is related to H_1 by (Khaderi et al., 2015):

$$K a^{i\varepsilon} = C H_1 a^{\lambda_1 - 1/2} \tag{5}$$

where C is a constant that depends on the α, β and the wedge angle of the contact, and ε is

$$\varepsilon = \frac{1}{2\pi} \ln \frac{1-\beta}{1+\beta}. \tag{6}$$

The energy release rate G is (Hutchinson and Suo, 1991)

$$G = \frac{1-\beta^2}{E^*} |K|^2 \tag{7}$$

where

$$\frac{1}{E^*} = \frac{1+\kappa_1}{16\mu_1} + \frac{1+\kappa_2}{16\mu_2}. \tag{8}$$

For the upper interface considered, $\beta = 0$, thus $\varepsilon = 0$ and

$$G_{up} = \frac{C_{up}}{E_{up}^*} H_{up}^2 a_{up}^{0.20}. \tag{9}$$

For the lower interface considered, $\beta = 0$ too and

$$G_{low} = \frac{C_{low}}{E_{low}^*} H_{low}^2 a_{low}^{0.08}. \tag{10}$$

where $E_{up}^* = 5.26$ MPa and $E_{low}^* = 155$ GPa are the moduli calculated from Eq. (8) for the upper and lower interfaces. C_{up} and C_{low} are constants obtained from numerical simulations which are identical for both plane strain and axisymmetric conditions (Khaderi et al., 2015); and a_{up} and a_{low} are the upper and lower interfaces crack lengths as shown in Fig. 1(c). Eqs. (9) and (10) only hold for edge cracks embedded in the corresponding edge singularity zone. If the edge crack is longer than the length of the edge singularity zone or delamination initiates at the center of the interfaces, the strain energy release rate must be obtained directly from numerical simulations.

Table 1
Parameters of the microtransfer printing system.

	Young's modulus	Poisson's ratio	Radius	Thickness or height
Stamp	E_{st}=2 MPa	ν_{st}=0.49	R = 50 μm	t = 100, 50, 20, 10 μm
Chip	E_c=150 GPa	ν_c=0.18	R = 50 μm	h = 10, 1, 0.1 μm
Substrate	E_{su}=150 GPa	ν_{su}=0.18	>250 μm	>250 μm

2.2. Criteria for determining the delamination path in microtransfer printing

For perfectly bonded interfaces as shown in Fig. 1(b), the magnitude of the edge singularity (H_{up} and H_{low}) can be used to assess edge initiated failure (Akisanya and Fleck, 1997; Khaderi et al., 2015; Balijepalli et al., 2016 and 2017). For the microtransfer printing problem considered here, the upper interface will fail when $H_{up} \geq H_{up\text{-}c}$, where $H_{up\text{-}c}$ is the critical magnitude of the edge singularity of the upper interface; and the lower interface will fail when $H_{low} \geq H_{low\text{-}c}$, where $H_{low\text{-}c}$ is the critical magnitude of the edge singularity of the lower interface. In a retrieval process, the lower interface fails before the upper interface. In a printing process the upper interface must fail before the lower interface. Which interface fails first is determined by comparing H_{up}/H_{low} and $H_{up\text{-}c}/H_{low\text{-}c}$. If

$$H_{up}/H_{low} > H_{up-c}/H_{low-c} \quad \text{or} \quad \frac{H_{up}/H_{up-c}}{H_{low}/H_{low-c}} > 1 \tag{11}$$

the upper interface delaminates and it is a printing process. Alternatively, if

$$H_{up}/H_{low} < H_{up-c}/H_{low-c} \quad \text{or} \quad \frac{H_{up}/H_{up-c}}{H_{low}/H_{low-c}} < 1 \tag{12}$$

the lower interface delaminates and it is a retrieval process.

When pre-cracks are present, a similar energy release rate (G_{up} and G_{low}) based criterion can be used to predict interfacial delamination. The upper interface delaminates when the energy release rate $G_{up} \geq G_{up\text{-}c}$, where $G_{up\text{-}c}$ is the critical energy release rate of the upper interface; and the lower interface delaminates when $G_{low} \geq G_{low\text{-}c}$, where $G_{low\text{-}c}$ is the critical energy release rate of the lower interface. If

$$G_{up}/G_{low} > G_{up-c}/G_{low-c} \quad \text{or} \quad \frac{G_{up}/G_{up-c}}{G_{low}/G_{low-c}} > 1 \tag{13}$$

the upper interface delaminates and it is a printing process. Alternatively, if

$$G_{up}/G_{low} < G_{up-c}/G_{low-c} \quad \text{or} \quad \frac{G_{up}/G_{up-c}}{G_{low}/G_{low-c}} < 1 \tag{14}$$

the lower interface delaminates and it is a retrieval process (Tucker et al., 2009; Kim-Lee et al., 2014). Eqs. (13) and (14) hold for both edge and center cracks.

3. Finite element modeling

The baseline case considered in this work consists of a circular chip with radius R = 50 μm, various thicknesses of h = 10 μm, 1 μm and 0.1 μm, placed on a sufficiently large substrate (at least 250 μm in radius and thickness that can be regarded as an elastic half-space). A circular stamp with a lateral dimension matching the chip and various stamp heights, t = 10 μm, 20 μm, 50 μm and 100 μm, is in contact with the chip (Fig. 1). The radius of the stamp is chosen to match that of the chip as this is typically used to enable precise manipulation of individual chips in the microtransfer printing process (i.e., this stamp geometry allows a stamp to be used to selectively retrieve a single chip from a dense array) and has been widely used in past studies (Kim et al., 2012; Minsky and Turner, 2017; Carlson et al., 2011; Cheng et al., 2012; Tucker et al., 2009; Kim-Lee et al., 2014). The finite thickness of the stamp is similar to the experimental configurations used by Bartlett and Crosby (2014) and Minsky and Turner (2017) to passively control the delamination path through the stamp thicknesses. An actively controlled implementation of such a design has also been achieved by tuning the subsurface stiffness of a composite system (Tatari et al., 2018). The stamp, chip, and substrate are defined to have the elastic properties noted in Section 2. Table 1 summarizes these parameters.

The boundary conditions and loading are summarized in Fig. 1(a). The bottom of the substrate was fixed in all directions. At the top of the stamp, the displacement was constrained in radial direction and a uniform displacement was applied in the z-direction. This boundary condition at the top of the stamp was used because in a printing tool the soft elastomer stamp is typically bonded to a rigid platen that is controllably displaced. The stamp-chip interface (upper interface) and the chip-substrate interface (lower interface) were modeled as perfectly bonded by applying appropriate tie constraints to all of the nodes at the interface. For cases where pre-cracks exist, a pre-crack with length (a_{up}) at the upper interface and/or (a_{low}) at the lower interface is prescribed at the edge or center of the interfaces by removing the tie constraint between nodes within the crack region. The energy release rate for the upper interface crack (G_{up}) and lower interface crack (G_{low}) are calculated via the virtual crack closure technique (VCCT) (Krueger, 2004).

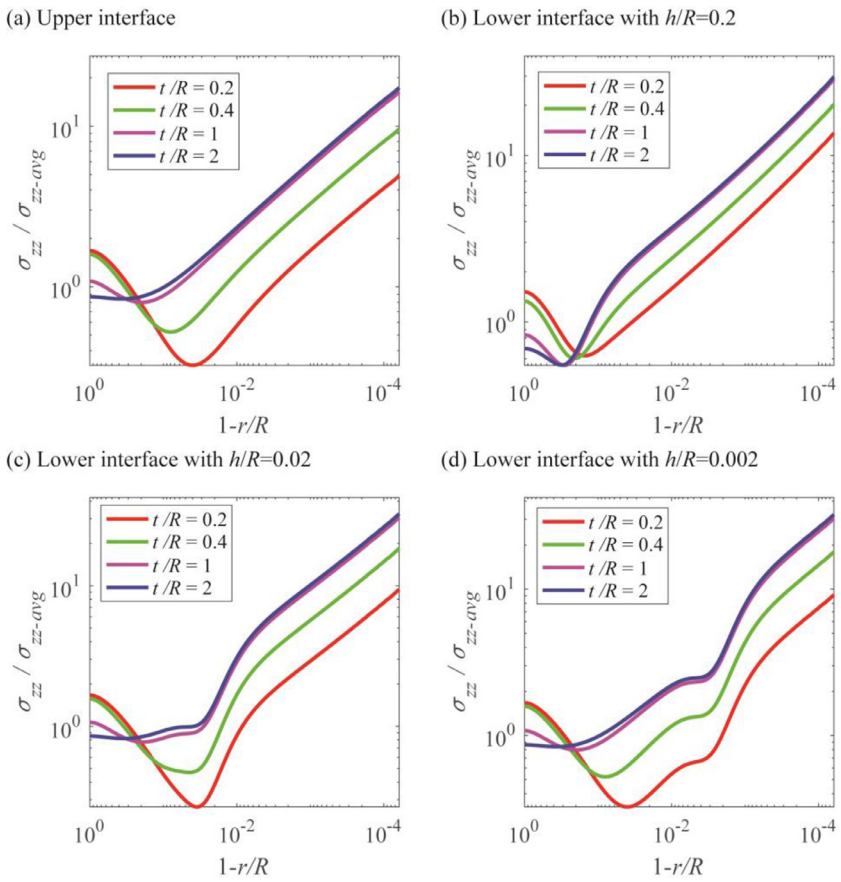

Fig. 2. Normalized normal stress distribution at upper and lower interfaces for stamps with varying thickness, t/R: (a) Upper interface (stamp-chip interface); these results are independent of the chip thickness, h/R. (b) Lower interface (chip-substrate interface) with $h/R = 0.2$. (c) Lower interface with $h/R = 0.02$. (d) Lower interface with $h/R = 0.002$.

The analysis was performed in the commercial FE software Abaqus Standard (Abaqus 2016, Providence, RI). Axisymmetric quadrilateral elements (CAX4RH) were used to mesh the model. In select cases (described in Section 4.5), plane strain simulations were also completed; for these cases plane strain quadrilateral elements (CPE4RH) were used to mesh the model. For all models, the mesh near both interfaces was refined and mesh convergence studies were performed with further refinement resulting in less than 3% difference in the stress and energy release rate. Approximately 2×10^6 to 5×10^6 elements were used over the range of different geometries considered here.

4. Results and discussion

The aim of this study is to establish under which conditions modifying the interfacial stress distribution at the upper interface (e.g. via stamp geometry or loading configuration) will provide the ability to enhance the retrieval or printing step of the microtransfer printing process. If the upper and lower interfaces are modified in the same manner by a change to the stamp geometry or applied loading, then the change does not lead to increased control of the process. We consider both perfectly bonded and different pre-cracked interfaces. The results are organized as follow: First, results for perfectly bonded interfaces are presented (Section 4.1). Second, cases in which a small edge crack is present at the lower interface are examined (Section 4.2). Third, results for cases in which a long edge crack is present at the lower interface (Section 4.3) are discussed. Then cases of failure initiated away from edges are investigated (Section 4.4 and Appendix B). Finally, a stamp design strategy, guided by the leading order of stress singularity at edge, is proposed and analyzed (Section 4.5).

4.1. Perfectly bonded interfaces

Normalized stress distributions at the upper and lower interfaces for various stamp thicknesses (t/R) and chip thicknesses (h/R) when both interfaces are perfectly bonded are shown in Fig. 2. The stress distribution is plotted on a logarithmic scale to highlight the edge singularity zone. The magnitude of the edge singularity (H) is determined by performing a linear fit to the logarithmic plot of the stress distribution, and the intercept is equal to log$H$ (Khaderi et al., 2015;

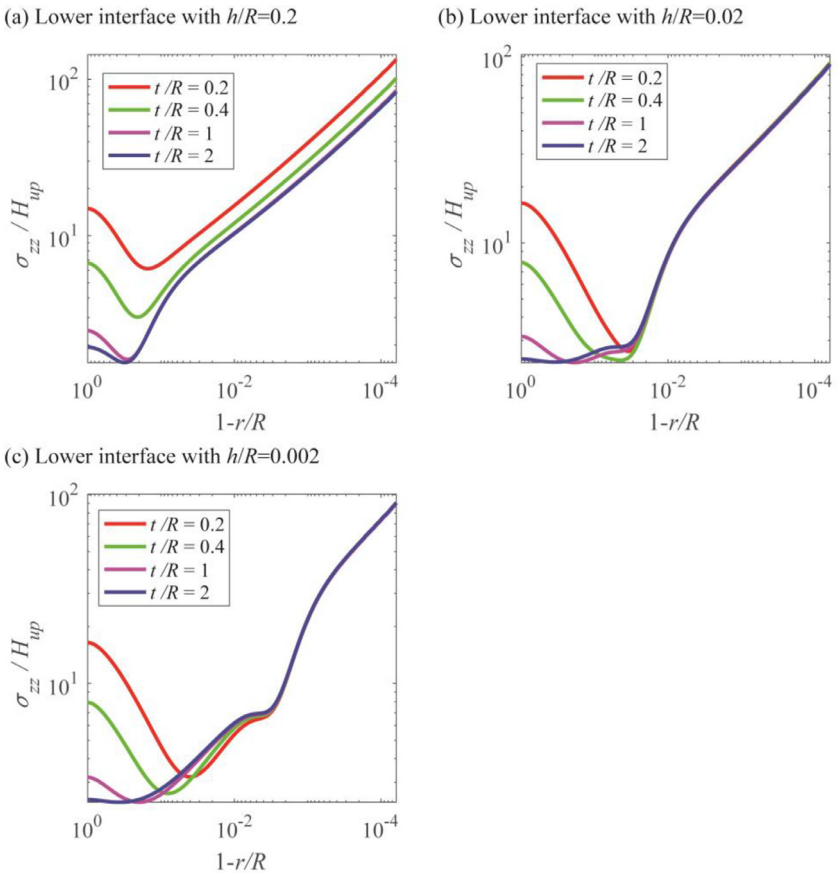

Fig. 3. Normal stress distribution at the lower interface normalized by the magnitude of the edge singularity at the upper interface (H_{up}) for different stamp (t/R) and chip thicknesses: (a) $h/R = 0.2$ (b) $h/R = 0.02$ (c) $h/R = 0.002$.

Balijepalli et al., 2017). The magnitude of the edge singularity can be used as a criterion for interfacial failure (Akisanya and Fleck, 1997; Khaderi et al., 2015; Balijepalli et al., 2016 and 2017).

The elastomer stamp is in contact with a much stiffer Si chip, thus the stress distribution at the upper interface and H_{up} is independent of the chip thickness (h/R) as shown in Fig. 2(a). The stress distribution at the lower interface depends on both stamp thickness (t/R) and chip thickness (h/R) and is shown in Fig. 2(b)-(d). The linear region in this logarithmic plot indicates the edge singularity zone and the size of this region defines the length of the edge singularity zone, d_{len}. From Fig. 2, it is evident that the d_{len} at both the upper and lower interfaces depends on the characteristic dimension of the structure. Specifically, the length of the edge singularity zone at the upper interface, $d_{len\text{-}up}$, decreases as the stamp thickness (t/R) decreases and the length of the edge singularity zone at the lower interface, $d_{len\text{-}low}$, decreases as the chip thickness (h/R) decreases. Moreover, as shown in Fig. 2(a), the magnitude of edge singularity at the upper interface (H_{up}) decreases with t/R, which indicates higher adhesion strength at the upper interface with decreasing t/R, consistent with results from similar systems (Bartlett and Crosby, 2014; Minsky and Turner, 2015 and H. 2017; R.G. Balijepalli et al., 2017). Concurrently, the magnitude of the edge singularity at the lower interface (H_{low}) for all of the chip thicknesses studied also reduces with t/R as shown in Fig. 2(b)-(d), thus the adhesion at the lower interface is also enhanced by decreasing stamp thickness. This result shows that both interfaces are enhanced as the thickness of stamp is reduced, thus changing the stamp geometry will change the overall adhesion force measured in a microtransfer printing process and it is often assumed that a stamp with a higher adhesion force will increase yield in the retrieval step. However, the results here show that a change in adhesion force does not necessarily guarantee a change in the relative adhesion strengths of the two interfaces and thus may not alter the performance of the microtransfer printing process.

To examine the relative change in adhesion strength between the upper and lower interfaces, the stress distribution at the lower interface is normalized by the magnitude of the edge singularity at the upper interface (H_{up}), as shown in Fig. 3. For a chip with thickness $h/R = 0.2$, the stress at the lower interface increases as t/R is decreased for $t/R<1$ (Fig. 3(a)), thus while both H_{up} and H_{low} decrease with decreasing t/R (Fig. 2), the ratio, H_{up}/H_{low} also decreases with decreasing t/R. As a result, reducing stamp thickness from $t/R = 1$ to $t/R \leq 0.4$ (see Fig. 3(a)) for $h/R = 0.2$ will enhance the ability to retrieve chips; this effect has been observed in previously reported results (Minsky and Turner, 2017). However, the results in Fig. 3(b)-(c)

show that when the chip thickness, h/R, is more than an order of magnitude smaller than the stamp thickness, t/R, (i.e., $h/R = 0.02$ or 0.002 with $t/R \geq 0.2$) that the lower interface stress near the edge is insensitive to t/R. For these cases, the length of the edge singularity zone at the lower interface is much smaller than that of the upper interface ($d_{len\text{-}low} << d_{len\text{-}up}$) and there is a region near the edge of the lower interface where the stress distribution is independent of t/R and thus H_{up}/H_{low} is constant as the stamp thickness is changed. This region is embedded in the edge singularity zone of the upper interface, and the stress in this zone scales linearly with H_{up}. We call this region at the lower interface where the stress is independent of t/R the *embedded stress zone* and the length of the embedded stress zone is approximately equal to the thickness of the chip (Fig. 3(b) and (c)). It is clear from Fig. 3 that, for a chip with a thickness (h/R) much smaller than the stamp height (t/R), modifying the stress distribution at the upper interface modifies the stress within the embedded stress zone at the lower interface in the same way and H_{up}/H_{low} is insensitive to changes in stamp thickness. In summary, from the results in Fig. 3 we find that for perfectly bonded interfaces that decreasing the stamp thickness will lead to enhanced retrieval and increasing the stamp thickness will lead to enhanced printing only when t/R is comparable to or smaller than h/R. In other words, stamp thickness is only a useful "knob" for controlling the microtransfer printing process when $t/h \leq$~1.

4.2. Short lower interface crack located within the embedded stress zone

In the preceding discussion, the interfaces were perfectly bonded. In this section, cases in which an edge crack is present are examined (Fig. 1(c)). For a thin stamp ($t/R<1$), the length of the edge singularity zone at the upper interface is about 10% of the stamp height ($d_{len\text{-}up}/t \approx 0.1$) (Fig. 2(a)) (R.G. Balijepalli et al., 2017); and for a thick stamp ($t/R>1$), the length of the edge singularity zone at the upper interface is about 10% of the stamp radius ($d_{len\text{-}up}/R \approx 0.1$) (Khaderi et al., 2015). As the soft stamp can conform to defects on the upper surface of the chip and the length of the edge singularity zone at the upper interface, $d_{len\text{-}up} \geq 0.02R$ in this work (corresponding to 10% of $t/R = 0.2$ case), the crack length at the upper interface is expected to be small enough and is assumed to be located in the edge singularity zone of the upper interface ($a_{up} < d_{len\text{-}up}$) (Kim-Lee et al., 2014; R.G. Balijepalli et al., 2017). We first investigate the case where the crack at the lower interface is small such that it is within the embedded stress zone (i.e. $a_{low} < h$). A small pre-crack at the lower interface is generally preferable unless intentionally designed otherwise, since it corresponds to higher fabrication precision, a smaller chance of interfacial failure, and lower thermal and electrical contact resistances in the final device. When the crack at the lower interface is located in the embedded stress zone, the stress distribution at the upper interface is not affected by the presence of a crack at the lower interface since the chip is $\approx 10^5$ times stiffer than the stamp.

4.2.1. Upper interface crack smaller than the chip thickness ($a_{up}/h<1$ with $a_{up}/t<0.1$)

When the upper interface crack is smaller than the chip thickness, the presence of a crack at the upper interface does not affect the stress distribution at the lower interface. When the upper interface crack is located in the edge singularity zone of the upper interface ($a_{up} < d_{len\text{-}up}$), the energy release rate at upper interface (G_{up}) can be obtained as a function of H_{up} and a_{up} from dimensional analysis (with units of H_{up} as given in Eq. (3)) as

$$G_{up} = \frac{C_{up}}{E^*_{up}} H^2_{up} a^{0.20}_{up} = \frac{3.7}{E^*_{up}} H^2_{up} a^{0.20}_{up} \tag{15}$$

where C_{up} is a constant that depends on the elastic mismatch and the wedge angle of the contact at the upper interface. C_{up} is found to be 3.7 from our FE calculations for the system considered here.

The energy release rate at the lower interface (G_{low}) can be expressed as a function of H_{low} and a_{low} for the case when the lower interface crack is located in the edge singularity zone of the lower interface ($a_{low} < d_{len\text{-}low} \approx 0.1$ h) using dimensional analysis with unit of H_{low} indicated by Eq. (4), giving

$$G_{low} = \frac{C_{low}}{E^*_{low}} H^2_{low} a^{0.08}_{low} = \frac{7.8}{E^*_{low}} H^2_{low} a^{0.08}_{low} \tag{16}$$

where C_{low} is a constant that depends on the elastic mismatch and the wedge angle of the contact at the lower interface. C_{low} is found to be 7.8 from FE calculations.

Fig. 4(a) and (b) show the normalized energy release rate when both the upper and lower interface cracks are located in their respective edge singularity zones and the upper interface crack is smaller than the chip thickness. Since $G \propto H^2$ for a given crack length, the trend is similar to the results shown in Fig. 2, both G_{up} and G_{low} reduce with decreasing the stamp thickness (t/R). Note that the mixed-mode conditions for the upper and lower interface cracks are independent of t/R and h/R since σ_{rz}/σ_{zz} are constant within the edge singularity zones as shown in Eqs. (3) and (4).

The normalized energy release rate ratio between the upper and lower interfaces (G_{up}/G_{low}), which determines the performance of the microtransfer printing processes, is shown in Fig. 4(c). For $h/R = 0.2$, G_{up}/G_{low} reduces by 60% when t/R decreases from 1 to 0.2 and is insensitive to t for $t/R>$~1. This indicates that in this regime, reducing the stamp thickness (t/R) facilitates retrieval and increasing the stamp thickness facilitates printing for a thick chip ($h/R \geq$~0.1). However, for thin chips ($h/R<$~0.1), it is also evident in Fig. 4(c) that changing the stamp thickness only provides control over the microtransfer printing process when h/R is comparable to or larger than t/R ($h/t>$~0.1), and G_{up}/G_{low} is independent of t/R when h/R is more than an order of magnitude smaller than t/R ($h/t \leq$~0.1). This is a similar result to that obtained in the previous section for defect-free interfaces. In the regime where G_{up}/G_{low} is insensitive to t/R (i.e. $h/t<0.1$ and $h/R<0.1$, the case of transferring

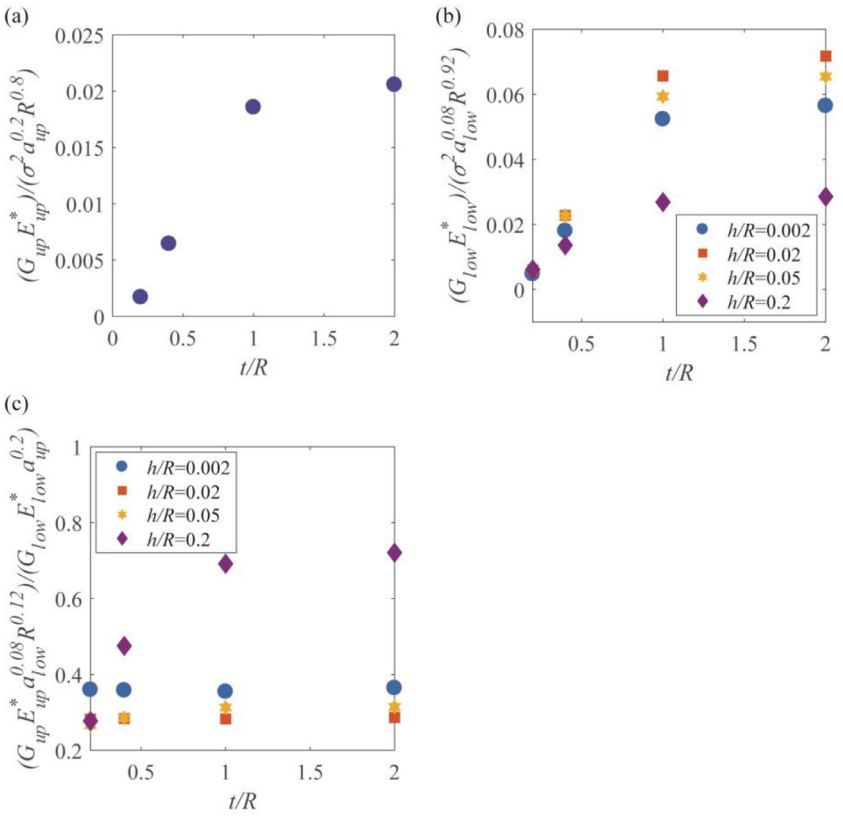

Fig. 4. Normalized energy release rates for the case of a short upper pre-crack ($a_{up}<d_{len\text{-}up}$ and $a_{up}<h$) and a lower pre-crack in the edge singularity zone ($a_{low}<d_{len\text{-}low}$). (a) Normalized energy release rate at the upper interface (G_{up}) (b) Normalized energy release rate at the lower interface (G_{low}) (c) Ratio of the energy release rate between the upper and lower interfaces (G_{up}/G_{low}).

thin chips), the analysis framework established here can be used to further understand the factors that affect retrieval and printing. When $h/t<0.1$, the edge singularity zone at the lower interface is embedded in the edge singularity zone at the upper interface, and from a dimensional analysis based on the units of H_{up} and H_{low} in Eqs. (3) and (4)

$$H_{low} = C_{em}H_{up}h^{0.06} = 1.5H_{up}h^{0.06} \tag{17}$$

where C_{em} is a constant that depends on the elastic mismatch and the wedge angle of the contact at the upper and lower interface and is found to be 1.5 from our FE calculations.

Substitution of Eq. (17) into Eq. (16) yields:

$$G_{low} = \frac{7.8}{E^*_{low}}\left(1.5H_{up}h^{0.06}\right)^2 a_{low}^{0.08} = \frac{17.6}{E^*_{low}}H_{up}^2 h^{0.12}a_{low}^{0.08} \tag{18}$$

Combining Eq. (15) and Eq. (18), G_{up}/G_{low} can be determined and we can write the ratio of energy release rates to the ratio of critical energy release rates as expressed in the retrieval and printing criteria given earlier Eqs. (13) and ((14)) as:

$$\frac{G_{up}/G_{up-c}}{G_{low}/G_{low-c}} = 0.2\frac{G_{low-c}}{G_{up-c}}\frac{E^*_{low}}{E^*_{up}}\frac{a_{up}^{0.20}}{h^{0.12}a_{low}^{0.08}} = 0.2\frac{G_{low-c}}{G_{up-c}}\frac{E^*_{low}}{E^*_{up}}\left(\frac{a_{up}}{h}\right)^{0.12}\left(\frac{a_{up}}{a_{low}}\right)^{0.08}. \tag{19}$$

As noted earlier, printing requires $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})>1$ and retrieval requires $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})<1$. Eq. (19) shows that $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$ only depends on the elastic mismatch (E^*_{up}/E^*_{low}), the ratio of critical energy release rates ($G_{up\text{-}c}/G_{low\text{-}c}$) and geometric factors (a_{up}/h and a_{up}/a_{low}). For given defect sizes, smaller h results in larger $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$, indicating that thinner chips are more difficult to retrieve. However, the exponents on a_{up}/h and a_{up}/a_{low} are small, so $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$ is only weakly dependent on these factors. Eq. (19) suggests that for micro-transfer printing of thin chips with small pre-cracks at the lower interface, the elastic modulus ratio and the critical energy release rate ratio are the primary parameters that can be tuned to control the process. More specifically, from a stamp design perspective, one can shift from printing to retrieval by increasing the critical strain energy release rate of the stamp-chip interface or increasing the modulus of the stamp in order to decrease $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$. This finding is consistent with the previous reports of transfer printing noted in the Introduction. Noted that if the length of the lower interface

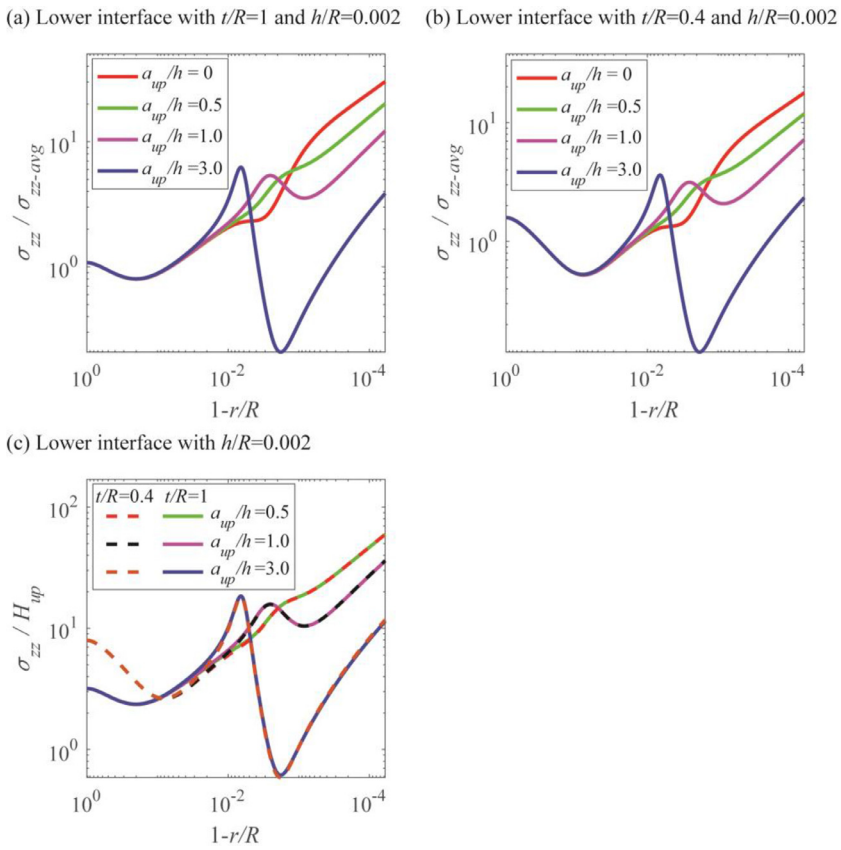

Fig. 5. (a) Normalized normal stress distribution at the lower interface with $t/R = 1$ and $h/R = 0.002$ for various a_{up}/h. (b) Normalized normal stress distribution at the lower interface with $t/R = 0.4$ and $h/R = 0.002$ for various a_{up}/h. (c) Normal stress distribution at the lower interface normalized by the magnitude of the edge singularity at the upper interface (H_{up}) with $t/R = 1$ and $t/R = 0.4$ for various a_{up}/h.

crack is larger than the lower interface edge singularity zone, but smaller than the embedded stress zone (i.e. $0.1h<a_{low}<h$), $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$ is still independent of t/R as discussed in Appendix A.

4.2.2. Upper crack comparable to or larger than the chip thickness ($a_{up}/h \geq 1$ with $a_{up}/t < 0.1$)

When the upper interface crack is comparable to or larger than the chip thickness, the presence of a crack at the upper interface affects the stress distribution at the lower interface. Fig. 5(a) and (b) show the normalized normal stress distribution at the lower interface with $h/R = 0.002$ for $t/R = 1$ and 0.4. As the upper interface crack length increases, the magnitude of the edge singularity at the lower interface (H_{low}) is reduced since it is shielded by the upper interface crack. However, if the normal stress on the lower interface is normalized by the magnitude of the singularity at the upper interface (H_{up}), as shown in Fig. 5(c), the embedded stress zone at the lower interface still exists and G_{up}/G_{low} is insensitive to stamp thickness, t/R.

In summary, regardless of whether the upper interface crack length is smaller or larger than the chip thickness, as long as the upper and lower interface cracks are embedded in the edge singularity zone of the upper interface, which is the case for a chip with a thickness that is at least an order of magnitude smaller than the stamp height ($h/t<0.1$) and a small pre-crack at lower interface, G_{up}/G_{low} is a constant and independent of the far field condition (e.g. stamp thickness and loading configuration) that modifies the global stress distribution. This indicates that to change G_{up}/G_{low} by the modification of stress distribution, the length of the edge singularity zone at the upper interface should be smaller than or comparable to the length of the edge singularity zone at the lower interface (i.e. $d_{len\text{-}up}/d_{len\text{-}low}<\sim1$). However, this requires that the stamp has a thickness comparable to the chip thickness. It is often not straightforward to fabricate an elastomer stamp with a thickness that is comparable to the chip thickness as microtransfer printing is used to transfer ultra-thin components.

4.3. Long lower interface crack that extends beyond the embedded stress zone

Fig. 3(b) and (c) shows that although the stress within the embedded stress zone at the lower interface scales linearly with H_{up}, the stress outside of this zone does not. As a result, when the crack length at the lower interface is longer than the length of the embedded stress zone, it is not dominated by the edge singularity zone at the upper interface and can

Table 2
$(G_{up}E_{up}{}^{*}a_{low})/(G_{low}E_{low}{}^{*}a_{up}{}^{0.2}R^{0.8})$ for various t/R and a_{low}/h with $h/R = 0.002$.

a_{low}/h			
t/R	100	50	20
1	1.8×10^{-10}	3.7×10^{-9}	2.1×10^{-7}
0.4	2.3×10^{-9}	6.9×10^{-9}	2.6×10^{-7}

be influenced by a global change in stress distribution resulting from a change in the stamp thickness. From dimensional analysis:

$$G_{low} = \frac{g}{E^{*}_{low}}\sigma^{2}a_{low} \tag{20}$$

where g depends on the elastic mismatch, the geometry of the stamp and chip, boundary conditions and the lower interface crack length. Assuming, the upper interface crack is located in the edge singularity zone of upper interface, Eq. (15) still holds. Table 2 shows the normalized G_{up}/G_{low} with $h/R = 0.002$ and a long lower interface crack. When t/R is changed from 1 to 0.4, G_{up}/G_{low} is changed for all lower interface crack lengths studied. This clearly indicates that modifying the interfacial stress distribution can modify G_{up}/G_{low} for a long lower interface crack even when h/R is small. However, the presence of a long crack at the lower interface not only increases the energy release rate for the lower interface crack but also reduces the energy release rate for the upper interface crack since it shields the stress on the upper interface crack. As a result, G_{up}/G_{low} is quite small and modifying the interfacial stress distribution likely would not be able to create a situation in which delamination is initiated at the upper interface to allow for printing of the chip.

4.4. Interface failure away from the edges

Note that all the discussions above are based on the assumption that the interfaces fail from the edges. However, as t/R decreases, the failure mechanism may change from a crack that initiates at the edge to a crack that initiates at the center (Minsky and Turner, 2015; Balijepalli et al., 2017). The case of a center crack is discussed in Appendix B and it is found that G_{up}/G_{low} is still insensitive to t/R for a sufficiently thin chip, thus this case does not provide more control in transfer printing processes than the edge failure cases discussed above.

4.5. Stamp design strategy guided by the leading order of stress singularity at edge (λ_1)

When the lower interface crack is located in the embedded stress zone, the preceding results have shown that the common method of tuning adhesion by tuning the interfacial stress distribution at the stamp-chip interface often does not change $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$. Thus, stress modification at the upper interface provides limited opportunity to control microtransfer printing processes. In a narrow regime (t/h<~1, Section 4.1) reducing the thickness of the stamp can enhance chip retrieval but fabrication and use of stamps with thicknesses comparable to the chip thickness is impractical in many situations as microtransfer printing is often used to transfer ultrathin (<100 nm) chips. To overcome this limitation, a stamp design strategy guided by the value of the leading order of stress singularity at the edge (λ_1) is proposed in this section to achieve control of $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$.

Typically, tunable adhesion is achieved primarily by effectively tuning the magnitude of the edge singularity (H) through the geometry or composition of the stamp (Balijepalli et al., 2016 and R.G. 2017; Minsky and Turner, 2015 and 2017). However, tuning H is often not effective in a microtransfer printing process where two interfaces are involved, as both G_{up} and G_{low} scale with $H_{up}{}^{2}$ and thus a change in H_{up} does not change G_{up}/G_{low}. In order to achieve tunability, it is necessary to have more than one independent parameter that can be changed by the far field condition. Consider Eq. (2), generally λ_1 is smaller than λ_2 and only H_1 associated with λ_1 is the dominant term. However, for a specific elastic mismatch and wedge contact angle, the roots of the characteristic equation that determine λ can be repeated roots. In this case, λ_1 equals λ_2 and both the magnitudes H_1 and H_2 are the leading order magnitudes of singularity. From the analysis of Khaderi et al. (2015), there is one geometry and material combination that yields repeated roots of λ at the upper interface. This specific case is α=−1 and β=0 and a wedge angle of the stamp-chip contact that is 180°; this geometry is shown in Fig. 6(a). This case is readily achieved in real applications as α=−1 and β=0 correspond to an incompressible stamp that is much softer than the chip like the typical elastomeric stamp (e.g., PDMS) commonly used in a microtransfer printing of high modulus semiconductor chips. The 180° wedge angle requires the lateral dimensions of the stamp be larger than the chip size as shown Fig. 6(b). This stamp geometry is not often used as it does not allow selective retrieval of components, but it is feasible and has been used in some reports of microtransfer printing (e.g. Meitl et al., 2006; Sen et al., 2018).

To demonstrate that the stamp design strategy discussed above can achieve controlled microtransfer printing, even for thin chips, the configuration shown in Fig. 6(b) is analyzed. Two approaches are investigated to control the microtransfer printing process: (1) Vary the height of the stamp (t), which is straightforward to implement and similar to the composite stamp design proposed by H. Minsky and Turner (2017); (2) Apply shear displacement on top of the stamp during normal

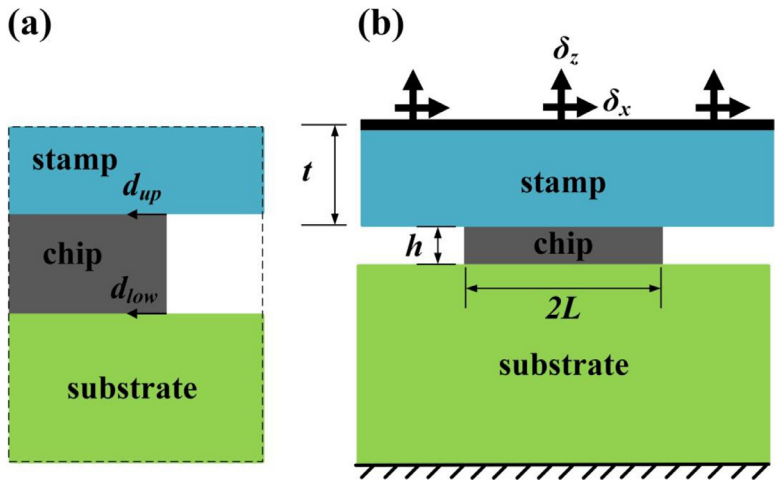

Fig. 6. Schematic of a microtransfer printing process with a stamp design guided by the leading order of stress singularity at the edge (a) Detail of edge geometry. (b) Overall geometry and loading configuration.

pull-off, which is akin to the shear assisted microtransfer printing method described by Carlson et al. (2011). It should be noted that while application of shear displacement has been demonstrated to significantly tune the adhesion of both rectangular and circular pillars (Carlson et al., 2011; Minsky and Turner, 2015, 2017), modeling delamination of a circular pillar loaded by a shear displacement requires a full 3D FE simulation. Since the stress field in the edge singularity zones of the upper and lower interfaces are identical for both axisymmetric and plane strain conditions (Khaderi et al., 2015; Balijepalli et al., 2017), the general understanding presented in this paper is applicable to both axisymmetric and plane strain problems. In this section the system shown in Fig. 6(b) is modeled as a plane strain case to allow for the application of shear. The model consists of a rectangular chip with half width $L = 50$ μm, thicknesses $h = 0.1$ μm, and a sufficiently wide stamp with various heights.

For the configuration shown in Fig. 6(a), the stress distribution within the edge singularity zone at the upper interface is (Khaderi et al., 2015):

$$\begin{aligned}\sigma_{zz} &= H_I d_{up}^{-0.50} \\ \sigma_{rz} &= H_{II} d_{up}^{-0.50}\end{aligned} \tag{21}$$

When an upper interface crack is located in the edge singularity zone of the upper interface, from a dimensional analysis based on the units of H_I and H_{II} indicated by Eq. (21), the energy release rate at the upper interface (G_{up}) can be expressed as:

$$G_{up} = \frac{C_m}{E^*_{up}}\left(H_I^2 + H_{II}^2\right) = \frac{3.1}{E^*_{up}}\left(H_I^2 + H_{II}^2\right) \tag{22}$$

where C_m is a constant and is found to be 3.1 from our FE calculations for the configuration shown in Fig. 6(b).

The edge singularity zone at the lower interface is the same as earlier in this paper and stress are given by Eq. (4). For the case of a sufficiently thin chip in which the embedded stress zone exists, a dimensional analysis based on the units of H_{low}, H_I and H_{II} indicated by Eqs. (4) and (21) gives:

$$H_{low} = (C_I H_I + C_{II} H_{II}) h^{-0.04} = (1.0 H_I + 1.3 H_{II}) h^{-0.04} \tag{23}$$

where C_I and C_{II} are constants that depend on the elastic mismatch and the wedge angle of the contact at the upper and lower interfaces. For a soft incompressible stamp and the geometry shown in Fig. 6(b), C_I and C_{II} are found to be 1.0 and 1.3 from FE calculations. Substitution into Eq. (10) yields:

$$G_{low} = \frac{7.8}{E^*_{low}} (1.0 H_I + 1.3 H_{II})^2 h^{-0.08} a_{low}^{0.08} \tag{24}$$

and thus $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$ can be expressed as

$$\frac{G_{up}/G_{up-c}}{G_{low}/G_{low-c}} = \frac{3.1}{7.8} \frac{G_{low-c}}{G_{up-c}} \frac{E^*_{low}}{E^*_{up}} \frac{H_I^2 + H_{II}^2}{(1.0 H_I + 1.3 H_{II})^2} \left(\frac{h}{a_{low}}\right)^{0.08} \tag{25}$$

Note that Eq. (25) is only physically meaningful when $1.0H_I + 1.3H_{II} > 0$ and $H_I > 0$, so that $\sigma_{zz} > 0$ near edge at both interfaces. When $\lambda_1 = \lambda_2$, the mode mixity of the upper interface crack is not constant and depends on H_1 and H_2, thus $G_{up\text{-}c}$ may not be constant as the critical strain energy release rate can depend on mode-mixity. Waters and Guduru (2010) used

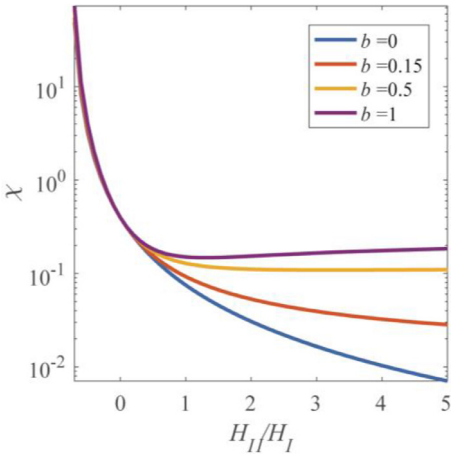

Fig. 7. Non-dimensional ratio of energy release rates (χ) for different b and H_{II}/H_I.

the empirical relation from Hutchinson and Suo (1991) to describe the dependence of critical energy release rate on mode-mixity between an incompressible elastomer and a rigid surface as

$$G_{up-c} = G_{up-Ic}\left[1 + 1.5\tan^2[(1-b)\phi]\right] \tag{26}$$

where $G_{up\text{-}Ic}$ is the mode I critical energy release rate and b is an experimentally determined constant between 0 and 1. ϕ is the phase angle with ϕ=$\tan^{-1}(K_{II}/K_I)$=$\tan^{-1}(H_{II}/H_I)$ here. A $b = 1$ indicates that the critical energy release rate is independent of the phase angle. Substitution into Eq. (25) yields:

$$\frac{G_{up}/G_{up-c}}{G_{low}/G_{low-c}} = \frac{3.1}{7.8}\frac{G_{low-c}}{G_{up-Ic}\left\{1+1.5\tan^2\left[(1-b)\tan^{-1}\left(\frac{H_{II}}{H_I}\right)\right]\right\}}\frac{E^*_{low}}{E^*_{up}}\frac{H_I^2+H_{II}^2}{(1.0H_I+1.3H_{II})^2}\left(\frac{h}{a_{low}}\right)^{0.08} \tag{27}$$

We define the normalized ratio of energy release rates as χ which contains all the terms associated with H_I and H_{II}, so that we can investigate the dependence of the ratio of energy release rates on H_{II} and H_I independent of the material properties and geometric factors (note that χ still depends b on the phase angle dependence given by Eq. (26)):

$$\chi = \frac{G_{up}\cdot\frac{G_{up-Ic}}{G_{up-c}}}{G_{low}}\cdot\frac{E^*_{up}}{E^*_{low}}\cdot\frac{{a_{low}}^{0.08}}{h^{0.08}} = \frac{3.1}{7.8}\frac{1.0+\left(\frac{H_{II}}{H_I}\right)^2}{\left\{1+1.5\tan^2\left[(1-b)\tan^{-1}\left(\frac{H_{II}}{H_I}\right)\right]\right\}\left(1.0+1.3\frac{H_{II}}{H_I}\right)^2}. \tag{28}$$

Larger $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$ or larger χ facilitates printing while smaller $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$ and smaller χ facilitates retrieval.

The value of χ for different b and H_{II}/H_I is shown in Fig. 7. Note that χ is a function of H_{II}/H_I and is independent of the absolute value of H_I and H_{II}. $\chi\to\infty$ when $H_{II}/H_I\to-0.77$, since the bottom interface edge will be in compression and thus will not fail if $H_{II}/H_I<-0.77$ according to Eq. (24). For $b = 1$ and 0.5 in Fig. 7, χ decreases as H_{II}/H_I increases and reaches minimum at H_{II}/H_I=1.3 for $b = 1$ and H_I/H_{II}=3.2 for $b = 0.5$. The minimum values of χ are 0.15 for $b = 1$ and 0.11 for $b = 0.5$. For $b = 0.15$ and 0, χ decreases monotonically as H_{II}/H_I increases. The minimum χ is 0.013 for $b = 0.15$ and 0 for $b = 0$ in the limit as $H_{II}/H_I\to\infty$.

The ratio of H_{II}/H_I and thus χ can be tuned through multiple approaches, including varying the stamp thickness (t) and applying shear displacement on top of the stamp during retraction as shown in Fig. 6(b). Note, the application of a shear displacement affects both the shear and normal stresses at the interface; shear displacement affects the normal stresses because a moment is applied on the interface by the shear force on the top of the stamp. Fig. 8 shows χ obtained from FE calculations as a function of stamp thickness (t/L) and the ratio of shear to normal displacement (δ_x/δ_z) for $b = 1$ and 0.15. Those two values of b are selected since $b = 1$ represents an extreme case where the critical energy release rate is independent of the phase angle, and $b = 0.15$ represents the experimental measured property of PDMS, a common material used for microtransfer printing stamps, in contact with glass (Waters and Guduru, 2010). The trend is similar for both $b = 1$ and 0.15. Increasing t/L leads to larger χ which is favorable for printing. In a normal pull-off process (i.e. only normal displacement is applied and δ_x/δ_z=0), increasing t/L from 0.2 to 1 increases χ by 8% for $b = 1$ and 24% for $b = 0.15$ suggesting that a thicker stamp is beneficial for printing. Meanwhile, increasing δ_x/δ_z also increases χ which indicates that application of shear displacement helps with printing. With $t/L = 0.2$, increasing δ_x/δ_z from 0 to 6 increases χ by 29% for $b = 1$ and 83% for $b = 0.15$. While for $t/L = 1$, increasing δ_x/δ_z from 0 to 6 increases χ by 630% for $b = 1$ and 820% for $b = 0.15$. Results in Fig. 8 suggest that use of a thin stamp in a normal pull-off process (i.e. δ_x/δ_z=0) is preferable for retrieval, while use of a thicker stamp with a shear displacement applied is preferable for printing. The analysis above clearly shows that χ and thus the microtransfer printing process can be effectively controlled by appropriate stamp design and loading condition using the stamp design strategy guided by the leading order of stress singularity at edge.

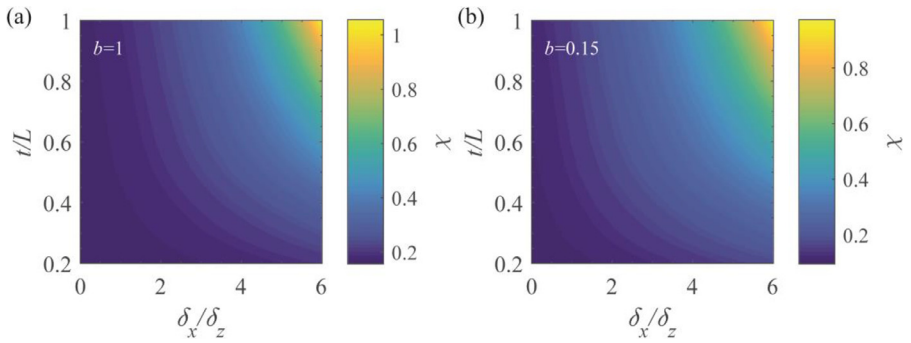

Fig. 8. Non-dimensional ratio of energy release rates (χ) as a function of t/L and δ_x/δ_z for (a) $b = 1$. (b) $b = 0.15$. A higher χ is favorable for printing while a lower χ is favorable for retrieving.

5. Conclusion

This work investigated the mechanics of a microtransfer printing process in which a thin stiff chip supported on a significantly thicker stiff substrate is transferred using a compliant stamp with various stamp heights. The stamp thickness affects the stress distribution at the interfaces and the apparent adhesion strength. The effect of modifying the interfacial stress distribution via stamp height on the delamination path between two interfaces in the microtransfer printing process is systematically studied. It was shown that both the stress distribution at the stamp/chip interface and the chip/substrate interface are modified by the change of the stamp thickness. Control of the delamination path in a microtransfer printing process can be achieved for situations where the chip thickness is larger or comparable to the stamp height and/or a long lower interface pre-crack is present. However, for a sufficiently thin chip with no or small pre-cracks, the adhesion strength at the stamp-chip interface and the chip-substrate interface are tuned to the same extent as the stress distribution at the stamp-chip interface is modified. In these cases, there is no relative adhesion change between the stamp-chip interface and the chip/substrate interface, and modifying the interfacial stress distribution at the stamp interface does not provide control of the microtransfer printing process.

To overcome the limitations noted above, a stamp design strategy guided by the leading order of stress singularity order at the edge is proposed. We show that by using an incompressible, soft stamp with a lateral dimension larger than the chip that the crack path selection in the microtransfer printing process can be engineered to be sensitive to the thickness and degree of normal and shear loading applied to the stamp. The results show that the use of a thin stamp and normal loading during retraction of the stamp is favorable for retrieval, while use of a thicker stamp and an applied shear displacement is favorable for printing.

Author statement

Mechanics of crack path selection in micortransfer printing: Challenges and opportunities for process control Aoyi Luo and Kevin T. Turner* Department of Mechanical Engineering and Applied Mechanics, University of Pennsylvania, Philadelphia, PA 19,104–6315, USA

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Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A

Lower interface crack located within the embedded stress zone and larger than the lower interface edge singularity zone ($0.1h<a_{low}<h$)

If the lower interface crack is larger than the lower interface edge singularity zone, but smaller than the embedded stress zone, the stress distribution within this region still linearly scales with H_{up} and G_{low} is also a function of H_{up}, a_{low} and h as:

Table A1
$f(a_{low}/h)$ for various a_{low}/h.

a_{low}/h	0.1	0.3	0.5
f	159.8	79.0	67.4

$$G_{low} = \frac{f\left(a_{low}/h\right)}{E^*_{low}} H^2_{up} h^{-0.8} a_{low} \tag{A1}$$

where f is a function of a_{low}/h. Table. A1 summarizes the values of $f(a/h)$ for different a_{low}/h. As a result, $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$ is still independent of the stress distribution.

Appendix B

Interface failure via a center crack

When the stress distribution at the upper interface is modified through a decrease of t/R, the failure mechanism may change from a crack that initiates at the edge to a crack that initiates at the center (Minsky and Turner, 2015; Balijepalli et al., 2017). Since the contact of a soft stamp with a stiff material in the center region is generally conformal, the upper interface center crack is assumed to be small compared to the chip thickness and other dimensions. From dimensional analysis, the energy release rate of a center crack at the upper interface (G_{up}) is:

$$G_{up} = \frac{C_{cen-up}}{E^*_{st}} \sigma^2_{zz-up}(r=0) a_{up} = \frac{0.7}{E^*_{st}} \sigma^2_{zz-up}(r=0) a_{up} \tag{B1}$$

where $C_{cen\text{-}up}$ is a constant and is found to be 0.7 from our FE calculations. Eq. (B1) is the same as that for a penny-shaped crack at the interface between an elastic half space and a rigid substrate, subjected to normal loading (Anderson, 2005).

If the lower interface center crack is small compared to the chip thickness ($a_{low}/h << 1$):

$$G_{low} = \frac{C_{cen-low}}{E^*_c} \sigma^2_{zz-low}(r=0) a_{low} = \frac{1.3}{E^*_c} \sigma^2_{zz-low}(r=0) a_{low} \tag{B2}$$

where $C_{cen\text{-}low}$ is a constant and is found to be 1.3 from our FE calculations which is the same as a penny-shaped crack in an infinite body subjected to normal loading (Anderson, 2005).

If the lower interface center crack is comparable to or larger than the chip thickness ($a_{low}/h \geq \sim 1$), the elasticity of both the chip and stamp affect the strain energy release rate of the lower interface

$$G_{low} = C\left(\frac{a_{low}}{h}, \frac{E^*_c}{E^*_{st}}\right) \sigma^2_{zz-low}(r=0) a_{low} \tag{B3}$$

where the constant C depends on a_{low}/h and E_c^*/E_{st}^*. For the given elastic mismatch of the stamp and the chip (E_c^*/E_{st}^*) studied here, Table. B1 lists C for different a_{low}/h.

From the discussion above, it is clear that the criterion $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$ depends on the elastic mismatch (E_c^*/E_{st}^*), the ratio of critical energy release rates ($G_{up\text{-}c}/G_{low\text{-}c}$), the geometric factor (a_{up}/a_{low}) and the ratio of stresses at the center of the upper and lower interfaces ($\sigma_{zz\text{-}up}(r=0)/\sigma_{zz\text{-}low}(r=0)$). $G_{up\text{-}c}/G_{low\text{-}c}$ is a constant because both critical energy release rates correspond to mode I fracture. If h/R is not sufficiently small, $\sigma_{zz\text{-}up}(r=0)/\sigma_{zz\text{-}low}(r=0)$ varies with t/R and thus $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$ also varies. For example, Table. B2 listed the value of $\sigma_{zz\text{-}up}(r=0)/\sigma_{zz\text{-}low}(r=0)$ for $h/R = 0.2$ with various t/R.

If h/R is sufficiently small, $\sigma_{zz\text{-}up}(r=0) = \sigma_{zz\text{-}low}(r=0)$, thus:

$$\frac{G_{up}/G_{up-c}}{G_{low}/G_{low-c}} = 0.5 \frac{G_{low-c}}{G_{up-c}} \frac{E^*_c}{E^*_{st}} \frac{a_{up}}{a_{low}} \tag{B4}$$

Table B1
C for various a_{low}/h.

a_{low}/h	0.5	1	2
C	1.49	1.99	4.14

Table B2
$\sigma_{zz\text{-}up}/\sigma_{zz\text{-}low}$ for various $h/R = 0.2$ with various t/R.

t/R	0.1	0.4	1	2
$\sigma_{zz\text{-}up}/\sigma_{zz\text{-}low}$	1.11	1.19	1.29	1.25

Again $(G_{up}/G_{up\text{-}c})/(G_{low}/G_{low\text{-}c})$ does not depend on the interfacial stress distribution and we cannot control microtransfer printing by changing t/R when it is a center crack for h/R sufficiently small.

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