

Ultraflat Sub-10 Nanometer Gap Electrodes for Two-Dimensional Optoelectronic Devices

Seon Namgung, Steven J. Koester,* and Sang-Hyun Oh*



Cite This: *ACS Nano* 2021, 15, 5276–5283



Read Online

ACCESS |



Metrics & More



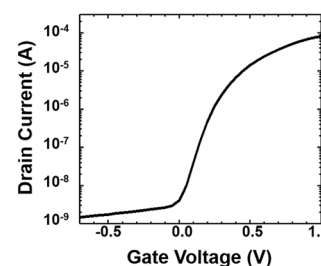
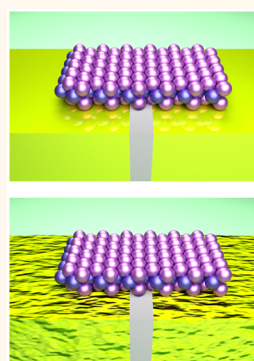
Article Recommendations



Supporting Information

ABSTRACT: Two-dimensional (2D) materials are promising candidates for building ultrashort-channel devices because their thickness can be reduced down to a single atomic layer. Here, we demonstrate an ultraflat nanogap platform based on atomic layer deposition (ALD) and utilize the structure to fabricate 2D material-based optical and electronic devices. In our method, ultraflat metal surfaces, template-stripped from a Si wafer mold, are separated by an Al_2O_3 ALD layer down to a gap width of 10 nm. Surfaces of both electrodes are vertically aligned without a height difference, and each electrode is ultraflat with a measured root-mean-square roughness as low as 0.315 nm, smaller than the thickness of monolayer graphene. Simply by placing 2D material flakes on top of the platform, short-channel field-effect transistors based on black phosphorus and MoS_2 are fabricated, exhibiting their typical transistor characteristics. Furthermore, we use the same platform to demonstrate photodetectors with a nanoscale photosensitive channel, exhibiting higher photosensitivity compared to microscale gap channels. Our wafer-scale atomic layer lithography method can benefit a diverse range of 2D optical and electronic applications.

KEYWORDS: two-dimensional materials, field-effect transistor, atomic layer lithography, atomic layer deposition, photodetector, template stripping



Transfer Characteristics of MoS_2 on Nanoscale Gap

In modern electronics, there has always been a high demand to integrate more electronic components on a chip, a need which has fueled the scaling of devices with critical dimensions down to a few nanometers.^{1–3} To maintain the electrostatic control as the channel length is scaled down, a thinner channel structure must be used to reduce short-channel effects.^{4–8} Thus, two-dimensional (2D) materials, which can be thinned down to single atomic layer, have been considered promising for gaining short-channel immunity and have been employed to demonstrate high on–off current ratios, low power consumption, and fast operation.^{9–15}

To fabricate nanoscale short-channel devices based on 2D materials, several fabrication strategies have been applied. For example, nanoscale channel length was achieved by angled metal deposition and using a nanowire mask.^{16–19} However, those methods cannot be used to fabricate multiple devices or to orient devices in different directions from the direction of angled deposition. Other approaches have been proposed to provide a precreated nanogap platform, which works as a source–drain electrode pair, onto which 2D materials are transferred as a channel material.^{20,21} Based on these methods, short-channel devices based on 2D materials have

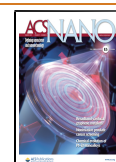
been reported, where the large bandgap of MoS_2 allowed a high on–off ratio ($\sim 10^6$) even with the short channel length. However, these methods rely on etching or cleavage of the crystalline structure along the crystal axis or grain boundaries, which limits the direction of device formation along these predefined boundaries. In addition, the roughness of as-deposited metal electrodes beneath the 2D materials can have a detrimental effect on the intimate contact between the 2D material and base electrodes. Alternatively, vertical transistors based on 2D materials have been explored to controllably define channel lengths to ~ 10 nm,^{22,23} but the integration of 2D materials on the vertical sidewalls remains a challenge.

Here, we develop a scalable method to build an ultraflat nanogap platform, which can be used for short-channel 2D material devices without directional restriction on device formation. In this approach, we construct two metal layers

Received: December 23, 2020

Accepted: February 19, 2021

Published: February 24, 2021



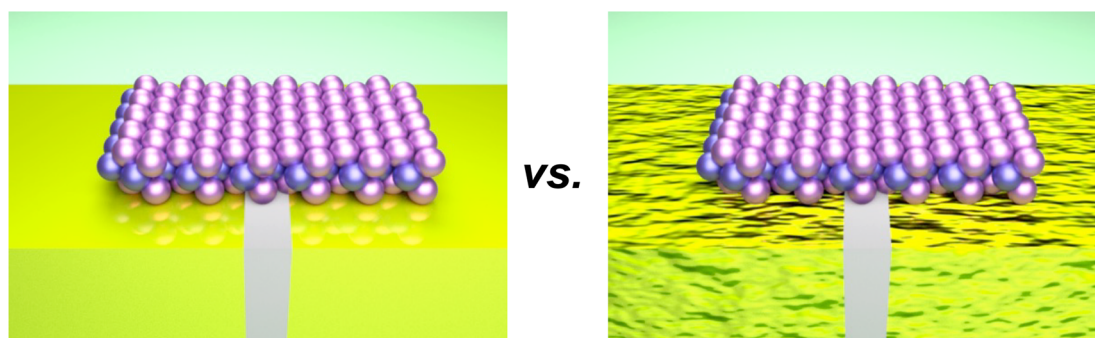


Figure 1. Schematic images showing a short-channel device built by transferring 2D materials on top of ultraflat template-stripped (left) and rough as-deposited (right) metal structures with nanoscale gap.

separated by a nanoscale gap as short as 10 nm, defined precisely by a sandwiched Al_2O_3 film deposited by an atomic layer deposition (ALD) process.^{24,25} The two metal layers with the nanogap separation are formed by a template-stripping method,^{26–30} resulting in metal layers with a root-mean-squared (RMS) roughness as low as 0.315 nm. This ultraflat interface should be favorable for intimate contact with 2D materials and minimize carrier scattering from the rough surface. In this work, we demonstrate that the ultraflat platform can be used to build 2D material based short-channel field-effect transistors (FETs) and photodetectors. This simple approach, wherein 2D materials can be placed on top of predesigned ultraflat nanogaps, allows large-scale fabrication of 2D material-based short-channel devices.

RESULTS AND DISCUSSION

Device Fabrication Process. The schematic diagram in Figure 1 shows devices built by transferring 2D materials on top of a precreated metal base pair separated by a nanogap. In these device structures, the pair of metal bases work as electrodes connecting the transferred 2D material flake, while the nanogap between two electrodes functions as a channel for carrier transport. Since the electrical and optical properties of 2D materials are significantly affected by the roughness of the substrate, the ultraflat template-stripped Au used in our work (left) should be advantageous compared to the rougher as-deposited Au platform (right) for carrier transport in 2D materials with less contact resistance.

Our nanogap platform has ultraflat metal surfaces on both sides that are template-stripped off of a Si wafer. In the lateral direction, a gap size as small as 10 nm is precisely defined by an ALD Al_2O_3 layer between the two flat metal surfaces. Figure 2a shows the fabrication process of our ultraflat nanogap platform. The process starts with deposition of an Al_2O_3 layer on a Si wafer using ALD (step 1). The flatness of a Si wafer (typically RMS roughness of ~ 0.3 nm)²⁶ and atomically controlled layer-by-layer formation of Al_2O_3 from the ALD method result in the ultraflat metal surface that will eventually serve as the ultraflat electrodes in the final template-stripped structure. It should be noted that the thickness of the Al_2O_3 layer in step 1 corresponds to the length of a nanogap in the final structure. The first metal layer is created by photolithography on top of the Al_2O_3 -deposited wafer (step 2). Since the whole structure built on the Si wafer needs to be stripped off of the wafer, the metals used in these methods are limited to metals with low adhesion to the Al_2O_3 layer, such as Au, Ag, and Pd.

Next, the exposed region of the Al_2O_3 layer is etched with phosphoric acid (step 3). Here, the first metal layer acts as an etch mask to protect Al_2O_3 beneath the metal layer. Since Si is much more resistant than Al_2O_3 against the phosphoric acid etchant, only Al_2O_3 is etched out, leaving the base Si unaffected. After the wet etching, the same thickness of Al_2O_3 layer is deposited by ALD again (step 4), using the same protocol as in step 1. This step is crucial to achieve the ultraflatness across the gap without a height difference between electrodes in the final structure. To secure a seamless structure between two metal layers, the second metal is deposited with a few μm of overlap with the first metal, which in our demonstration is limited by the photolithography resolution (step 5). With the overlap, the distance between the first metal and second metal is solely defined by the thickness of the Al_2O_3 ALD layer, which corresponds to the channel length in the final structure.

Sub-10 nm metal nanogap structures have been used to study fundamental physics in quantum regime such as boosted light–matter interaction and quantized electron tunneling.^{31–34} Top-down approaches such as e-beam lithography are challenging to use for fabricating sub-10 nm nanogap structures over large areas. Diverse alternative approaches have been proposed, such as self-assembled monolayers, the insertion of 2D materials,³⁵ and precisely controlled metal deposition or electromigration. Compared to those methods, atomic layer lithography, taking advantage of the ALD technique for forming solid dielectric films with atomic precision, allows the fabrication of sub-10 nm gaps uniformly over large regions in a controllable and reproducible manner. Many promising optical applications based on the highly enhanced electric field inside nanogaps have been successfully demonstrated using atomic layer lithography, such as extraordinary optical transmission, strong light absorption, and ultrasensitive molecular detection.^{36–38} In our work, in addition to the versatile optical applications, atomic layer lithography is utilized to provide a short-channel device platform for 2D materials.

To peel off the whole structure, an optical adhesive (NOA61, Norland Inc.) is applied on the structures on the Si wafer and covered with a glass slide as a mechanical support (step 6). After curing the glue, the whole structure, except the Al_2O_3 layer on the Si wafer, is stripped off from the wafer mechanically (step 7). This separation is possible because the adhesion between the metal layers and the Al_2O_3 layer on the wafer is weak compared to other interfaces, that is, the adhesion between Al_2O_3 /Si, metal/epoxy, Al_2O_3 /epoxy, and epoxy/glass. The stripped structure is turned over (step 8),

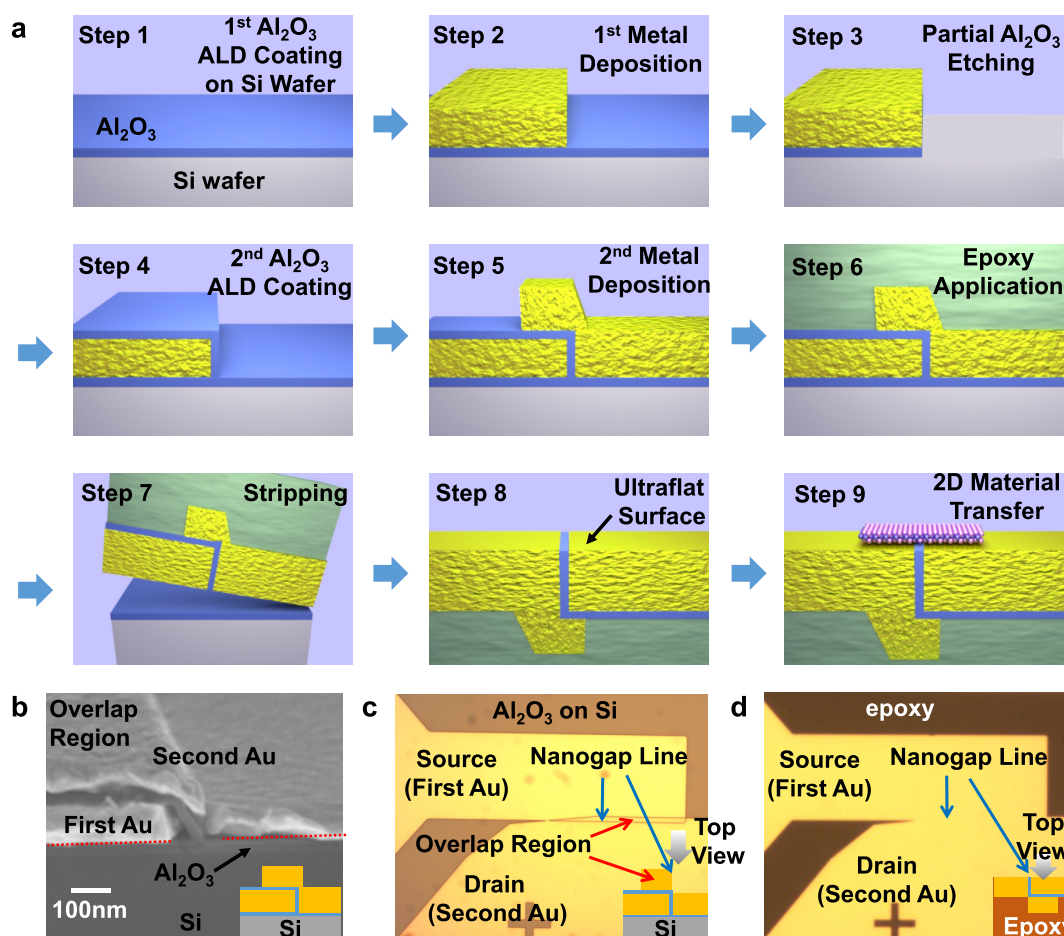


Figure 2. Fabrication of an ultraflat nanogap platform. (a) Schematic diagram showing the fabrication process of an ultraflat nanogap platform (see text for details). (b) SEM image showing a structure after the second metal deposition. Inset image indicates the corresponding process (step 5). There is no height difference in the base lines below the first metal and the second metal (indicated by red dotted lines). (c) Optical micrograph of a whole device structure before template stripping (step 5). The overlapped area between the first Au and the second Au can be seen *before* template stripping (marked by red arrows). The nanogap line is also seen due to the scattering from the height difference at the line (marked by blue arrows). (d) Optical micrograph of the device shown in (c) *after* template stripping (step 9). Since the structure is turned over, the overlapped region cannot be seen. The nanogap line cannot be seen due to the ultraflatness and nanoscale dimension (*i.e.*, no light scattering).

and as a final step, a flake of 2D material is transferred on top of the ultraflat metal surface, which was initially facing the Si/Al₂O₃ mold (step 9). Since the Al₂O₃ layer is left on the wafer in step 7, the ultraflat bare metal surfaces are exposed and can be contacted with the 2D material directly. In addition, since this method does not rely upon a crystal axis of a crystalline base, we can fabricate nanogap structures in any arbitrary direction.

Template-Stripped Ultraflat Nanogap Electrodes.

Figure 2b shows a scanning electron microscopy (SEM) image of a cross-sectional view corresponding to step 5. It should be noted that the height of the bottom lines of the two Au electrodes is the same across the Al₂O₃ barrier, marked by red dotted lines in Figure 2b. The same height of the bottom lines was achieved by using the same condition and number of cycles in the ALD deposition to build the Al₂O₃ layer beneath the first Au layer (in step 1) and the Al₂O₃ layer beneath the second Au layer (in step 4). By depositing the second metal with an overlapped region on top of the first metal, the distance between the first Au layer and the second Au layer is solely determined by the Al₂O₃ layer formed between the two metal layers. The distance of

the separation determines the channel length of the final device.

Figure 2c shows a top-view image of the structure before template stripping, corresponding to step 5. The nanogap is formed along the boundary between the two Au layers (marked by blue arrows). The overlapped region between two Au layers is also clearly seen from the top-view image (marked by red arrows). On the other hand, after being stripped off and turned over, the overlapped region is not seen from the top-view image in Figure 2d corresponding to step 9, since the overlapped region is underneath the first Au layer. It should also be noted that the nanogap line cannot be seen after being stripped off, which was clearly seen before being stripped off due to light scattering at the boundary (Figure 2c). The absence of light scattering at the boundary after being stripped off indicates no height difference exists between the two Au layers in the final structure (Figure 2d).

Metrology. To characterize our nanogap platform, we used SEM and atomic force microscopy (AFM). Figure 3a shows SEM images of nanogap structures of widths from 10 to 30 nm. The thickness of the gap size is determined by the thickness of the Al₂O₃ layer between the two electrodes

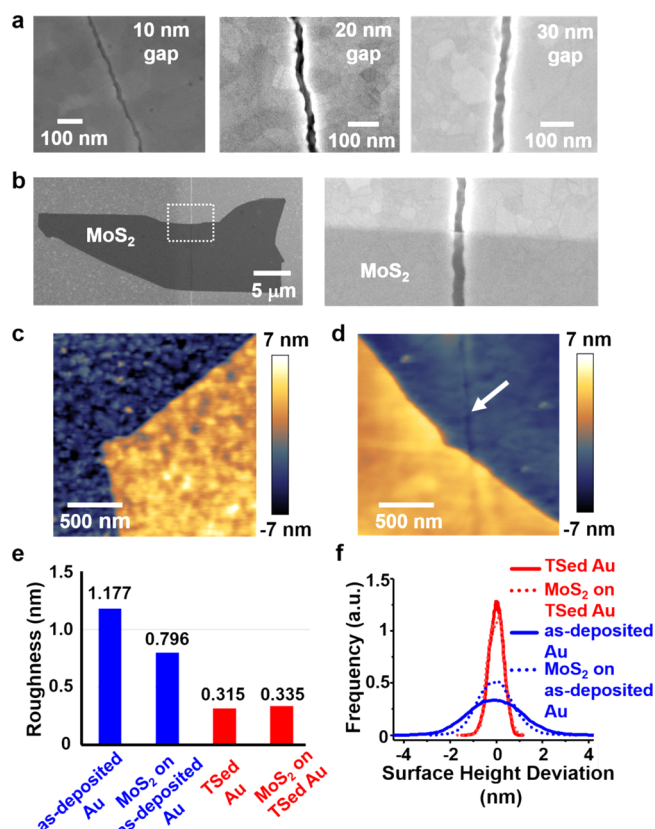


Figure 3. Characterization of ultraflat nanogap platform. (a) SEM images of nanogaps with different size. (b) SEM image of an MoS₂ flake transferred on an ultraflat nanogap platform. The region in the dotted lines is magnified and shown in the right image. (c) AFM image of an MoS₂ flake transferred on an as-deposited Au surface. (d) AFM image of an MoS₂ flake transferred on a template stripped (TSed) Au surface with a nanogap. (e) RMS roughness of Au bases and MoS₂ on the Au bases. (f) Histogram of the surface height deviation of Au bases and MoS₂ on the Au bases. Note the reduction on the roughness of MoS₂ on an as-deposited Au base compared to that of an original as-deposited Au base in (e) and the change on the distribution of surface height deviation of MoS₂ on an as-deposited Au base compared to that of an original as-deposited Au base in (f). These results indicate the suspension of MoS₂ over the as-deposited Au base, resulting from poor contact between them.

(Figure 2b). These nanoscale gaps are constructed over a large area owing to the uniformity of the ALD layer. Thus, our method can be practically utilized as a general process in massive manufacturing of nanoscale gap structures over a large area without restriction of gap formation along a certain angle. To build nanogap-based devices, we simply transferred 2D material flakes on top of our platform. Figure 3b shows an SEM image after a flake of MoS₂ was transferred onto a nanogap. The nanogap structure is clearly seen underneath the flake (right image) and acts as a channel in a final device.

We also conducted AFM analysis on the 2D materials on the base Au platform to confirm the intimate contact between 2D materials and ultraflat nanogap structures. Figure 3c,d shows AFM images of an MoS₂ flake transferred onto an as-deposited Au metal surface and an MoS₂ flake transferred onto a template-stripped nanogap structure, respectively. The white arrow in Figure 3d indicates a nanogap on the

template-stripped surface. The sandwiched Al₂O₃ layer between electrodes is not observed in the AFM image, because the surface of the Al₂O₃ layer is well below the electrodes. In a few cases, the Al₂O₃ layer was observable, but still lower than the electrodes (Supplementary Figure S1). Thus, in general, our results show that the ultraflat platform can be used for device fabrication without being disturbed by the Al₂O₃ layer. The dark-blue regions (lower regions) in both images indicate base Au regions, and the dark-yellow regions (higher regions) indicate MoS₂ regions on top of each Au surface. The stronger color contrast in Figure 3c compared to Figure 3d indicates the larger surface roughness of the as-deposited Au surface and MoS₂ on the as-deposited Au surface. We conducted statistical analysis on each surface to confirm if the MoS₂ flakes make intimate contact with the base Au surface. The RMS roughness of the template-stripped side of the first Au layer is 0.315 nm, while that of the MoS₂ surface on the template-stripped Au is 0.335 nm (red bars in Figure 3e). We note the surface of the template-stripped side of the second Au layer is also ultraflat and has a RMS roughness of 0.350 nm. The histogram profiles of surface height deviation of both surfaces are in good agreement (red solid and dotted line in Figure 3f). The good consistency of RMS roughness and the surface height deviation profile between both surfaces indicates MoS₂ makes intimate contact on the ultraflat template-stripped Au surface. On the other hand, the RMS roughness of the as-deposited Au surface is 1.177 nm, while that of the MoS₂ surface on the as-deposited Au is 0.796 nm (blue bars in Figure 3e). The histogram profiles of surface height deviation of MoS₂ surface on as-deposited Au surface (blue dotted line in Figure 3f) is more centered with lower deviation values compared to that of the as-deposited base Au surface (blue solid line in Figure 3f). The reduction of the RMS roughness and more centered deviation profile of MoS₂ surface on as-deposited surface indicates that the MoS₂ is suspended over the rough as-deposited surface, disrupting intimate contact between them. These results provide strong evidence that a more intimate contact can be established between 2D materials and metal contacts using our fabrication platform compared to conventional techniques.

Characterization of Short-Channel Field-Effect Transistors. After transferring 2D material flakes on top of our ultraflat nanogap platform, we explored the electrical characteristics of 2D material-based devices. The schematic diagram in Figure 4a shows the device structure of a nanoscale FET based on our ultraflat electrode platform. The two metal layers separated by a nanogap function as source-drain electrodes and MoS₂ and black phosphorus (BP) as channel materials.^{39–44} For the devices with BP channels, we deposited 10 nm of ALD Al₂O₃ on top of the BP after transferring the BP onto the nanogap structures, to protect BP from degradation in ambient conditions. In our nanoscale FET structure, ionic liquid is applied on top of a transferred 2D material flake, operating as a gate electrode. Before the 2D material transfer, the leakage current between the two electrodes was measured and found to be negligible, which confirms the nanogap insulates the two electrodes electrically (Supplementary Figure S2). The electrical isolation between two metal structures without 2D materials allows our platform to be used to build FETs by transferring 2D materials on top of the structure. Figure 4b,c shows the transfer characteristics and subthreshold swing (SS) vs drain

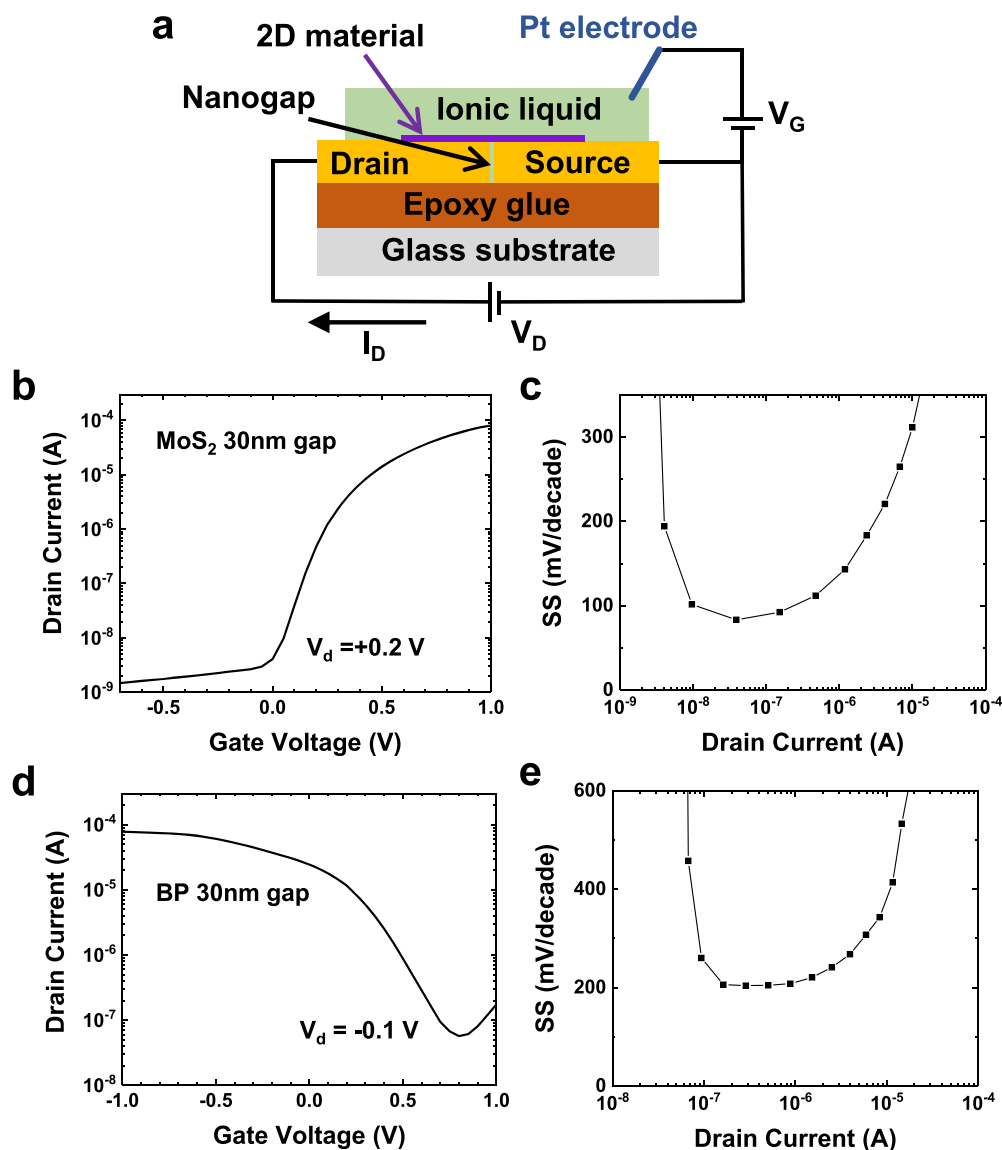


Figure 4. Electrical properties of short-channel 2D material FETs based on an ultraflat nanogap platform. (a) Schematic diagram showing an FET structure based on an ultraflat nanogap platform. The two metal regions separated by a nanogap work as source–drain electrodes. Ion liquid is applied on top of the 2D materials, working as a gate electrode. (b, c) Transfer characteristics and SS vs drain current of an MoS₂ FET with a 30 nm channel length, respectively. (d, e) Transfer characteristics and SS vs drain current of a BP FET with a 30 nm channel length, respectively.

current plot for an MoS₂ FET on a 30 nm nanogap platform, respectively. The transfer characteristics clearly show n-type behavior with a high on–off ratio of $\sim 10^4$. The SS value is measured as low as 83 mV/decade. Figure 4d,e shows the transfer characteristics and the SS vs drain current plot of a BP device on a 30 nm nanogap platform, respectively. In this device, the transfer characteristics clearly show p-type behavior with an on–off ratio of $\sim 10^3$. The measured SS is as low as 204 mV/decade. We also observed the operation of a BP device using nanogap spacings down to 10 nm (Supplementary Figure S3). These device characteristics with BP and MoS₂ flakes on nanogap structures show that our platform can be utilized to build 2D material-based short-channel FETs.

We further studied ambipolar behavior of a BP FET with a 15 nm nanogap structure (Figure 5). With negative drain voltage, p-type characteristics from hole conductivity were observed (Figure 5a,b), while n-type characteristics from

electron conductivity were observed with positive drain voltage (Figure 5c,d). In the output characteristics (Figures 5b,d), current saturation is observed in both cases. This ambipolar behavior from a single device is useful for practical applications such as building logic gates.

Photodetector Based on Black Phosphorus on a Nanogap Channel. In addition to the FET devices, we used our platform to fabricate and demonstrate photodetectors with a nanoscale photosensitive channel. Photodetectors based on 2D materials have been demonstrated to exhibit high sensitivity, broadband operation, and high-speed response.^{45,46} In highly integrated chips, photodetectors with a nanoscale photosensitive area are important for on-chip photonic integrated circuits. Here, to compare the performance of photodetection in nanoscale and microscale channels, we created an ultraflat platform with a gap increasing from 15 nm to a few μm . Then, we transferred a BP flake on top of our platform. We conducted scanning

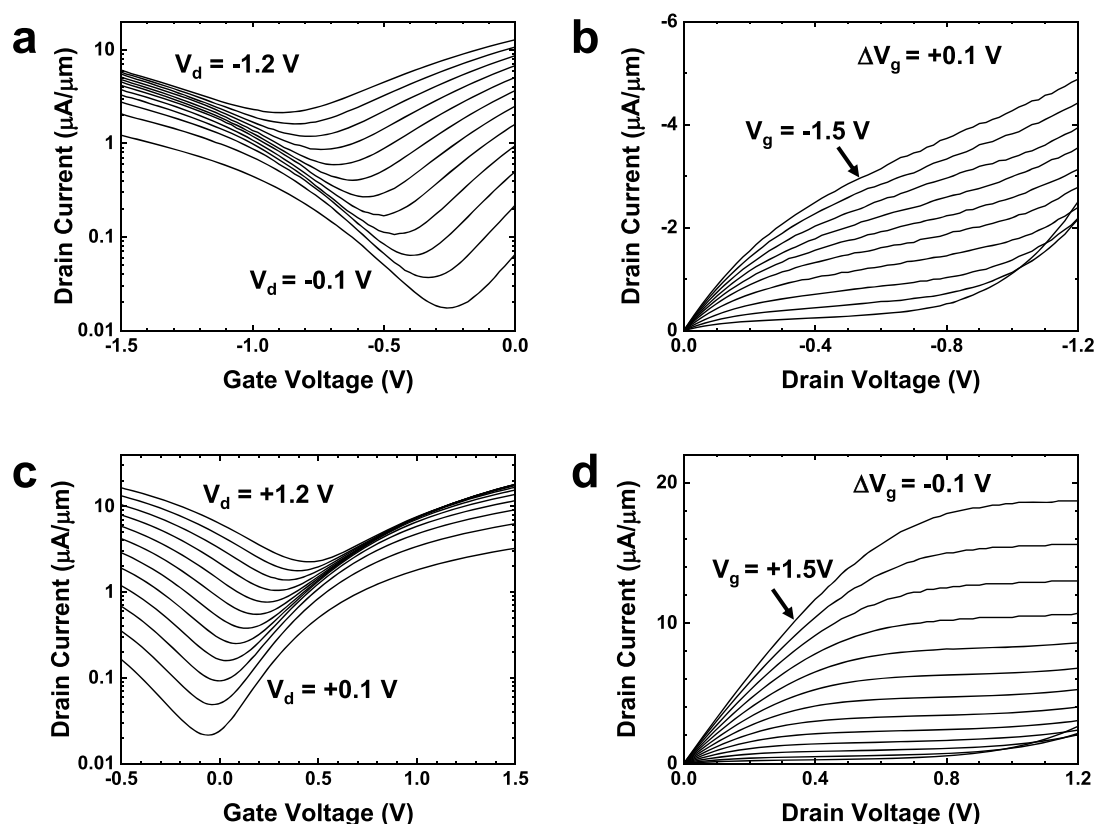


Figure 5. Ambipolar behavior of a BP FET with 15 nm nanogap. (a, b) Transfer and output characteristics of a BP with 15 nm gap with negative drain voltages showing p-type FET characteristics. (c, d) Transfer and output characteristics of the device in (a, b) with positive drain voltages showing n-type FET characteristics.

photocurrent microscopy (SPCM)^{47,48} on the device, as shown in Figure 6a. The device was scanned in a raster pattern, and photocurrent through the gap was recorded with a focused 532 nm laser spot with 320 nW power. Figure 6b shows spatial maps of photocurrents with 50 mV and -50 mV applied voltage. With 50 mV (-50 mV) of applied drain voltage, positive (negative) photocurrent was measured across the gap channel. In both cases, photocurrent was only measured in the gap region, and the photocurrent within nanogap region is larger than in the microgap regions. In the nanogap region, responsivity is measured as high as 40 mA/W. This larger photocurrent in the nanogap region can be attributed to a more effective charge separation from the larger electric field formed between the two electrodes. Thus, our platform can be utilized to build photodetectors with a nanoscale channel simply by placing 2D materials on top of the platform.

CONCLUSIONS

We have developed a scalable method to create an ultraflat nanogap electrode platform based on atomic layer lithography and template-stripping methods. Two metal regions are separated by an Al_2O_3 ALD layer, and the thickness of the Al_2O_3 layer precisely defines the distance between the two metal layers. The two metal surfaces in the platform exhibit ultraflatness, and are vertically aligned without height difference. We utilize the platform to build electronic and optical devices based on 2D materials, simply by placing different 2D material flakes on top of our platform. The ultraflatness across two metal regions should be beneficial to

minimize contact resistance and carrier scattering in the 2D material. We demonstrate FET devices with BP and MoS_2 flakes showing their typical semiconducting characteristics. Furthermore, we show that our platform can be utilized to build photodetectors with nanoscale photosensitive regions using an SPCM setup. Potentially, creation of a bimetallic ultraflat platform composed of different metals⁴⁹ for each electrode would enhance the photodetector performance by facilitating charge carrier separation due to the built-in potential created by the different metal work functions. Notably, since our method to build an ultraflat nanogap platform relies on uniform formation of ALD over wafer scale, optoelectronic devices with controllable nanogap size can be fabricated in a facile manner over large areas.

METHODS

Device Fabrication. For the nanogap formation shown in Figure 2a, an Al_2O_3 layer of desired thickness was deposited on a bare Si wafer using ALD. Electrode patterns were created by photolithography and a 100 nm-thick Au layer was deposited using electron beam evaporation. Phosphoric acid was used to etch the Al_2O_3 layer. The same ALD and metallization method was used to create the second Au electrodes. Optical adhesive (NOA61, Norland Inc.) was used as a backing layer, and a glass slide was used as a support. The adhesive was cured by ultraviolet light exposure and heat treatment on a hot plate ($65\text{ }^\circ\text{C}$ for 12 h). After peeling the nanogap structures off of the Si mold, MoS_2 or BP flakes were mechanically exfoliated and placed on the ultraflat nanogap structures using a microscope-based alignment setup. To protect BP, a 10 nm-thick Al_2O_3 layer was deposited over the whole substrate using ALD.

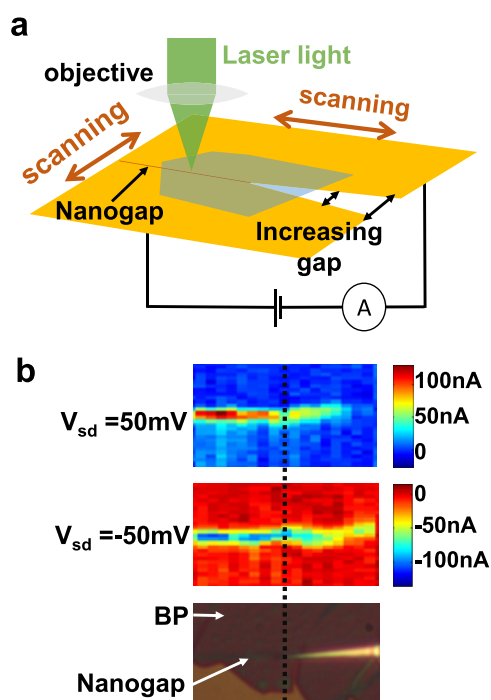


Figure 6. Short-channel photodetector based on ultraflat nanogap platform. (a) Experimental setup for scanning photocurrent microscope. The gap between two electrodes increases from nanoscale gap to microscale gap. (b) Spatial mapping of photocurrent on a BP photodetector based on ultraflat nanogap platform. Enhanced photocurrent is observed on the nanogap region compared to the microscale region.

Device Characterization. SEM (JEOL 6700 FE SEM) and noncontact AFM (Keysight 5500 environmental SPM) were used to characterize nanogap structures and devices. Electrical measurement was performed using an Agilent B1500A semiconductor parameter analyzer in ambient conditions. Ionic liquid (1-butyl-3-methylimidazolium hexafluorophosphate, Sigma-Aldrich) was used for gating, and Pt wire was used for electrical connection. For SPCM, a laser light with a wavelength of 532 nm was focused using a 50 $\times$ objective (0.55 N.A.) for device illumination, and a Keithley 2450 source meter was used to apply a voltage and measure electrical current between source–drain electrodes. The optical power at the sample was determined as 320 nW. The device was scanned in a raster pattern using a piezo-stage (Mad City Laboratories, Inc.) over the fixed laser spot.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsnano.0c10759>.

Further device characterization including surface roughness and FET measurements (PDF)

AUTHOR INFORMATION

Corresponding Authors

Steven J. Koester – Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota 55455, United States; orcid.org/0000-0001-6104-1218; Email: skoester@umn.edu

Sang-Hyun Oh – Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota 55455, United States; orcid.org/0000-0002-6992-5007; Email: sang@umn.edu

Author

Seon Namgung – Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota 55455, United States; Department of Physics, Ulsan National Institute of Science and Technology (UNIST), Ulsan 44919, Republic of Korea

Complete contact information is available at: <https://pubs.acs.org/doi/10.1021/acsnano.0c10759>

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The authors acknowledge funding from the Air Force Office of Scientific Research under award no. FA9550-14-1-0277 (S.N. and S.J.K.). S.-H.O. acknowledges support from the Sanford P. Bordeaux Chair in Electrical Engineering at the University of Minnesota. This work was also supported by the National Research Foundation of Korea (NRF) grant to S.N. by the Korean government (MSIT) (no. 2019R1F1A1060588) and the 2019 Research Fund (1.190095.01) of UNIST (Ulsan National Institute of Science and Technology). Characterization of materials was carried out in the University of Minnesota Characterization Facility, which received capital equipment support from the U.S. National Science Foundation (NSF) through the University of Minnesota MRSEC under NSF award no. DMR-2011401. Device fabrication was performed in the Minnesota Nano Center, which is supported by the NSF through the National Nanotechnology Coordinated Infrastructure (NNCI) under award no. ECCS-2025124.

REFERENCES

- (1) Moore, G. E. Cramming More Components onto Integrated Circuits. *Electronics* **1965**, *38*, 114–117.
- (2) Salahuddin, S.; Ni, K.; Datta, S. The Era of Hyper-Scaling in Electronics. *Nature Electronics* **2018**, *1*, 442–450.
- (3) Bohr, M. T.; Young, I. A. CMOS Scaling Trends and Beyond. *IEEE Micro* **2017**, *37*, 20–29.
- (4) Yan, R.-H.; Ourmazd, A.; Lee, K. F. Scaling the Si MOSFET: From Bulk to SOI to Bulk. *IEEE Trans. Electron Devices* **1992**, *39*, 1704–1710.
- (5) Suzuki, K.; Tanaka, T.; Tosaka, Y.; Horie, H.; Arimoto, Y. Scaling Theory for Double-Gate SOI MOSFETs. *IEEE Trans. Electron Devices* **1993**, *40*, 2326–2329.
- (6) Frank, D. J.; Taur, Y.; Wong, H. S. P. Generalized Scale Length for Two-Dimensional Effects in MOSFET's. *IEEE Electron Device Lett.* **1998**, *19*, 385–387.
- (7) Oh, S.-H.; Monroe, D.; Hergenrother, J. M. Analytical Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical Surrounding-Gate MOSFETs. *IEEE Electron Device Lett.* **2000**, *21*, 445–447.
- (8) Jeong, M.; Doris, B.; Kedzierski, J.; Rim, K.; Yang, M. Silicon Device Scaling to the Sub-10-nm Regime. *Science* **2004**, *306*, 2057–2060.
- (9) Chhowalla, M.; Jena, D.; Zhang, H. Two-Dimensional Semiconductors for Transistors. *Nat. Rev. Mater.* **2016**, *1*, 16052.
- (10) Thiele, S.; Kinberger, W.; Granzner, R.; Fiori, G.; Schwierz, F. The Prospects of Transition Metal Dichalcogenides for Ultimately Scaled CMOS. *Solid-State Electron.* **2018**, *143*, 2–9.
- (11) Liu, H.; Neal, A. T.; Ye, P. D. Channel Length Scaling of MoS₂ MOSFETs. *ACS Nano* **2012**, *6*, 8563–8569.
- (12) Granzner, R.; Geng, Z.; Kinberger, W.; Schwierz, F. MOSFET Scaling: Impact of Two-Dimensional Channel Materials. *2016 13th IEEE ICSICT* **2016**, 466–469.

- (13) Gao, Q. G.; Zhang, Z. F.; Xu, X. L.; Song, J.; Li, X. F.; Wu, Y. Q. Scalable High Performance Radio Frequency Electronics Based on Large Domain Bilayer MoS₂. *Nat. Commun.* **2018**, *9*, 4778.
- (14) Feijoo, P. C.; Jimenez, D.; Cartoixa, X. Short Channel Effects in Graphene-Based Field Effect Transistors Targeting Radio-Frequency Applications. *2D Mater.* **2016**, *3*, 025036.
- (15) Wu, Y.; Lin, Y.-M.; Jenkins, K.; Ott, J.; Dimitrakopoulos, C.; Farmer, D.; Xia, F.; Grill, A.; Antoniadis, D.; Avouris, P. RF Performance of Short Channel Graphene Field-Effect Transistor. Proceedings from the 2010 IEEE International Electron Devices Meeting, San Francisco, CA, Dec 6–8, 2010; IEEE: New York, 2010; pp 9.6.1–9.6.3.
- (16) Miao, J. S.; Zhang, S. M.; Cai, L.; Wang, C. Black Phosphorus Schottky Diodes: Channel Length Scaling and Application as Photodetectors. *Adv. Electron. Mater.* **2016**, *2*, 1500346.
- (17) Patel, K. A.; Grady, R. W.; Smithe, K. K. H.; Pop, E.; Sordan, R. Ultra-Scaled MoS₂ Transistors and Circuits Fabricated without Nanolithography. *2D Mater.* **2020**, *7*, 015018.
- (18) Liao, L.; Lin, Y. C.; Bao, M. Q.; Cheng, R.; Bai, J. W.; Liu, Y. A.; Qu, Y. Q.; Wang, K. L.; Huang, Y.; Duan, X. F. High-Speed Graphene Transistors with a Self-Aligned Nanowire Gate. *Nature* **2010**, *467*, 305–308.
- (19) Cao, W.; Liu, W.; Kang, J. H.; Banerjee, K. An Ultra-Short Channel Monolayer MoS₂ FET Defined by the Curvature of a Thin Nanowire. *IEEE Electron Device Lett.* **2016**, *37*, 1497–1500.
- (20) Xie, L.; Liao, M.; Wang, S.; Yu, H.; Du, L.; Tang, J.; Zhao, J.; Zhang, J.; Chen, P.; Lu, X.; Wang, G.; Xie, G.; Yang, R.; Shi, D.; Zhang, G. Graphene-Contacted Ultrashort Channel Monolayer MoS₂ Transistors. *Adv. Mater.* **2017**, *29*, 1702522.
- (21) Xu, K.; Chen, D.; Yang, F.; Wang, Z.; Yin, L.; Wang, F.; Cheng, R.; Liu, K.; Xiong, J.; Liu, Q.; He, J. Sub-10 nm Nanopattern Architecture for 2D Material Field-Effect Transistors. *Nano Lett.* **2017**, *17*, 1065–1070.
- (22) Jiang, J.; Doan, M. H.; Sun, L.; Kim, H.; Yu, H.; Joo, M. K.; Park, S. H.; Yang, H.; Duong, D. L.; Lee, Y. H. Ultrashort Vertical-Channel van der Waals Semiconductor Transistors. *Adv. Sci.* **2020**, *7*, 1902964.
- (23) Jiang, J.; Doan, M. H.; Sun, L.; Ghimire, M. K.; Kim, H.; Yun, S. J.; Yang, H.; Duong, D. L.; Lee, Y. H. Schottky-Barrier Quantum Well in Two-Dimensional Semiconductor Nanotransistors. *Mater. Today Phys.* **2020**, *15*, 100275.
- (24) George, S. M. Atomic Layer Deposition: an Overview. *Chem. Rev.* **2010**, *110*, 111–131.
- (25) Leskelä, M.; Ritala, M. Atomic Layer Deposition Chemistry: Recent Development and Future Challenges. *Angew. Chem., Int. Ed.* **2003**, *42*, 5548–5554.
- (26) Hegner, M.; Wagner, P.; Semenza, G. Ultralarge Atomically Flat Template-Stripped Au Surfaces for Scanning Probe Microscopy. *Surf. Sci.* **1993**, *291*, 39–46.
- (27) Weiss, E. A.; Kaufman, G. K.; Kriebel, J. K.; Li, Z.; Schalek, R.; Whitesides, G. M. Si/SiO₂-Templated Formation of Ultraflat Metal Surfaces on Glass, Polymer, and Solder Supports: Their Use as Substrates for Self-Assembled Monolayers. *Langmuir* **2007**, *23*, 9686–9694.
- (28) Nagpal, P.; Lindquist, N. C.; Oh, S.-H.; Norris, D. J. Ultrasoft Patterned Metals for Plasmonics and Metamaterials. *Science* **2009**, *325*, 594–597.
- (29) Yang, J.-C.; Gao, H.; Suh, J. Y.; Zhou, W.; Lee, M. H.; Odom, T. W. Enhanced Optical Transmission Mediated by Localized Plasmons in Anisotropic, Three-Dimensional Nanohole Arrays. *Nano Lett.* **2010**, *10*, 3173–3178.
- (30) Lindquist, N. C.; Nagpal, P.; McPeak, K. M.; Norris, D. J.; Oh, S.-H. Engineering Metallic Nanostructures for Plasmonics and Nanophotonics. *Rep. Prog. Phys.* **2012**, *75*, 036501.
- (31) Yang, Y.; Gu, C. Z.; Li, J. J. Sub-5 nm Metal Nanogaps: Physical Properties, Fabrication Methods, and Device Applications. *Small* **2019**, *15*, 1804177.
- (32) Xu, Y.; Ji, D. X.; Song, H. M.; Zhang, N.; Hu, Y. W.; Anthopoulos, T. D.; Di Fabrizio, E. M.; Xiao, S. M.; Gan, Q. Light-Matter Interaction within Extreme Dimensions: From Nano-manufacturing to Applications. *Adv. Opt. Mater.* **2018**, *6*, 1800444.
- (33) Ren, Z. H.; Chang, Y. H.; Ma, Y. M.; Shih, K. L.; Dong, B. W.; Lee, C. Leveraging of MEMS Technologies for Optical Metamaterials Applications. *Adv. Opt. Mater.* **2020**, *8*, 1900653.
- (34) Xiang, D.; Jeong, H.; Lee, T.; Mayer, D. Mechanically Controllable Break Junctions for Molecular Electronics. *Adv. Mater.* **2013**, *25*, 4845–4867.
- (35) Zaretski, A. V.; Marin, B. C.; Moetazedi, H.; Dill, T. J.; Jibril, L.; Kong, C.; Tao, A. R.; Lipomi, D. J. Using the Thickness of Graphene to Template Lateral Subnanometer Gaps between Gold Nanostructures. *Nano Lett.* **2015**, *15*, 635–640.
- (36) Ji, D. X.; Cheney, A.; Zhang, N.; Song, H. M.; Gao, J.; Zeng, X.; Hu, H. F.; Jiang, S. H.; Yu, Z. F.; Gan, Q. Efficient Mid-Infrared Light Confinement within Sub-5-nm Gaps for Extreme Field Enhancement. *Adv. Opt. Mater.* **2017**, *5*, 1700223.
- (37) Zhang, N.; Hu, H. F.; Singer, M.; Li, K. H.; Zhou, L.; Ooi, B. S.; Gan, Q. Large-Scale Sub-1-nm Random Gaps Approaching the Quantum Upper Limit for Quantitative Chemical Sensing. *Adv. Opt. Mater.* **2020**, *8*, 2001634.
- (38) Cai, H. B.; Meng, Q. S.; Zhao, H.; Li, M. L.; Dai, Y. M.; Lin, Y.; Ding, H. Y.; Pan, N.; Tian, Y. C.; Luo, Y.; Wang, X. P. High-Throughput Fabrication of Ultradense Annular Nanogap Arrays for Plasmon-Enhanced Spectroscopy. *ACS Appl. Mater. Interfaces* **2018**, *10*, 20189–20195.
- (39) Li, L. K.; Yu, Y. J.; Ye, G. J.; Ge, Q. Q.; Ou, X. D.; Wu, H.; Feng, D. L.; Chen, X. H.; Zhang, Y. B. Black Phosphorus Field-Effect Transistors. *Nat. Nanotechnol.* **2014**, *9*, 372–377.
- (40) Haratipour, N.; Namgung, S.; Oh, S.-H.; Koester, S. J. Fundamental Limits on the Subthreshold Slope in Schottky Source/Drain Black Phosphorus Field-Effect Transistors. *ACS Nano* **2016**, *10*, 3791–3800.
- (41) Wood, J. D.; Wells, S. A.; Jariwala, D.; Chen, K. S.; Cho, E.; Sangwan, V. K.; Liu, X.; Lauhon, L. J.; Marks, T. J.; Hersam, M. C. Effective Passivation of Exfoliated Black Phosphorus Transistors against Ambient Degradation. *Nano Lett.* **2014**, *14*, 6964–6970.
- (42) Li, X. F.; Yu, Z. Q.; Xiong, X.; Li, T. Y.; Gao, T. T.; Wang, R. S.; Huang, R.; Wu, Y. Q. High-Speed Black Phosphorus Field-Effect Transistors Approaching Ballistic Limit. *Sci. Adv.* **2019**, *5*, No. eaau3194.
- (43) Desai, S. B.; Madhvapathy, S. R.; Sachid, A. B.; Llinas, J. P.; Wang, Q. X.; Ahn, G. H.; Pitner, G.; Kim, M. J.; Bokor, J.; Hu, C. M.; Wong, H. S. P.; Javey, A. MoS₂ Transistors with 1-Nanometer Gate Lengths. *Science* **2016**, *354*, 99–102.
- (44) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS₂ Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147–150.
- (45) Koppens, F. H. L.; Mueller, T.; Avouris, P.; Ferrari, A. C.; Vitiello, M. S.; Polini, M. Photodetectors Based on Graphene, Other Two-Dimensional Materials and Hybrid Systems. *Nat. Nanotechnol.* **2014**, *9*, 780–793.
- (46) Long, M. S.; Wang, P.; Fang, H. H.; Hu, W. D. Progress, Challenges, and Opportunities for 2D Material Based Photodetectors. *Adv. Funct. Mater.* **2019**, *29*, 1803807.
- (47) Graham, R.; Yu, D. Scanning Photocurrent Microscopy in Semiconductor Nanostructures. *Mod. Phys. Lett. B* **2013**, *27*, 1330018.
- (48) Namgung, S.; Shaver, J.; Oh, S.-H.; Koester, S. J. Multimodal Photodiode and Phototransistor Device Based on Two-Dimensional Materials. *ACS Nano* **2016**, *10*, 10500–10506.
- (49) Chen, X.; Ciraci, C.; Smith, D. R.; Oh, S.-H. Nanogap-Enhanced Infrared Spectroscopy with Template-Stripped Wafer-Scale Arrays of Buried Plasmonic Cavities. *Nano Lett.* **2015**, *15*, 107–113.