



Electrical and electrothermal properties of few-layer 2D devices

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Abstract

While two-dimensional (2D) materials have emerged as a new platform for nanoelectronic devices with improved electronic, optical, and thermal properties, and their heightened sensitivity to electrostatic and mechanical interactions with their environment has proved to be a bottleneck. Few-layer (FL) 2D devices retain the desirable thinness of their monolayer cousins while boosting carrier mobility. Here, we employ an electrothermal model to study FL field-effect devices made from transition metal dichalcogenides MoS₂ and WSe₂ and examine the effect of both electrical and thermal interlayer resistances, as well as the thermal boundary resistance to the substrate, on device performance. We show that overall conductance improves with increasing thickness (number of layers) at small gate voltages, but exhibits a peak for large gate voltages. Joule heating impacts performance due to relatively poor thermal conductance to the substrate and this impact, along with the location of the hot spot in the FL stack, varies with carrier screening length of the material. We conclude that coupled electrothermal simulation can be employed to design FL 2D devices with improved performance.

Keywords Transition metal dichalcogenides · Heat dissipation · Thermal boundary conductance

1 Introduction

The persistent downscaling of nanostructures, such as electronic devices, sensors, NEMS, or nanocomposites, increases the surface-to-volume ratio and introduces atomic-scale disorder at boundaries and interfaces. To avoid these issues, the nanoelectronic community has turned to intrinsically two-dimensional (2D) material platforms. 2D materials, including graphene [1] and transition metal dichalcogenides [2, 3] (TMDCs, e.g., MoS₂, WSe₂, etc.), have extraordinary structural, mechanical, and physical properties. Devices made up of single-layer (SL), few-layer (FL) 2D materials, and their heterostructures hold tremendous potential for next-generation nanoelectronic applications, including low-power devices and optoelectronics [4–6].

While 2D materials provide intriguing opportunities for future device applications, thermal management in them can become a challenge. Heat removal in 2D FETs is mainly cross-plane through the substrate, owing to the small thermal healing length (a measure of lateral heat spreading, around

100 nm) [7] and large lateral/vertical aspect ratio. Current in FL graphene, MoS₂, and WSe₂ is vertically localized in a few layers [8–10], causing a hot spot, and the location and spread of this hot spot depend on gate voltage via the carrier concentration in each layer. At the same time, the thermal boundary conductance (TBC), which is the metric for heat removal in the cross-plane direction, is largest for layers nearest the substrate [11] and decreases as the layers move further from the substrate. Cross-plane thermal transport across the 2D–3D interface is hampered by the van der Waals (vdW) bonds that govern the interface, which are weaker than covalent bonds and thus known for reducing interface thermal transport [12, 13].

Heat dissipated by electrons is carried to the substrate via quantized lattice vibrations (phonons) whose transmission is limited by the large difference between the phase spaces of the 2D material and the 3D substrate, small overlap between their vibrational densities of states, and the mechanical mismatch between the stiff substrate and soft out-of-plane flexural phonon modes, which transfer most of the heat across the interface [14]. However, the total TBC of few-layer stacks involving graphene increases with increasing layers due to the aggregate contributions from additional layers as compared to single-layer counterparts [15]. In addition to Joule heating, the temperature of the dissimilar interfaces

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can be asymmetrically modulated due to the thermoelectric Peltier effect. The geometry mismatch between the 2D materials and their metal electrodes (i.e., difference in the thickness) can also give rise to localized heating near the electrodes due to the current crowding effect.

To date, researchers have developed a thorough understanding of heat dissipation through contacts (in the in-plane direction) and substrates (in the cross-plane direction) for SL 2D FETs. However, heat dissipation and transport from hot spots in FL 2D devices remains far less explored. We have developed a multi-physics, self-consistent electrothermal model for calculating the per-layer temperature rise resulting from Joule heating in FL TMDC FETs [16]. Our electrothermal model captures the competing influences of a decreasing per-layer TBC and increasing temperature-dependent per-layer mobility. Furthermore, we analyze the impact of the channel length and number of layers in the FL stack on thermal and electrical properties. Lastly, we note that the accurate modeling of thermal interfaces involving 2D materials can greatly improve the effectiveness of subsequent finite element calculations for large-scale device integration where reliable inputs for thermal interface resistance must be used.

2 Background

The ultrathin nature and relatively weak vdW interlayer bonding of 2D materials may offer several key advantages for future integrated circuits. The thinness improves electrostatic control and facilitates device downscaling, while the vdW bonding allows stacking. Taken together, they could extend Moore's law and enable high-density device integration for modern integrated circuit designs. Atomic flatness and the absence of dangling bonds prevent scattering due to surface roughness (SR), which severely limited mobility in ultrathin body 3D silicon-on-insulator (SOI) field-effect transistors (FETs). For example, graphene has superlative electrical and thermal conductivity, foldability, and optical transparency, with an intrinsic carrier mobility of over $200,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [17]. However, it lacks band gap—a basic requirement for switching field-effect transistor (FET) applications; in contrast, TMDCs all have an energy band gap which makes them preferable candidates for applications in digital logic, optoelectronics, and photovoltaics.

One major challenge with SL TMDCs is that they typically exhibit degraded carrier mobility and poor electrical conductance relative to their bulk versions due to strong Coulomb scattering with charged interfacial impurities [18–21]. Measured room temperature (RT) mobility of monolayer MoS_2 on SiO_2 substrate ranges from 0.1 to $55 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [22–24]. In the past few years, there have been significant research efforts invested toward growing high-quality, impurity- and defect-free TMDCs to improve

their mobility. Another route to higher mobility is encapsulating the monolayer with a 2D insulator, such as hexagonal boron nitride (hBN) [25]. However, these methods are time-intensive and expensive.

A viable alternative is to use few-layer (FL) TMDCs instead of their SL counterparts. Carrier mobility has been found to improve significantly with the number of layers in FL TMDCs, with highest RT mobility of $700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ attained in 10-nm-thick (13-layer) FL MoS_2 FET [10]. A record high Hall mobility of $34,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ has been reported for a 6-layer MoS_2 FET encapsulated between hexagonal boron nitride (hBN) layers at 3 K [24]. A more recent study reported a RT mobility of about $60 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in FL MoS_2 flakes grown by chemical vapor deposition (CVD) [26], a popular and economical method for growing wafer-scale thin films. In FL WSe_2 , mobility reached $350 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in 10-layer samples at RT [27]. Mobility of such CVD-grown FL TMDCs is also significantly higher than those of organic semiconductors, currently used for wearable electronics, which makes FL TMDCs an ideal substitute for organic semiconductors.

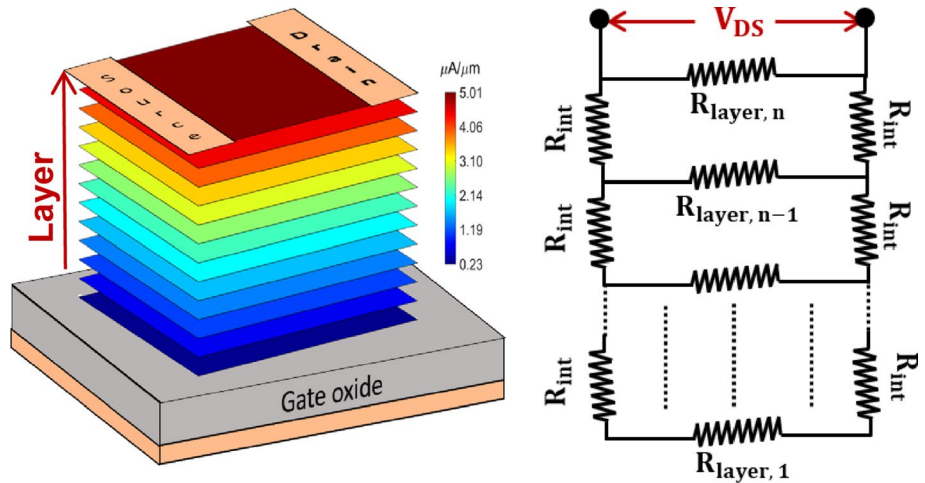
Contact resistance R_c plays a major role in influencing the field-effect mobility of an FET. In FL TMDC FETs, contact resistance has two components—one arising from the resistance between the metal and top layer of the TMDC and the other stems from the resistance between the layers, often referred to as *interlayer resistance* R_{int} . Das and Appenzeller [9] used a transfer length method (TLM) to calculate an average interlayer resistance and found it to be inversely proportional to the gate voltage. Chang et al. [28] proposed a modified Y-function method (YFM) to fit their resistances extracted from TLM. YFM has been further used to explain the thickness-dependent behavior in FL MoS_2 transistors [29]. Both the approaches—TLM and YFM—use the idea that channel and contact resistances are decoupled and can be treated as series resistors, and thus, the total resistance can, simply, be written as their sum. However, this is an approximation which works well only when the interlayer resistance is considerably smaller than the layer resistances. In our model, we overcome this limitation by treating the resistances of each layer and the interlayer resistances between them separately in a resistor network model.

3 Methodology

3.1 Multilayer 2D resistive network model

The current distribution in FL TMDC FETs is represented as a resistive network [9], as shown in Fig. 1. The resistive network comprises of layer resistors, representing the resistance of each monolayer, and interlayer resistors, representing the resistance between adjacent layers due to interlayer coupling. $R_1, R_2, \dots$

Fig. 1 (left) A schematic of the non-uniform current distribution and the pathway of heat removal (right) a resistance network model representing current flow in a FL-2D FET



R_N are the resistances of layers 1, 2, ... N , respectively. In this model, the metal (source and drain) contacts are considered to be deposited on the topmost layer, resulting in current injection that starts at the top of the FL stack and farthest from the substrate. The current faces an additional interlayer resistance R_{int} to access the next bottom layer. The extent of current penetration through the stack depends on the strength of R_{int} with respect to the layer resistances. A smaller value of R_{int} means the current can readily penetrate to the bottom layers, whereas a larger value of R_{int} restricts the current flow to few layers from the top.

The layer resistances are calculated as the product of carrier densities and mobilities of each layer, $R_i = (\frac{L}{W})(qn_i\mu_i)^{-1}$. The total charge on the gate is calculated as $Q_{\text{total}} = C_{\text{ox}}(V_{\text{GS}} - V_{\text{th}})$. However, due to charged impurity screening, the distribution of carriers across layers is non-uniform. Due to back-gating, the carrier density is maximum in the bottommost layer and decreases exponentially with distance from the substrate. A Thomas–Fermi charge screening length λ is used to find out the distribution of carriers among layers, which is given by the ratio $\frac{n_{i+1}}{n_i} = \exp(-\frac{d_{\text{ML}}}{\lambda})$ such that the total charge induced in the channel is equal to the charge on the gate $Q_{\text{total}} = q \sum_{i=1}^N n_i$. Here, d_{ML} is the distance between two adjacent layers. Like the charge density, the distribution of carrier mobilities is also non-uniform. The mobility in SL TMDCs is found to be strongly dominated by charged impurity scattering [20], whereas a phonon-limited mobility is observed in the bulk counterparts [30]. In a FL TMDC, charged impurity scattering is strongest for the bottommost layer and decreases with the layers away from the substrate due to Thomas–Fermi charge screening. Thus, the mobility of the individual layers is modeled as [9, 16]

$$\mu_i(n_i, T_i) = \mu_1(n_i) + [\mu_{\infty}(T_i) - \mu_1(n_i)] \left[1 - \exp\left(-\frac{(i-1)d_{\text{ML}}}{\lambda}\right) \right], \quad (1)$$

where μ_{∞} and μ_1 are the bulk and single-layer mobility of the TMDC. The single-layer mobility of TMDCs is calculated based on our previous work [31], which includes acoustic, optical, and remote surface optical phonon, as well as charged impurity scattering.

Employing the resistive network model, one can fit experimentally measured I_D – V_{DS} curves for different gate voltages at temperature T to extract the unknown model parameters— R_{int} , $\mu_{\infty}(T)$, and λ . In our recent study on FL WSe_2 , we obtained R_{int} , $\mu_{\infty}(300 \text{ K})$, and λ to be 6 k Ω , 114 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, and 13 nm. The screening lengths for graphene and MoS_2 are 1 and 7 nm, respectively [8, 9], owing to the differences between their electronic structures. In this work, we vary the value for λ while using same values for R_{int} and μ_{∞} to compare electrical properties of graphene, MoS_2 , and WSe_2 . Using λ , layer resistances ($R_1, R_2, \dots, R_N$) are calculated. Then, we go on to calculate the current distributions across all the layers, followed by layer-wise Joule heating. The non-uniform current distribution results in non-uniform Joule heating across different layers of the FL 2D stack. Heat dissipation in the i th-layer is given by $H_i = I_i^2 R_i$. Then we obtain layer-dependent thermal boundary conductance (TBC) values calculated from our multilayer TBC model, discussed in the next subsection.

On finding the heat dissipation H_i of each layer and their respective thermal boundary conductance TBC_i , we obtain the layer-wise temperature rise in the multilayer stack using $\Delta T_i = H_i / \text{TBC}_i$. For small drain–source voltages V_{DS} , the layer-wise temperature rise ΔT_i is also small. However, for large V_{DS} , the device self-heats causing the mobility $\mu_{\infty}(T'_i)$ to deteriorate. Experimentally, it has been found that the temperature-dependent bulk mobility exhibits a power-law behavior $\mu_{\infty}(T'_i) = \mu_{\infty}(T_i) \times (T'_i/T_i)^{-1.9}$ [30]. Depending on the temperature rise, the mobility of each layer (based on Eq. 1) is updated, and layer-wise resistances R_i and Joule heating H_i are recalculated. Using TBC_i from our thermal model, new layer temperatures T'_i are calculated. This

electrothermal coupling is used to set up an iterative loop, where we update ΔT_i based on the temperature-dependent mobility of the previous iteration. We continue this iteration until the total power dissipation $\sum_i H_i$ reaches convergence, which we define to be the point when the difference of the total power dissipation between two consecutive iterations is less than $1 \mu\text{W} \mu\text{m}^{-2}$.

3.2 Multilayer thermal boundary conductance model

Upon injection, electrons in the 2D layer scatter with the crystal lattice distributing their thermal energy and heating up the 2D layer. Quantized lattice vibrations, or phonons, carry thermal energy through contacts with the source, drain, and into the substrate. Due to the large surface area contact with the substrate, the majority of thermal energy will be removed across the 2D–3D interface and via the substrate. A key challenge in modeling 2D–3D heat transfer is that the phonons in the 2D layer travel in-plane—their momenta and velocities only have components in the two-dimensional phase space of the layer. Consequently, the 2D phonons never impinge on the interface, but instead travel parallel to it, so energy transfer to the substrate occurs only through out-of-plane atomic motion due to flexural (ZA) phonons and their stretching/compressing of the vdW bonds that connect the 2D layer and substrate [32–35]. The vibrational modes of the 2D material and the substrate are treated in their bulk form, with the phonon dispersion calculated for the uncoupled 2D and 3D materials from density functional theory in the supercell approach. This is accomplished with existing codes: Quantum Espresso [48, 47] for DFT and Phonopy [120] for the calculation of phonon modes in the supercell approach. This approach is computationally efficient because the two materials are treated separately and their vibrational frequencies can be computed on relatively small supercells.

First-principles calculated vibrational modes can then be used as inputs to a cross-dimensional 2D–3D thermal boundary conductance model that can be derived from the semiclassical phonon Boltzmann transport equation (pBTE) [36]. The steady-state phonon Boltzmann transport equation (pBTE) for ZA phonons with the relaxation time approximation (RTA) [37] is

$$\vec{v}_{\text{ZA}}(\vec{q}) \cdot \nabla T \frac{dN_0(\omega)}{dT} = -\frac{N_{\text{ZA}}(\vec{q}) - N_0(T)}{\tau_{\text{total}}(\omega)}. \quad (2)$$

$N_{\text{ZA}}(\vec{q})$ is the out-of-equilibrium ZA phonon distribution function, N_0 is the Bose–Einstein distribution, $N_0(T) = [\exp(\frac{\hbar\omega}{k_B T}) - 1]^{-1}$, $\tau_{\text{total}}^{-1}(\omega)$ is the total scattering rate from all mechanisms, and $\vec{v}_{\text{ZA}}$ and ω are the group velocity and angular frequency of ZA phonons, respectively. Since

the 2D layer and the substrate are at different temperatures, we must separate the total scattering rate $\Gamma_{\text{total}} = \tau_{\text{total}}^{-1}$ into two parts: one capturing the interactions of ZA phonons with other phonons (termed Γ_{int}) at T_H and the other capturing ZA phonon interactions with the vibrational modes in the substrate (termed Γ_{sub}) at T_{sub} , where typically $T_{\text{sub}} < T_H$. The pBTE then expands into

$$\vec{v}_{\text{ZA}}(\vec{q}) \cdot \nabla T \frac{dN_0(\omega)}{dT} = -\Gamma_{\text{sub}}(\omega)[N_{\text{ZA}}(\vec{q}) - N_0(T_{\text{sub}})] - \Gamma_{\text{int}}(\omega)[N_{\text{ZA}}(\vec{q}) - N_0(T_H)], \quad (3)$$

where Γ_{int} is the internal scattering rate of the 2D layer driving the out-of-equilibrium ZA phonon distribution N_{ZA} to an equilibrium distribution at T_H and Γ_{sub} is the substrate scattering rate driving N_{ZA} to an equilibrium distribution at T_{sub} . Assuming uniform heating across the 2D layer, we solve for the out-of-equilibrium distribution function of ZA phonons N_{ZA} as

$$N_{\text{ZA}}(\vec{q}) = \frac{\Gamma_{\text{sub}}(\omega)N_0(T_{\text{sub}}) + \Gamma_{\text{int}}(\omega)N_0(T_H)}{\Gamma_{\text{sub}}(\omega) + \Gamma_{\text{int}}(\omega)}. \quad (4)$$

From the above, the heat flux into the substrate can be solved by integrating over the frequency spectrum as $Q = \int \hbar\omega \Gamma_{\text{sub}}(\omega) N_{\text{ZA}}(\vec{q}) D_{2D}(\omega) d\omega$, where $D_{2D}(\omega)$ is the vibrational density of states (vDOS) of the 2D layer. Substituting N_{ZA} into the heat flux Q and expanding for a small temperature gradient $\Delta T = T_H - T_{\text{sub}}$, the TBC for single layer is obtained as

$$\text{TBC}(T) = \frac{Q}{\Delta T} = \int \hbar\omega \frac{dN_0(T)}{dT} \Gamma_{\text{sub}}(\omega) \frac{\Gamma_{\text{int}}(\omega)}{\Gamma_{\text{sub}}(\omega) + \Gamma_{\text{int}}(\omega)} D_{2D}(\omega) d\omega. \quad (5)$$

The above expression is solved numerically using the phonon dispersion and vibrational density of states of the 2D layer and substrate as inputs.

It is important here to emphasize the counterintuitive role of scattering from the perspective of 2D–3D cross-plane interfacial transport as compared to the picture of in-plane energy transport. In the case of cross-plane transport, more substrate scattering leads to more ZA phonons transferring their energy across the 2D–3D interface and therefore a higher TBC. However, this elastic process depletes the ZA phonon population in the 2D layer which is replenished by internal phonon scattering mechanisms (Γ_{int}). If internal scattering is weak, then the repopulation of ZA phonons will be slow leading to an internal bottleneck of heat transport from the 2D layer into the substrate. The $\Gamma_{\text{sub}}\Gamma_{\text{int}}/[\Gamma_{\text{sub}} + \Gamma_{\text{int}}]$ term in Eq. (5) illustrates this relation and is equivalent to two conductors in series: one representing internal heat transfer from in-plane to out-of-plane phonons and the other external heat transfer from out-of-plane phonons to the substrate. We denote the resistance

associated with the substrate scattering rate Γ_{sub} as the *external resistance* and the additional resistance caused by weak internal scattering Γ_{int} as the internal resistance.

The rate at which ZA phonons in a single 2D layer are perturbed by the substrate is derived from Fermi's golden rule [35, 38]

$$\Gamma_{\text{sub}}(\omega) = \frac{\pi}{2} \frac{D_{\text{sub}}(\omega)}{m_{\text{sub}} m_{2\text{D}}} \frac{K_{\text{sub}}^2}{\omega^2}, \quad (6)$$

where D_{sub} and m_{sub} are the vDOS and surface atom mass of the substrate, respectively, $m_{2\text{D}}$ is the unit cell mass of the 2D layer, and K_{sub} is the vdW spring coupling constant. For a given substrate, $\Gamma_{\text{sub}}(\omega)$ is proportional to $1/\omega^2$ and is independent of temperature. The $1/\omega^2$ dependence suggests that the majority of phonon transfer across the interface comes from long-wavelength, low-energy phonons with q-vectors close to the center of the Brillouin zone. The substrate scattering rate for a single 2D layer can readily be extended to FL stacks [11, 15] taking the form,

$$\Gamma_{i,\text{sub}}^{\text{FL}}(\omega) = \frac{\pi}{2} \left[\frac{m_{2\text{D}}}{K_{\text{sub}}} + \frac{(i-1)m_{2\text{D}}}{K_z} \right]^{-2} \frac{m_{2\text{D}}}{m_{\text{sub}}} \frac{D_{\text{sub}}(\omega)}{\omega^2}, \quad (7)$$

where K_z is the interlayer vdW coupling constant between repeating 2D monolayers. The $(i-1)$ term in $\Gamma_{i,\text{sub}}^{\text{FL}}$ leads to a reduction in the per-layer substrate scattering rate as the layer moves further from the substrate.

In modeling the internal scattering mechanisms that repopulate the ZA phonon population to facilitate interface transport, consideration is given to anharmonic three-phonon (normal and umklapp) scattering, phonon-boundary scattering, and scattering with an encapsulating layer when one is present. We compute the frequency- and temperature-dependent normal and umklapp three-phonon scattering rates (Γ_N and Γ_U) following the empirical formalism presented by Morelli et al. [39], where both rates increase linearly with temperature— $\Gamma_{U,N} \propto T$. For high thermal conductivity 2D materials that have a large ZA branch contribution, internal scattering could be quite weak leading to a thermal bottleneck caused by slow repopulation of ZA phonons. It may then become necessary to increase internal scattering to boost TBC at the cost of decreasing in-plane thermal transport in 2D materials where the ZA branch contributes significantly to in-plane transport. To this end, it has been shown that coating the 2D layer stack with an encapsulating layer increases internal scattering and can therefore help reduce internal resistance [36]. ZA phonon interactions with an encapsulating layer are analogous to those with the substrate; however, in this case the 2D layer and the coating layer are thermally equilibrated at the steady state, assuming thermal radiation from the surface of the encapsulation is negligible. As a result, the scattering rate for an

encapsulating layer must satisfy the principle of detailed balance and takes the form

$$\Gamma_{i,\text{enc}}^{\text{FL}}(\omega) = \frac{\pi}{2} \left[\frac{m_{2\text{D}}}{K_{\text{enc}}} + \frac{(\text{NL}-i)m_{2\text{D}}}{K_z} \right]^{-2} m_{2\text{D}} \left[\frac{D_{\text{enc}}(\omega)}{m_{\text{enc}}} + \frac{D_{2\text{D}}(\omega)}{m_{2\text{D}}} \right] \frac{1}{\omega^2}, \quad (8)$$

where NL is the total number of layers, $D_{\text{enc}}(\omega)$ is the vDOS of the substrate, and m_{enc} is the mass of the surface atoms of the encapsulating layer. Contrary to the substrate scattering rate, here the scattering is largest for layers nearest the encapsulating layer. Since the 2D layer and the encapsulating layer are thermally equilibrated, there is no net heat flux between them and phonons that transfer from the 2D layer into the encapsulating layer are replenished by phonons of equal energy from the encapsulating layer. Because of the symmetry, the effect of encapsulation is analogous to an increase in the internal scattering of ZA phonons and their rates are added. By repopulating the ZA phonons, encapsulation reduces internal resistance and boosts overall TBC.

Combining the above, we compute the layer-dependent TBC from

$$\text{TBC}_i(T) = \frac{Q}{\Delta T} = \int \hbar \omega \frac{dN_0(T)}{dT} \Gamma_{i,\text{sub}}^{\text{FL}}(\omega) \frac{\Gamma_{i,\text{int}}^{\text{FL}}(\omega, T)}{\Gamma_{i,\text{sub}}^{\text{FL}}(\omega) + \Gamma_{i,\text{int}}^{\text{FL}}(\omega, T)} D_{2\text{D}}(\omega) d\omega, \quad (9)$$

where $\Gamma_{i,\text{int}}^{\text{FL}}(\omega, T) = \Gamma_N(\omega, T) + \Gamma_U(\omega, T) + \Gamma_{\text{bound}}$ for uncoated stacks and $\Gamma_N(\omega, T) + \Gamma_U(\omega, T) + \Gamma_{\text{bound}} + \Gamma_{i,\text{enc}}^{\text{FL}}(\omega)$ for encapsulated stacks. We employ the above model to perform a comprehensive analysis of temperature and thickness-dependent TBC of uncoated and aluminum oxide (AlO_x)-coated single- and few-layer graphene, MoS_2 , and WSe_2 supported by an amorphous SiO_2 substrate.

4 Results

4.1 Thickness-dependent electrical properties

Thickness dependence of low-field electrical properties has been studied for various 2D materials including graphene, MoS_2 , MoSe_2 , WSe_2 , and black phosphorus. The field-effect mobility, and hence the conductance, has been found to improve with device thickness which is a direct consequence of screened Coulomb potential in top layers due to substrate impurities. Figure 2 shows conductance per layer (G_i) in an N -layer stack for $N=5$ (blue), $N=10$ (green), $N=20$ (yellow), $N=30$ (red) and $N=40$ (cyan). Figures in each column are grouped based on the screening lengths with λ equal to 13 nm (WSe_2), 7 nm (MoS_2), and 1 nm (graphene), respectively, from left to right. Further, figures on the top and bottom rows correspond to ON-state (overdrive

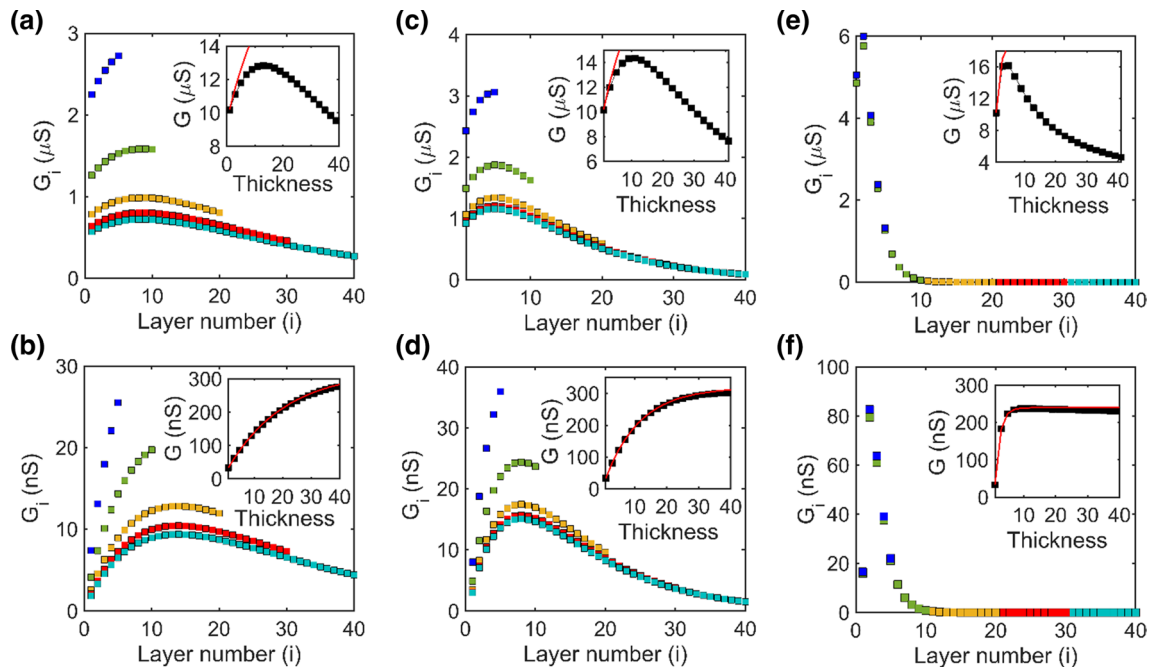


Fig. 2 Electrical conductance per layer (G_i) in an N -layer 2D stack, N being 5, 10, 20, and 30 represented by blue, yellow, red, and cyan, respectively. **a**, **c**, and **e** are plotted for an overdrive voltage (V_{ov}) of 30 V, and **b**, **d**, and **f** represent OFF-state ($V_{ov} = 1$ V). Figures in each column represent different screening lengths— λ equal to 13, 7, and

1 nm from left to right corresponding to graphene, MoS₂, and WSe₂, respectively. The thickness dependence of device conductance is shown in the inset of each figure with black square markers. The red line shows the device conductance ($\sum_i G_i$) when $R_{int} = 0$ (Color figure online)

voltage $V_{ov} = 30$ V) and OFF-state ($V_{ov} = 1$ V) conductance, respectively. While the gate-induced carrier concentration decays exponentially away from the substrate, carrier mobility improves rapidly due to reduced charged impurity scattering in top layers. Consequently, a peak in conductance occurs around intermediate layers depending on the screening length. In Fig. 2a and b [$\lambda = 13$ nm], the 9th layer is the most conductive layer, whereas for $\lambda = 1$ nm, $i = 3$ has the maximum conductance [see Fig. 2e and f]. Layer 5 is the most conductive layer for $\lambda = 7$ nm shown in Fig. 2c and d. The shape of the peak of G_i versus layer number determines the active layers that are carrying the majority of the current through the device.

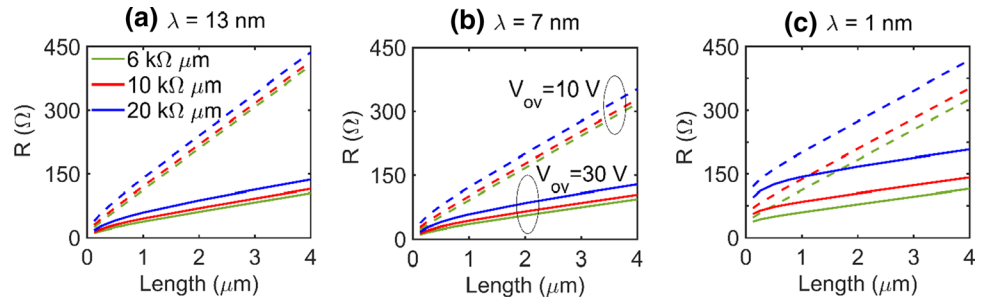
The insets in Fig. 2 show the total conductance (square markers) for various thicknesses; here, thickness represents number of layers in the stack. The red lines in the insets represent the total conductance if there was no interlayer resistance ($R_{int} = 0$)—the sum of conductance of all layers, $\sum_i G_i$. We can see that when the device is in an OFF-state [Fig. 2b, d, f], R_{int} plays a negligible role and the resistor network can be simplified to a network of parallel resistors. In such a case, the conductance of the stack is given by the sum of the conductance of all layers. However, in the ON-state [Fig. 2a, c, e], interlayer resistance plays a major role in determining the conductance of the device. For the current to access the intermediate layers, which are relatively

more conductive, there is a penalty of voltage drop across each interlayer resistance, resulting into a deviation from the red line. Therefore, there is an optimum number of layers (thickness) for the device to have maximum conductance—13, 11, and 5 layers for λ equal to 13 nm, 7 nm, and 1 nm, respectively.

5 Length-dependent electrical properties

The resistance of a 13-layer stack is plotted against length for different screening lengths $\lambda = 13, 7$, and 1 nm in Fig. 3a–c, respectively. The resistance varies linearly with length of the device for $L > 500$ nm for all λ . For smaller lengths, the layer resistance ($\propto L$) becomes comparable to R_{int} , which is independent of L , and therefore, the resistance exhibits a nonlinear dependence. Device resistance is also plotted for different R_{int} shown by green (6 k Ω μ m), red (10 k Ω μ m), and blue (20 k Ω μ m) lines. R_{int} plays a weaker role for $\lambda = 13$ nm than λ equal to 1 nm. In devices made of materials with larger λ , the top layers are quite conductive, as shown in Fig. 2. Therefore, a larger fraction of total current flows through the top layers resulting into smaller voltage drops across interlayer resistances. For $\lambda = 1$ nm, since the active layers are near the bottom of the stack, majority of the

Fig. 3 Dependence of device resistance on channel length for different λ **a** 13 nm, **b** 7 nm, and **c** 1 nm. Green, red, and blue lines represent R_{int} equal to 6, 10, and 20 $\text{k}\Omega/\mu\text{m}$, respectively. The dependence on gate voltage is shown by dashed ($V_{\text{ov}} = 10$ V) and solid ($V_{\text{ov}} = 30$ V) lines (Color figure online)



current flows through all the interlayer resistances to access the bottom layers. As a result, we observe a stronger dependence of total resistance on magnitude of R_{int} for $\lambda = 1$ nm.

Figure 3 also shows that the device resistance exhibits dependence on gate voltages (V_{ov} of 10 and 30 V are represented by dashed and solid lines, respectively), which is strongest for $\lambda = 13$ nm and weakest for $\lambda = 1$ nm. The total resistance can be interpreted as the sum of channel (layer) resistance and contact resistance (including R_c and the effect of interlayer resistances), $R = R_0 L + R_{\text{contact}}$, where R_0 is the channel resistance per unit length. Thus, the slope of the R versus L lines would represent R_0 , whereas R_{contact} is represented by the y-intercept. We can see that channel resistance reduces drastically with increasing gate voltage, which is

due to the increased carrier densities in all layers. On the other hand, negligible variation in R_{contact} due to gate voltage implies that the dependence of the total resistance on gate voltage stems from layer resistance.

6 Layer-dependent TBC and the effect of encapsulation

The TBC derived in “Methodology” section emphasized the important role of the overlap between vibrational density of states (vDOS), atomic masses of either material that comprise the interface, and the vdW spring coupling constant K_{sub} . Figure 4a shows the ZA branch vDOS of single-layer

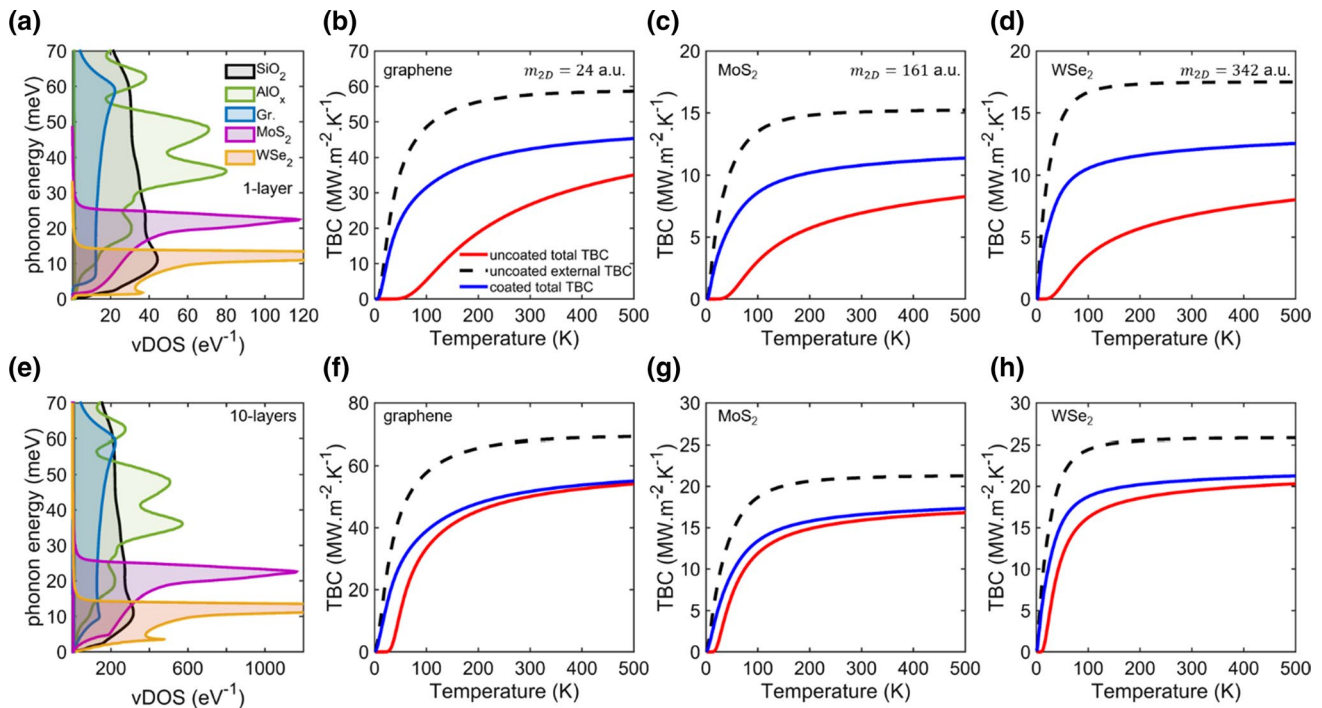


Fig. 4 Vibrational density of states (vDOS) is shown for single-layer graphene, MoS_2 , WSe_2 , amorphous SiO_2 , and amorphous AlO_x is shown in **a**. The temperature-dependent uncoated external TBC (dashed black), uncoated total TBC (solid red), and AlO_x -coated total TBC (solid blue) is shown for single-layer graphene, MoS_2 , and

WSe_2 on SiO_2 is shown in **b**, **c**, and **d**, respectively. **e–h** show the analogous vDOS and temperature-dependent TBC for corresponding uncoated and AlO_x -coated 10-layer stacks on SiO_2 . The vDOS of SiO_2 and AlO_x in panel (e) are scaled up for plotting purposes (Color figure online)

graphene (blue), MoS₂ (purple), and WSe₂ (orange) alongside the vDOS of amorphous SiO₂ (black) and amorphous AlO_x (green). From graphene to WSe₂, we see a reduction in the ZA phonon bandwidth corresponding to a flattening of the ZA branch. Flatter ZA branches are favorable for TBC due to the $1/\omega^2$ dependence of Γ_{sub} ; however, the benefits from a flatter ZA branch can be counterbalanced by heavier 2D layer atoms that decrease Γ_{sub} [40]. The external TBC—that is $G_{\text{ext}}(T) = \lim_{\Gamma_{\text{int}} \rightarrow \infty} G(T) \propto \Gamma_{\text{sub}}$ —depends quadratically on the vdW coupling constant K_{sub} which is proportional to the adhesion energy between the 2D material and substrate [41]. Here, we assume a constant vdW spring coupling constant of $K_{\text{sub}} = 2.7$ N/m for all interfaces and focus on the properties of the materials that comprise the interface rather than on the interface quality itself, which may be highly sensitive to the methods of fabrication [42]. Figure 4b–d shows the temperature-dependent total uncoated TBC (solid red), uncoated external TBC (dashed black), and total AlO_x-coated TBC (solid blue) for single-layer graphene, MoS₂, and WSe₂ on amorphous SiO₂. We can see the competition between the heavier mass of MoS₂ and WSe₂ and their correspondingly flatter ZA branch vDOS's, where, in comparison with graphene, both TMDCs have smaller TBCs despite having narrower ZA phonon bandwidths. The uncoated total TBC shows a strong temperature dependence indicating that internal scattering, which is linear with temperature, has a dominant role. Weak internal scattering in the uncoated stacks leads to a 52.9%, 53.6%, and 60.7% reduction in the total TBC (red line) for graphene (b), MoS₂ (c), and WSe₂ (d), respectively. However, upon encapsulation approximately 26.67%, 25.36%, and 29.89% of these losses are regained in the AlO_x-coated graphene (f), MoS₂ (g), and WSe₂ (h) samples due to an increase in internal scattering.

Figure 4e shows the vDOS of 10-layer graphene (blue), MoS₂ (purple), and WSe₂ (orange) alongside the vDOS of amorphous SiO₂ (black) and amorphous AlO_x (green). The vDOS of the 2D FL stacks is summed across each branch to show the total vDOS. Figure 4f–h shows the uncoated and coated TBC of 10-layer graphene, MoS₂, and WSe₂. The ZA branch from each additional 2D layer in the few-layer stack all contributes to the total TBC, although layers farther from the substrate contribute less as dictated by $\Gamma_{i,\text{sub}}^{\text{FL}}$. Similar to the encapsulating layer in the single-layer interfaces, the additional 2D layers in the FL stack help reduce the temperature dependence of the uncoated samples which is most pronounced at temperature below 200 K. Further, we see that encapsulation has a minimal overall effect on the TBC since the additional layers on top of any i th layer act as an encapsulation layer and insulate layers below them from the AlO_x-coated layer. We see a reduction of 26%, 24.29%, and 24.08% in the uncoated total TBC from the uncoated external TBC of graphene, MoS₂, and WSe₂, respectively, due to internal resistance. And due to the isolation of the

AlO_x-coated layer by the additional layers, we only regain 2.3%, 3.27%, and 4.9% in the AlO_x-coated total TBC for graphene, MoS₂, and WSe₂ upon encapsulation. The robustness of the TBC for uncoated 10-layer stacks is promising for optoelectronic applications where an encapsulating layer may not be present.

Figure 5 shows the room-temperature thickness dependence of the total TBC (solid black) for uncoated and AlO_x-coated graphene (a, b), MoS₂ (c, d), and WSe₂ (e, f) on the left-hand side axis. The right-hand side axis shows the percent contribution *per layer, per stack* starting with one layer in the top left and increasing in thickness moving from left to right. The topmost line of blue circles represents the first layer closest to the substrate in each FL stack. We can see the percent contribution from each layer reduces monotonically as the layer moves farther from the substrate. Layer 1 ($i = 1$) represents the layer directly above the substrate closest to the gate. For most FL stacks with more than 6 layers, the first three layers contribute the bulk majority to the TBC as indicated by their percent contributions being larger than 10%. For 40-layer stacks, the first three layers for graphene, MoS₂, and WSe₂ interfaces make up 66%, 54%, and 52% of the total effective TBC. Figure 5b, d, f illustrates the effect of the AlO_x-coated layer for FL stacks with less than 10 layers, where we observe a modest increase in the TBC of 58.8%, 55.39%, and 77.6% for graphene, MoS₂, and WSe₂, respectively. For FL stacks with more than 10 layers, the total TBC begins to plateau as the added TBC contributions from additional layers begin to diminish. Further, the AlO_x layer has a negligible effect on the total TBC for stacks with more than 20 layers as the coating layer is sufficiently isolated from the layer closest to the substrate by the additional 2D layers in the FL stack.

7 Effect of Joule heating on device resistance

In this section, we study the effect of Joule heating on device resistance by increasing the drain–source voltage V_{DS} to be 20 V. Figure 6(a) shows the thickness dependence of the resistance in devices made up of materials with different screening lengths—13 nm (solid lines), 7 nm (dashed lines), and 1 nm (dotted lines). At V_{ov} equals to 10 V (yellow lines), unlike at low field ($V_{\text{DS}} = 1$ V, Fig. 2), the resistance does not exhibit an optimum thickness for a material with larger λ ($= 13$ nm); we found that the resistance keeps decreasing with increasing thickness up to 40 layers. On the other hand, similar to the low-field thickness-dependent behavior the material with smaller λ ($= 1$ nm) exhibits a minimum resistance at around 5 layers. Similarly, for $\lambda = 7$ nm, a 29-layer-thick device exhibits minimum resistance. A material with $\lambda = 7$ nm exhibits an interesting gate-dependent optimum

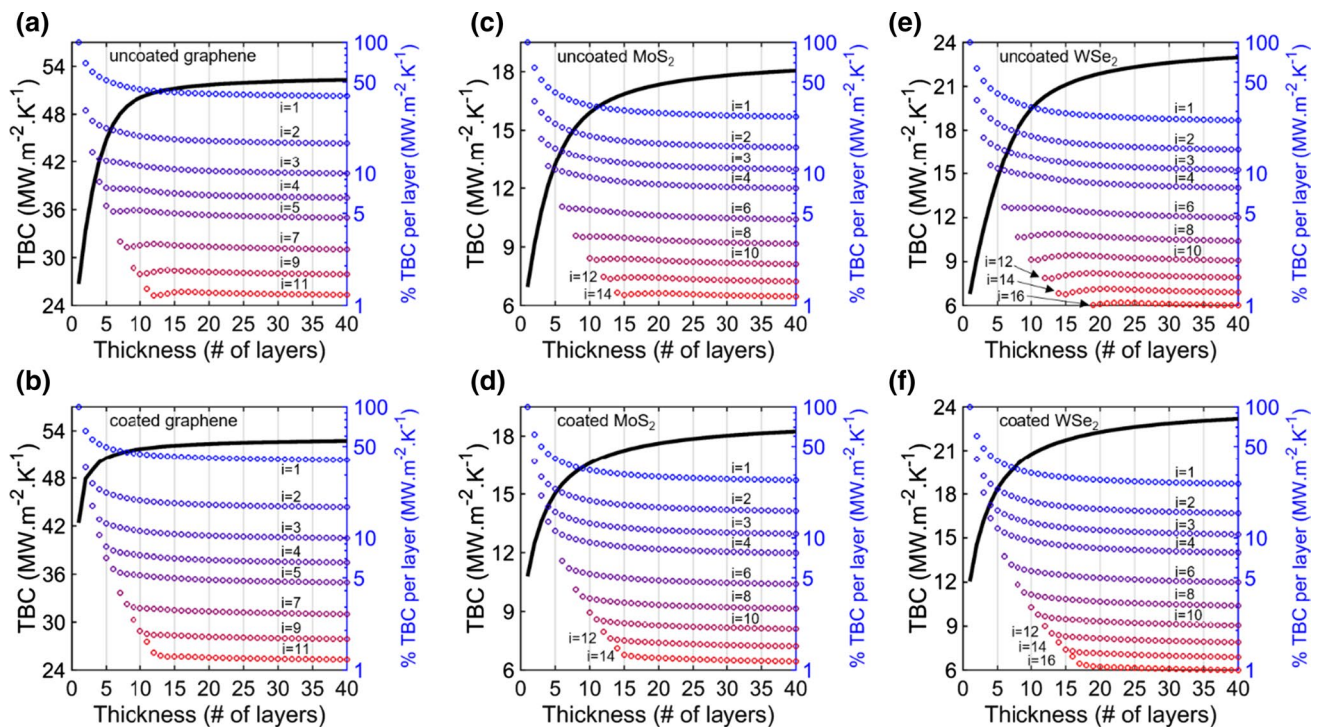


Fig. 5 Thickness-dependent thermal boundary conductance at the room temperature for uncoated (a, c, e) and AlO_x -coated (b, d, f) graphene, MoS_2 , and WSe_2 on SiO_2 is shown on the left-hand side axes. The per layer, per stack percent contribution to the TBC is shown by the blue and red circles and correspond to the right-hand

side axes. The labels for the circles correspond to the i th-layer in the corresponding FL structure. Layer ($i = 1$) represents the layer directly above the substrate closest to the gate. As i increases, the layers move further from the gate and closer to the S/D contacts and encapsulating layer (Color figure online)

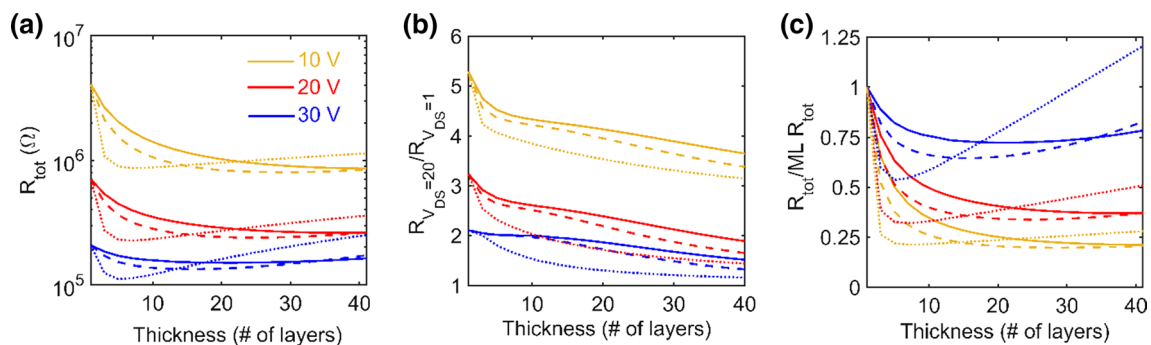


Fig. 6 Effect of self-heating on device resistances. **a** shows the thickness dependence of device resistance for different λ —13 nm (solid lines), 7 nm (dashed lines), and 1 nm (dotted lines) at $V_{\text{DS}} = 20$ V. Yellow, red, and blue colors represent different gate voltages V_{ov}

equal to 10, 20, and 30 V, respectively. **b** shows the ratio of the device resistances at $V_{\text{DS}} = 20$ V and $V_{\text{DS}} = 1$ V versus thickness. **c** shows the thickness dependence of the device resistance normalized by the resistance of single layer at $V_{\text{DS}} = 20$ V (Color figure online)

number of layers. We observed that the optimum number of layers for different λ decreases with increasing gate voltages—25 and 19 layers for $V_{\text{ov}} = 20$ (red lines) and 30 V (blue lines), respectively. For $\lambda = 1$ nm, the optimum number of layers were independent of gate voltage.

Due to Joule heating at high $V_{\text{DS}} (= 20$ V), the device resistances increase as compared to their low-field values ($V_{\text{DS}} = 1$ V) for all V_{ov} . We plot the ratio between the

resistances at $V_{\text{DS}} = 20$ V and $V_{\text{DS}} = 1$ V against thickness of the 2D stack for different gate voltages and screening lengths in Fig. 6b. We found that the effect of self-heating is maximum in single-layer device where the ratio is the highest. The resistances increased by more than 500, 300, and 200% for V_{ov} equal to 10, 20, and 30 V, respectively. The resistance does not increase significantly due to self-heating when a thicker stack of 2D material is used, especially at large gate

voltages. The resistance increases by 50% for $\lambda = 13$ nm and by less than 12% for $\lambda = 1$ nm at $V_{ov} = 30$ V. We also found that for a given thickness and gate voltage, the material with the largest λ ($= 13$ nm) exhibits highest increase in resistance due to self-heating.

In Fig. 6c, we show the maximum percentage by which the resistance of a device can be decreased by increasing thickness for different λ when the device is self-heating ($V_{DS} = 20$ V). Our results show that among materials with different λ , the least resistance can be achieved by increasing thickness in the material with smallest λ . The device resistance decreases to 22% when the number of layers is increased from 1 to 5 in a material with $\lambda = 1$ nm for a gate voltage of $V_{ov} = 10$ V. The effect of increasing thickness on resistance decreases with increasing gate voltage. For $V_{ov} = 30$ V, the resistance of the 5-layer-thick device is 53% of the resistance of the single-layer device for $\lambda = 1$ nm. For materials with larger λ , one can achieve such small resistances as exhibited by materials with $\lambda = 1$ nm at much thicker stacks, as shown in Fig. 6c.

8 Conclusions

We have used our self-consistent electrothermal model to study the conductance of FL 2D devices and found that it improves with increasing thickness (number of layers) at small gate voltages, but exhibits a peak for large gate voltages. The width of the peak, representing the most “active” layers in the stack, shows a strong dependence on the screening length of the material—active layers are in the bottom of the FL stack for small λ , whereas they are more spread out for larger λ . At small V_{ov} , the resistance network representing 2D stack approaches parallel resistors with zero interlayer resistance, whereas at large V_{ov} interlayer resistance limits the conductance of a thick device. Consequently, representation of the total resistance by two series resistors, channel and contact resistors, works well for long devices and can be effectively captured by a transfer length model. However, for smaller devices, TLM fails and the complete resistance network model must be used. In general, TLM only holds when interlayer resistance is much smaller than the layer resistances.

The thermal boundary conductance of uncoated single-layer 2D materials is largely suppressed and exhibits a strong temperature dependence caused by internal scattering. However, additional layers in FL stacks insulate the bottommost layers and add additional channels of phonon transport to the substrate leading to an increasing TBC with increasing FL thickness. The TBC increases sharply from single-layer reaching 90% of its maximum near thicknesses of 6 to 7 layers. The compound benefits from increased mobility and increased TBC with modest increases in FL

thickness are promising for the future implementation of FL 2D-based devices. Further, the robust TBC of FL 2D stacks without encapsulation is promising in optical applications where an encapsulating layer may not be present. At large source–drain voltages, there is significant Joule heating and temperature rise, especially in the layers furthest from the substrate. Our results show that the device conductance deteriorates the least due to self-heating in materials with small λ . Materials with large λ do not exhibit any optimum number of layers, whereas for small λ the active layers are confined to bottom few layers, similar to the behavior observed at small V_{DS} . During self-heating, the device resistance could be reduced to 22% of the monolayer resistance when the number of layers is increased to 5 for $\lambda = 1$ nm. Careful modeling of both electronic and thermal transport is necessary to optimize FL 2D devices and minimize self-heating. Further research into the factors that affect the coupling between the bottom layer and the substrate is needed, and a path forward may be via computationally optimizing heterostructured FL stacks that exhibit a favorable combination of TBC, screening, and mobility.

References

1. Castro Neto, A.H., Guinea, F., Peres, N.M.R., Novoselov, K.S., Geim, A.K.: The electronic properties of graphene. *Rev. Mod. Phys.* **81**(1), 109–162 (2009)
2. Novoselov, K.S., Jiang, D., Schedin, F., Booth, T.J., Khotkevich, V.V., Morozov, S.V., Geim, A.K.: Two-dimensional atomic crystals. *Proc. Natl. Acad. Sci. USA* **102**(30), 10451–10453 (2005)
3. Geim, A.K., Grigorieva, I.V.: Van der Waals heterostructures. *Nature* **499**, 419 (2013)
4. Das Sarma, S., Adam, S., Hwang, E.H., Rossi, E.: Electronic transport in two-dimensional graphene. *Rev. Mod. Phys.* **83**(2), 407–470 (2011)
5. Wang, Q.H., Kalantar-Zadeh, K., Kis, A., Coleman, J.N., Strano, M.S.: Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. *Nat. Nanotechnol.* **7**(11), 699–712 (2012)
6. Jariwala, D., Sangwan, V.K., Lauhon, L.J., Marks, T.J., Hersam, M.C.: Emerging device applications for semiconducting two-dimensional transition metal dichalcogenides. *ACS Nano* **8**(2), 1102–1120 (2014)
7. Suryavanshi, S.V., Pop, E.: S2ds: Physics-based compact model for circuit simulation of two-dimensional semiconductor devices including non-idealities. *J. Appl. Phys.* **120**, 224503 (2016)
8. Sui, Y., Appenzeller, J.: Screening and interlayer coupling in multilayer graphene field-effect transistors. *Nano Lett.* **9**(8), 2973–2977 (2009)
9. Das, S., Appenzeller, J.: Where does the current flow in two-dimensional layered systems? *Nano Lett.* **13**, 3396–3402 (2013)
10. Das, S., Chen, H.-Y., Penumatcha, A.V., Appenzeller, J.: High performance multilayer mos2 transistors with scandium contacts. *Nano Lett.* **13**(1), 100–105 (2013)
11. Behranginia, A., Hemmat, Z., Majee, A.K., Foss, C.J., Yasaei, P., Aksamija, Z., Salehi-Khojin, A.: Power dissipation of WSe₂

- field-effect transistors probed by low-frequency Raman thermometry. *ACS Appl. Mater. Interfaces* **10**(29), 24892–24898 (2018)
12. Li, M., Zhang, J., Xuejiao, Hu, Yue, Y.: Thermal transport across graphene/sic interface: effects of atomic bond and crystallinity of substrate. *Appl. Phys. A* **119**(2), 415–424 (2015)
 13. Schroeder, D.P., Aksamija, Z., Rath, A., Voyles, P.M., Lagally, M.G., Eriksson, M.A.: Thermal resistance of transferred-silicon-nanomembrane interfaces. *Phys. Rev. Lett.* **115**, 256101 (2015)
 14. Ong, Z.-Y., Qiu, Bo, Shanglong, Xu, Ruan, X., Pop, E.: Flexural resonance mechanism of thermal transport across graphene-SiO₂ interfaces. *J. Appl. Phys.* **123**(11), 115107 (2018)
 15. Ong, Z.-Y.: Thickness-dependent kapitza resistance in multilayered graphene and other two-dimensional crystals. *Phys. Rev. B* **95**, 155309 (2017)
 16. Majee, A.K., Hemmat, Z., Foss, C.J., Salehi-Khojin, A., Aksamija, Z.: Current rerouting improves heat removal in few-layer wse₂ devices. *ACS Appl. Mater. Interfaces* **12**(12), 14323–14330 (2020)
 17. Bolotin, K.I., Sikes, K.J., Jiang, Z., Klima, M., Fudenberg, G., Hone, J., Kim, P., Stormer, H.L.: Ultrahigh electron mobility in suspended graphene. *Solid State Comm.* **146**(9), 351–355 (2008)
 18. Ong, Z.-Y., Fischetti, M.V.: Mobility enhancement and temperature dependence in top-gated single-layer MoS₂. *Phys. Rev. B* **88**, 165316 (2013)
 19. Bao, W., Cai, X., Kim, D., Sridhara, K., Fuhrer, M.S.: High mobility ambipolar MoS₂ field-effect transistors: substrate and dielectric effects. *Appl. Phys. Lett.* **102**, 042104 (2013)
 20. Ma, N., Jena, D.: Charge scattering and mobility in atomically thin semiconductors. *PRX* **4**, 011043 (2014)
 21. Zhihao, Yu, Ong, Z.-Y., Li, S., Jian-Bin, Xu, Zhang, G., Zhang, Y.-W., Shi, Yi, Wang, X.: Analyzing the carrier mobility in transition-metal dichalcogenide MoS₂ field-effect transistors. *Adv. Func. Mater.* **27**(19), 1604093 (2017)
 22. Ghatak, S., Pal, A.N., Ghosh, A.: Nature of electronic states in atomically thin mos₂ field-effect transistors. *ACS Nano* **5**(10), 7707–7712 (2011)
 23. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V., Kis, A.: Single-layer MoS₂ transistors. *Nat. Nanotechnol.* **6**(3), 147–150 (2011)
 24. Cui, X., Lee, G.-H., Kim, Y.D., Arefe, G., Huang, P.Y., Lee, C.-H., Chenet, D.A., Zhang, X., Wang, L., Ye, F., Pizzocchero, F., Jessen, B.S., Watanabe, K., Taniguchi, T., Muller, D.A., Low, T., Kim, P., Hone, J.: Multi-terminal transport measurements of MoS₂ using a van der Waals heterostructure device platform. *Nat. Nanotechnol.* **10**, 534 (2015)
 25. Lee, G.-H., Yu, Y.-J., Cui, X., Petrone, N., Lee, C.-H., Choi, M.S., Lee, D.-Y., Lee, C., Yoo, W.J., Watanabe, K., Taniguchi, T., Nuckolls, C., Kim, P., Hone, J.: Flexible and transparent MoS₂ field-effect transistors on hexagonal boron nitride-graphene heterostructures. *ACS Nano* **7**(9), 7931–7936 (2013)
 26. Zheng, J., Yan, X., Zhixing, Lu, Qiu, H., Guanchen, Xu, Zhou, Xu, Wang, P., Pan, X., Liu, K., Jiao, L.: High-mobility multilayered mos₂ flakes with low contact resistance grown by chemical vapor deposition. *Adv. Mater.* **29**(13), 1604540 (2017)
 27. Pradhan, N.R., Rhodes, D., Memaran, S., Poumirol, J.M., Smirnov, D., Talapatra, S., Feng, S., Perea-Lopez, N., Elias, A.L., Terrones, M., Ajayan, P.M., Balicas, L.: Hall and field-effect mobilities in few layered p-wse₂ field-effect transistors. *Sci. Rep.* **5**, 8979 (2015)
 28. Chang, H.-Y., Zhu, W., Akinwande, D.: On the mobility and contact resistance evaluation for transistors based on mos₂ or two-dimensional semiconducting atomic crystals. *Appl. Phys. Lett.* **104**, 113504 (2014)
 29. Na, J., Shin, M., Joo, M.-K., Huh, J., Kim, Y.J., Choi, H.J., Shim, J.H., Kim, G.-T.: Separation of interlayer resistance in multilayer mos₂ field-effect transistors. *Appl. Phys. Lett.* **104**, 233502 (2014)
 30. Xu, S., Wu, Z., Lu, H., Han, Y., Long, G., Chen, X., Han, T., Ye, W., Wu, Y., Lin, J., Shen, J., Cai, Y., He, Y., Zhang, F., Lortz, R., Cheng, C., Wang, N.: Universal low-temperature ohmic contacts for quantum transport in transition metal dichalcogenides. *2D Mater.* **3**, 021007 (2016)
 31. Behranginia, A., Yasaei, P., Majee, A.K., Sangwan, V.K., Long, F., Foss, C.J., Foroozan, T., Fuladi, S., Hantehzadeh, M.R., Shahbazian-Yassar, R., Hersam, M.C., Aksamija, Z., Salehi-Khojin, A.: Direct growth of high mobility and low-noise lateral MoS₂-graphene heterostructure electronics. *Small* **13**, 1604301 (2017)
 32. Persson, B.N.J., Ueba, H.: Heat transfer between weakly coupled systems: Graphene on a-SiO₂. *Europhys. Lett.* **91**, 56001 (2010)
 33. Persson, B.N.J., Ueba, H.: Heat transfer between graphene and amorphous SiO₂. *J. Phys. Condens. Matter* **22**(46), 462201 (2010)
 34. Ong, Z.-Y., Cai, Y., Zhang, G.: Theory of substrate-directed heat dissipation for single-layer graphene and other two-dimensional crystals. *Phys. Rev. B* **94**, 165427 (2016)
 35. Correa, G.C., Foss, C.J., Aksamija, Z.: Interface thermal conductance of van der Waals monolayers on amorphous substrates. *Nanotechnology* **28**(13), 135402 (2017)
 36. Yasaei, P., Hemmat, Z., Foss, C.J., Li, S.J., Hong, L., Behranginia, A., Majidi, L., Klie, R.F., Barsoum, M.W., Aksamija, Z., Salehi-Khojin, A.: Enhanced thermal boundary conductance in few-layer Ti₃C₂ MXene with encapsulation. *Adv. Mater.* **30**, 1801629 (2018)
 37. Majee, A.K., Aksamija, Z.: Length divergence of the lattice thermal conductivity in suspended graphene nanoribbons. *Phys. Rev. B* **93**, 235423 (2016)
 38. Seol, J.H., Jo, I., Moore, A.L., Lindsay, L., Aitken, Z.H., Pettes, M.T., Li, X., Yao, Z., Huang, R., Broido, D., Mingo, N., Ruoff, R.S., Shi, L.: Two-dimensional phonon transport in supported graphene. *Science* **328**(5975), 213–216 (2010)
 39. Morelli, D.T., Heremans, J.P., Slack, G.A.: Estimation of the isotope effect on the lattice thermal conductivity of group IV and group III–V semiconductors. *Phys. Rev. B* **66**(19), 195304 (2002)
 40. Foss, C.J., Aksamija, Z.: Quantifying thermal boundary conductance of 2D–3D interfaces. *2DM* **6**(2), 025019 (2019)
 41. Prasher, R.: Acoustic mismatch model for thermal contact resistance of van der Waals contacts. *Appl. Phys. Lett.* **94**(4), 041905 (2009)
 42. Yasaei, P., Foss, C.J., Karis, K., Behranginia, A., El-Ghandour, A., Fathizadeh, A., Majee, A.K., Foster, C., Khalili-Araghi, F., Aksamija, Z., Salehi-Khojin, A.: Interfacial thermal transport in monolayer graphene- and MoS₂-based devices. *Adv. Mater. Interfaces* **4**, 1700334 (2017)