Innovative Propagation Mechanism for Inter-chip and Intra-chip Communication

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***Abstract*—SoC (System on chip) technology has rapidly developed in recent years, stimulating emerging research areas such as investigating the efficacy of wireless network interconnection within a single chip or between multiple chips. However the design of the on-chip antenna faces the challenge of obtaining high radiation efficiency and transmission gain due to conductive loss of the silicon substrate. A new on-chip propagation mechanism of radio waves, which takes advantage of the un-doped silicon layer, is developed in order to overcome this challenge. It was found that by properly designing the dimension of silicon wafer, the un-doped silicon layer is able to act like a waveguide. Most of the energy is directed to the approximately lossless the un-doped silicon layer of high resistivity instead of attenuating in the doped silicon substrate or radiating to the air. HFSS modeling and simulation results are provided to show that efficiency, gain and directivity of the on-chip antenna are greatly improved. In addition, this type of antennas can be easily reconfigured, which as a result, makes wireless SoCs with wireless interconnects or even a wireless network on PCB (Printed Circuit Board) possible.**

I. INTRODUCTION

Traditional wire-based interconnects have been the bottlenecks of power and timing performance for CMOS-based electronic devices. To address this problem, inter-chip (chip-to-chip) and intra-chip (on-chip) wireless interconnections using microwave or millimeter wave are being evaluated. Kim and K.K.O. studied the feasibility of integrating the antennas in ICs and demonstrated that wireless communication within silicon ICs is possible [1]. They claimed that the Bottom Layer (BL) or a guidance medium can be optimized in conjunction with integrated antennas to improve the system performance [2]. However, due to low resistivity (typically 10-20 Ω-cm) of the silicon substrate, the radiation efficiency and transmission gain of the integrated on-chip antenna was very low. The efficiency and gain were approximately 3% and -40 dB respectively at relatively low frequency (15 GHz) at 5 mm distance when standard 10-cm resistivity silicon substrate was used. Although the paper presents a novel method using high dielectric material, specifically using diamond for the BL on which silicon chips are mounted [3] [4], it can face huge resistance from conventional CMOS process because of cost and complexity of altering the current process. In this paper, a new propagation mechanism for on-chip wireless communication is proposed. It has been shown to improve radiation efficiency and increase transmission gain by adding a ground plane between silicon substrates and the un-doped silicon layer, while removing the ground plane under antenna area. While doing so, the un-doped silicon layer acts as a wave guide that provides the main path for electromagnetic (EM) waves. At the same time, the ground plane between the un-doped silicon layer and silicon substrate prevents the wave from leaking to the silicon substrates. This paper also studies the placement position of antenna pairs in order to achieve highest gain. It is found that these antennas pairs can be reconfigured to operate at different frequencies. Section II introduces the simulation model using HFSS; in Section III, simulation results are shown.

II. HFSS MODEL FOR SIMULATION

Both antennas for transmitting and receiving signals are modeled on Si substrates. Conventional stack structure of the CMOS process is shown in Fig. 1.

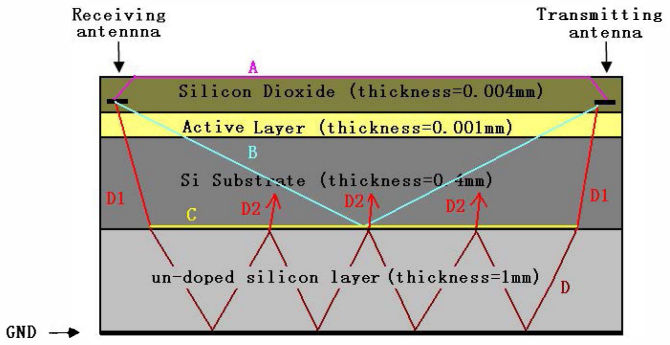

Fig. 1: Possible ray path for on-chip antenna pair

Antennas are inside the silicon dioxide (SiO2) layer which is 4 μm on top of the wafer. A highly doped active layer with conductivity as high as 800 Siemens/m is well below the SiO2 layer, followed by slightly doped Si substrates with the conductivity of 10 Siemens/m and then an un-doped silicon layer.

Four primary ray paths labeled A, B, C and D, that the signal can take when traversing between the transmitter and receiver are drawn in Fig. 1 and analyzed similar to that in [2]. Ray path A is the surface wave path through the interface of air and Si substrate. B is the wave propagating and attenuating in the Si substrate. C is the surface wave path along the interface of Si substrate and BL. D is the guided wave in the BL. Some of the energy is leaking to the Si substrate from the BL and then is attenuated as shown on D2 path; some of the energy is being attenuated before entering BL (D1 path). As a result radiation efficiency is very low, though D is the

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dominant propagating path. By thinning the silicon substrate from 260um to 10um, S21 and radiation efficiency will be improved, respectively, from -30.3 dB to -18.4 dB and from 2.8% to 22.5% [3]. However the Si substrate would be too thin to be practically used. In order to overcome this problem, a metallic layer (ground plane) between Si substrate and BL is added. The metal under the antenna area is removed in order to direct the wave down to BL without reflection. The bottom layer does not have to be high dielectric material, so conventional CMOS processes can still be used.

Fig. 2 shows the stack structure and dominant ray path of this new technology. The bottom layer with two metallic layers on the top and bottom acts like half metallic wave guide (vertical direction) and half dielectric wave guide (transverse direction). The relative dielectric constant (εr) used for both Si substrate and BL is 11.9. In order to avoid attenuation at path D1, doped silicon substrate as well as P-well layer under the antenna area is replaced by un-doped Silicon.

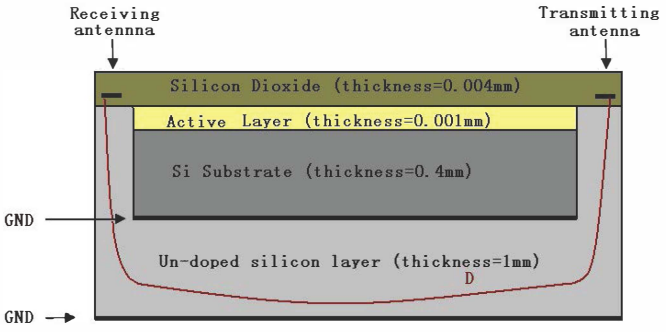

Fig. 2: Dominant ray path after inserting a ground layer between Si substrate and un-doped silicon layer

III. Simulation Results

Fig. 3 shows that the optimized antenna length is around 1mm at an operating frequency (f0) around 60 GHz for the best reflection coefficient (S11). A half wavelength dipole antenna is used, where the wavelength can be determined with Eq. 1, where the value of effective dielectric constant (ε_eff) is between dielectric constant of silicon dioxide (ε_SiO2=4.3) and dielectric constant of silicon (ε_Si=11.9).

$$\lambda_g = \frac{c}{\sqrt{|\varepsilon_{eff}|}} \tag{1}$$

Fig. 4 shows the magnitude of the electric field distribution inside the silicon substrate as well as inside the un-doped silicon layer. The strength of the electric field inside the un-doped silicon layer (orange) is much stronger than that inside the silicon substrate (green) and in the air (green). The un-doped silicon layer acting as a waveguide provides a nearly zero conductive loss path due to nearly zero conductivity with only a little dielectric loss. Therefore, the transmission coefficient (S21) is greatly improved as shown on Fig. 5.

Without the un-doped silicon substrate under the antenna area, the transmission coefficient can reach -30 dB; while with

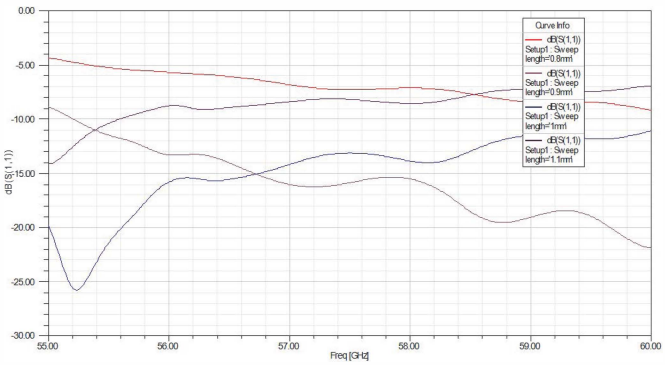

Fig. 3: Reflection coefficient (S11) versus frequency and length of antennas when un-doped Si takes place of lossy Si substrate under the antenna area

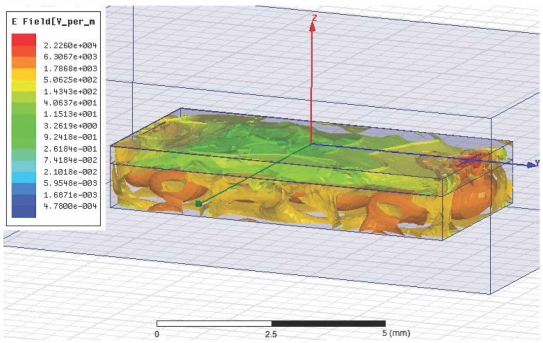

Fig. 4: Magnitude of electric field distribution inside the silicon substrate and un-doped silicon layer

the un-doped silicon under the antenna area, it can increase by 15 dB and reach -15 dB with the radiation efficiency of 28.78% compared with 3.6% with doped silicon. Because the relative dielectric constant of silicon (ε_(r,Si)) is much larger than that of the air, the un-doped silicon layer can be approximated to be perfect electric conductors [5] [7]. The lowest resonant frequency of the geometry for a given mode illustrated in Fig. 2 is given by Eq. 2, where a=4 mm, b=1 mm, ε_(r,Si)=11.9.

$$f_{cutoff,mn} = \frac{c}{2\pi\sqrt{\varepsilon_{r,Si}}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \tag{2}$$

There are nine modes with their cutoff frequencies below 62 GHz. Therefore, for an antenna pair operating at around 60 GHz, the EM wave propagating in the Si waveguide contains several modes, each of which has its own field distribution. The antenna pairs can only get highest S21 while they are placed where the EM field has the highest strength, right below the receiving antenna as shown in Fig. 7 (a). It is found that the first antenna pair has its S21 peak at 57.8 GHz while the second antenna pair has its S21 minimum value; when the second antenna pair reach the S21 peak at 58.9 GHz, the first antenna pair sees the minimum value. The isolation between the two antenna pairs is 20 dB. Thus different communication

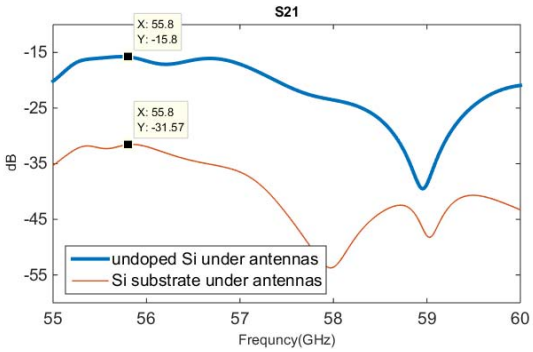

Fig. 5: Transmission coefficient (S21) when Si substrate is not replaced by un-doped Si (red); Transmission coefficient (S21) when Si substrate is replaced by un-doped Si (blue)

channels can be used for different antenna pairs. Receiving antennas placed on the Y axis demonstrate similar behavior as shown on Fig. 7 (b).

The last improvement is the directivity for chip-to-chip communication. The simulations show that due to the un-doped silicon layer waveguide, the EM wave radiates to the air if the field strength can reach the maximum value at the chip edge at a certain frequency.

Fig. 8 (a) shows the top view of the radiation pattern of the transmitting antenna. It was found that the directivity is nearly 6 dB along -Y direction at 57 GHz, while at other frequencies directivity may not be good (-2.6 dB) (Fig. 8 (b)). It is possible to take advantage of that phenomenon by assigning several channels for the purpose of chip-to-chip communication.

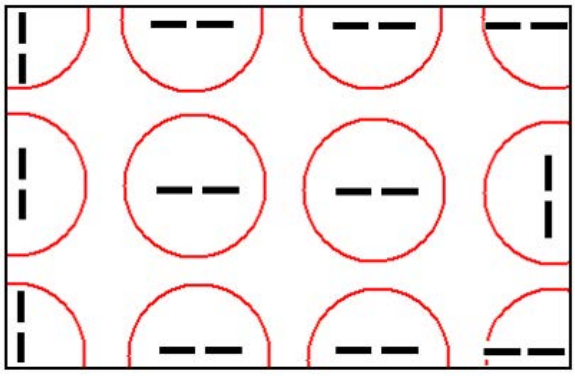

Fig. 6: Demonstration of antenna placement. Centers of the red circles have the highest EM field strength. Black bars are antennas. It does not matter if the antennas are placed vertically or horizontally

IV. Conclusions

The transmission gain and radiation efficiency of silicon on-chip antenna was improved by inserting a ground plane between the silicon substrate and un-doped silicon layer base on conventional CMOS process while removing the ground

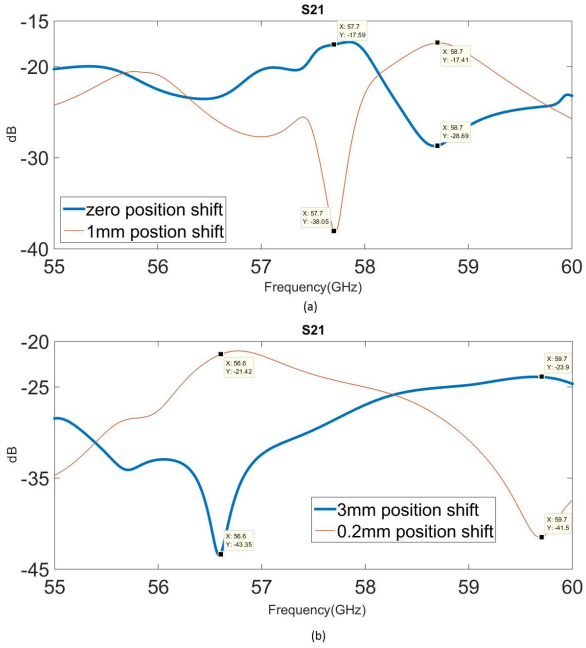

Fig. 7: (a) S21 v.s. antenna positions shifting along X axis; (b) S21 v.s. antenna positions shifting along Y axis

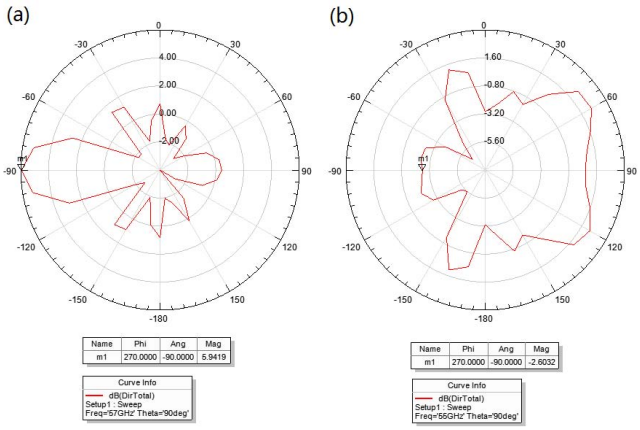

Fig. 8: (a) Top view radiation pattern at 57 GHz; (b) Top view radiation pattern at 55 GHz

plane as well as replacing doped silicon substrate with un-doped silicon under the antenna area. By optimizing the antenna length and chip dimensions, the maximum transmission coefficient (S21) and antenna efficiency can reach -15 dB and 28% respectively. According to the study of distribution characteristics of EM field inside the un-doped silicon layer, we found different channels can be assigned for different antenna pairs on-chip as well as for chip to chip communication. Thus, the technique discussed in this paper can enable new networks on chip.

V. Acknowledgement

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