

Hardware Implementation of Low-overhead Data Aided Timing and Carrier Frequency Offset Correction for OFDM Signals

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Abstract—In this paper a trained timing synchronization method using a matched filter and Carrier Frequency Offset synchronization method based on a modified correlation scheme is implemented in hardware for Orthogonal Frequency Division Multiplexing. MATLAB System Generator is used to target a Virtex-6 FPGA on the ML605 Xilinx evaluation board, with an optimized number of board resources utilized. A complex pseudo-noise sequence is used as a preamble for timing. The employed training sequence for frequency synchronization consists of only one pilot symbol, distinguishing this system from most approaches which rely upon multiple pilot symbols. By reducing the number of symbols required for the training period, it is possible to increase throughput. In addition, to ensure that the system has flexibility and is not protocol specific, the system allows for a variable number of FFT sizes and pilot symbol design parameters to be used. Performance of the system is shown to improve over an Additive White Gaussian Noise channel by implementing the design in comparison to not compensating for the distortion.

Index Terms—Carrier Frequency Offset, Data Aided Synchronization, FPGA Design, Frequency Synchronization, OFDM, Pilot Symbol Design, Timing Synchronization

I. INTRODUCTION

ORTHOGONAL Frequency Division Multiplexing (OFDM) is a multi-carrier transmission scheme that is widely used in wireless technology. Several examples of its use may be found in wireless local area networks such as in IEEE 802.11 a/g/n/ac, WiMAX, and in the down link of Long Term Evolution (LTE). The key advantages of OFDM lie in: *i*) the orthogonality of adjacent sub-carriers which results in OFDM being more spectrally efficient due to guard intervals not being required and *ii*) its resistance to severe channel conditions as described in [1]. Timing synchronization is necessary in OFDM schemes as described in [1] so that the payload of the signal may be recovered properly. Carrier Frequency Offset (CFO) is a common issue that occurs in OFDM systems from practical Radio Frequency (RF) transceivers. A mismatch between the local oscillators of the transmitter and receiver in the system results in a phase rotation of the received signal as discussed in [2]. This is an undesirable trait as information is frequently conveyed through transmission of different phases. Compensation methods are typically classified as data aided or non-data aided synchronization, in which the CFO is estimated either by using a set of training data that

is known to the receiver or through statistical techniques. Synchronization schemes may be considered coarse if the training sequence uses one or more pilot symbols, or fine if training data consists of individual sub-carriers referred to as pilot tones. In this work, a matched filter based timing synchronization and a coarse training based CFO estimation with correction scheme for OFDM signals is implemented on an Virtex-6 FPGA using Xilinx System Generator in MATLAB. Though cross correlators have been previously implemented in hardware, as seen in [3], [4], and in [5] for the purpose of timing synchronization, they lack work and discussion in implementation of frequency synchronization. Previous implementations are based on only one set of training data whereas, in this work, multiple training sequences may be used during detection in parallel to determine which set of training data corresponds to the received signal.

Frequency synchronization has been implemented on an FPGA in [6] using blind methods for fine estimation and implementations of coarse trained estimation have been performed through Xilinx tools in [7] and [8] that are based on correlation difference between multiple pilot symbols. In [9] a coarse trained synchronization method is presented using multiple lag parameters for correlation on multiple pilot symbols while perfect timing recovery is assumed. In previous works, all methods used for coarse trained CFO estimation rely on using multiple pilot symbols for training without the discussion of variable pilot symbol structures. The theory described by [10] is implemented in this paper such that the system requires only a single pilot symbol for CFO estimation with further extension allowing for scaling of pilot symbol design. As a result, there is an increase of throughput as the amount of meaningful data in the payload may be increased in contrast to previous hardware implementations which require multiple training symbols. Both time and frequency synchronizations have been implemented on hardware in [11] based on the work in [12], but this work utilizes multiple pilot symbols. In [13] synchronization is performed in hardware using serial operations while in [14] the synchronization methods were specific to WLAN and no discussion of channel or CFO effects on system performance were provided. The work shown in [11], [13], and [14] offered no scalability in terms of parameters chosen or number of training sequences considered. This paper presents an extension of the work introduced in [15] on the SDC [16] platform including both timing and frequency synchronization along with examining the performance of the

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system using various intrinsic flexible [17] design parameters under different distortion effects.

The structure of this paper is as follows: a theoretical framework of the OFDM signal, CFO effects, timing synchronization and CFO correction will be presented in Section II. A description of the system model will be discussed both for MATLAB script and the System Generator model for synchronization in Section III. Performance results over an Additive White Gaussian Noise (AWGN) channel will be analyzed in Section IV, and concluding remarks will be made in Section V.

II. THEORETICAL FRAMEWORK

A. OFDM Signal

A basic block diagram of a baseband equivalent OFDM signal is shown in Figure 1. A random bit stream was used as an input to a Quadrature Phase Shift Keying (QPSK) mapper, which uses a gray coding scheme to convey information through different transmitted phases. The QPSK symbols are converted to parallel data streams in which each stream corresponds to one sub-carrier. An OFDM symbol is considered a block that is formed that contains all of the sub-carriers used in the parallel streams. An Inverse Fast Fourier Transform (IFFT) is performed along the OFDM symbols to allow for the multi-carrier scheme. For the purposes of this implementation the inclusion of a cyclic prefix was ignored due to the resulting spectral inefficiency and decrease in use described in [18]. A single pilot symbol consisting of complex pseudo-noise samples of length equal to the length of the OFDM symbols is inserted in front of the payload to act as a training sequence for the receiver. The baseband equivalent OFDM signal is generated by then converting the parallel data streams back to serial. An OFDM packet may consist of a preamble, pilot symbols for synchronization and equalization, and a variable number of OFDM symbols for payload. For the purpose of this work, the preamble was selected to be a complex pseudo-noise sequence of length 32 or 64 samples. The pilot symbol structure used for each packet was based on the theory provided in [10] which expanded upon the original framework of [12] to allow for the use of a single pilot symbol. A design parameter L was selected for the number of repetitions of identical complex pseudo-noise sequences within the pilot symbol.

B. Distortion Effects

In this paper the two primary distortion effects for the system considered were CFO and noise.

1) *CFO Effects*: As discussed in Section I, CFO may be attributed to the RF transceiver. A mathematical description of the resulting signal $s[n]$ is shown in

$$x[n] = s[n] \exp\left(\frac{j2\pi v n}{T}\right), \quad 0 \leq n \leq T \quad (1)$$

where $s[n]$ is the OFDM signal, v is the phase offset relative to the sub-carrier spacing, and T is the duration of the OFDM packet in terms of number of samples.

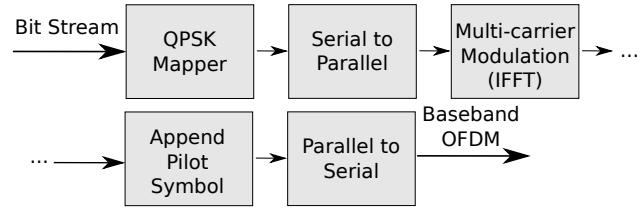


Fig. 1: OFDM Signal Structure used in this work.

2) *AWGN Channel*: For the purpose of this work, an AWGN channel was considered for various levels of Signal to Noise Ratio (SNR). The channel is modeled as a zero mean Gaussian random variable with variable variance. The resulting signal that is used for the system model, $y[n]$, is represented by

$$y[n] = x[n] + z[n] \quad (2)$$

where $z[n]$ is the noise component.

C. Timing Synchronization

The method used in this work consists of an energy detector and a matched filter, with the filter only being activated if a decision is made that a signal is present. The calculation for energy may be shown as

$$E_s = \sum_{n=0}^N |y[n]|^2 \quad (3)$$

where $y[n]$ is the received signal and N is an observation window length. As discussed in [1], a matched filter may be represented as a cross correlator as given by

$$P[n] = \sum_{m=-\infty}^{\infty} y^*[m]h[m+n] \quad (4)$$

where $h[n]$ is the reference signal. Through simplification it may be seen that the real and imaginary components of the cross correlation may be written as

$$\begin{aligned} \text{Re}\{P[n]\} &= P_{II}[n] + P_{QQ}[n] \\ \text{Im}\{P[n]\} &= P_{QI}[n] - P_{IQ}[n] \end{aligned} \quad (5)$$

where $P_{II}[n]$ is the cross correlation of the real component of the received signal and the real component of the reference signal, $P_{QQ}[n]$ is the cross correlation of the imaginary component of the received signal and the imaginary component of the reference signal, $P_{QI}[n]$ is the cross correlation of the imaginary component of the received signal and the real component of the reference signal, and $P_{IQ}[n]$ is the cross correlation of the real component of the received signal and the imaginary component of the reference signal. For the purpose of hardware implementation, it is necessary to separate the computation into real and imaginary components.

D. CFO Estimation Algorithm

The method proposed in [10] used the modified correlation calculation shown in

$$R[m] = \frac{1}{N - mM} \sum_{k=mM}^{N-1} x[k]h^*[k - mM], \quad 0 \leq m \leq H \quad (6)$$

where $y[k]$ is the signal from (2) at time index k , h is the training data, M is a constant equal to the ratio of the OFDM FFT size and the design parameter L , and H was a design parameter selected to be half of the value of L per the results found in [19]. For the purpose of hardware implementation, it is necessary to maintain the result in (6) as separate in-phase and quadrature phase components shown by

$$R[m] = \frac{1}{N - mM} (R_I[m] + jR_Q[m]) \quad (7)$$

where $R_I[m]$ and $R_Q[m]$ are the real and imaginary components of (6), respectively. The real component is:

$$R_I[m] = r_{II}[m] + r_{QO}[m] \quad (8)$$

where $r_{II}[m]$ is the correlation between the in-phase components of both the received samples and training data, and $r_{QO}[m]$ is the correlation between the quadrature phase components of the received samples and training data. Similarly the imaginary component of (7) is:

$$R_Q[m] = r_{QI}[m] - r_{IQ}[m] \quad (9)$$

where $r_{QI}[m]$ is the correlation of the quadrature phase received samples and in-phase training data, and $r_{IQ}[m]$ is the correlation between the in-phase received samples and quadrature phase training data. The phase differences of adjacent correlation samples from (7) are calculated in

$$\psi[m] = [\arg(R[m]) - \arg(R[m-1])]_{2\pi}, \quad 1 \leq m \leq H \quad (10)$$

where $[x]_{2\pi}$ denotes the modulo- 2π operation. The resulting values are used with the weights shown in

$$w[m] = \frac{3(L-m)(L-m+1) - H(L-H)}{H(4H^2 - 6LH + 3L^2 - 1)} \quad (11)$$

where m is evaluated over the same range in (10). Using (10) and (11) it is possible to determine the CFO estimate

$$\hat{v} = \sum_{m=1}^H w[m]\psi[m] \quad (12)$$

which may be used for correction.

E. CFO Correction

The approximation of the desired signal may be given by

$$\hat{s}[n] = y[n] \exp\left(\frac{-j2\pi\hat{v}n}{T}\right) \quad (13)$$

For implementation purposes (2) may be represented as

$$y[n] = y_I[n] + jy_Q[n] \quad (14)$$

where $y_I[n]$ is the real component and $y_Q[n]$ is the imaginary component of (2). Using Euler's Formula it is possible to represent the in-phase component of (13) as

$$\hat{s}_I[n] = y_I[n] \cos\left(\frac{-2\pi\hat{v}n}{T}\right) - y_Q[n] \sin\left(\frac{-2\pi\hat{v}n}{T}\right) \quad (15)$$

while similarly the quadrature phase component of (14) may be given as

$$\hat{s}_Q[n] = y_I[n] \sin\left(\frac{-2\pi\hat{v}n}{T}\right) + y_Q[n] \cos\left(\frac{-2\pi\hat{v}n}{T}\right) \quad (16)$$

which results in (13) being equivalent to

$$\hat{s}[n] = \hat{s}_I[n] + j\hat{s}_Q[n] \quad (17)$$

which allows for correction to be implemented in a hardware based design.

III. SYSTEM DESIGN

An overview of the entire system layout is presented in Figure 2 containing both the script and hardware portions of the design.

A. MATLAB Script

The signal $s[n]$ is generated in the MATLAB workspace for a chosen design parameter L and FFT size N . The system is capable of implementing L values of 8, 16, 32, and 64. FFT sizes of 64 and 128 are supported. The system allows for preambles of length 32 or 64 samples. The structure described in Figure 1 is implemented with different levels of distortion from (1) and (2). The signal represented in (2) is imported into the System Generator model as two time series variables representing the in-phase and quadrature phase samples. The configured preamble and pilot symbol from the MATLAB workspace is represented through multiple decimal values for both real and imaginary components. To avoid issues with MATLAB precision for binary to decimal conversion, each decimal value represents a 32 bit binary number. The system is capable of storing training data for multiple signal types, and the calculation of (4) is performed in parallel to determine which signal type was detected.

B. System Generator Model

As the next step, System Generator was used to target the design for a Virtex-6 ML605 FPGA evaluation board. In addition to the variables provided from Section III-A, the system also requires knowledge of which FFT size and design parameter L were chosen along with the length of the packet payload in terms of OFDM symbols.

1) Energy Detection:

The computation of (3) is used to determine the presence of a signal by comparing the output value to a predetermined threshold. For time smoothing purposes addressable shift registers are used on the in-phase and quadrature phase samples.

2) Matched Filter:

The decision from the energy detector is used as an enable signal for the cross-correlator. The multiplications with the training data are performed in parallel and the additions are cascaded. The computation of (4) may be performed for multiple sets of training data in parallel. Addressable shift registers are also used in the computation for time smoothing. The decision whether the received signal corresponds to a

TABLE I: Resource estimation targeted to an ML605 Virtex6 Board.

Resource Name	Count	% Utilization
LUT's	60122	40
FF's	37820	12
BRAM's	22	2
Mult/DSP48	66	8

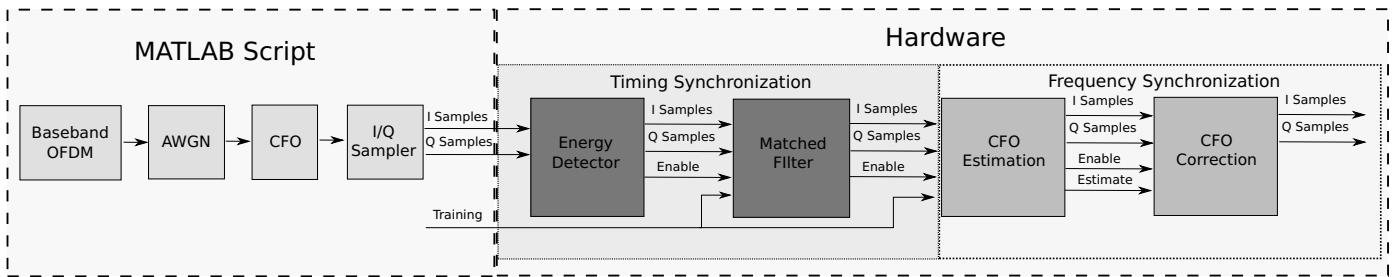


Fig. 2: System Layout.

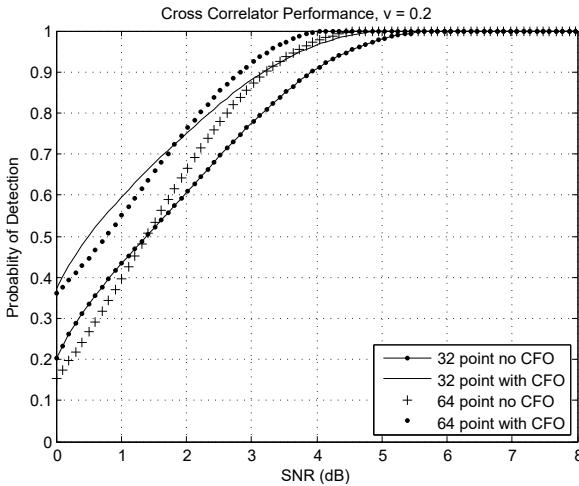


Fig. 3: Simulation— Cross Correlator Performance over SNR given CFO of 0.2.

particular set of training data is based on comparing a threshold to the sum of the terms in (5). The signal samples are delayed in such a manner that the inputs to the CFO Estimation block align with the CFO training data. The decision from the matched filter is used as an enable signal for the CFO Estimation component.

3) CFO Estimation:

- **Modified Correlation:** The calculation of (6) is implemented for both parameters of N by having two subsystems in parallel that accept the system inputs. By using the enable signal, and based on the value of N provided to the system, each correlation subsystem will be either enabled or disabled for computation. Each subsystem consists of four correlation blocks which calculate $r_{II}[m]$, $r_{QQ}[m]$, $r_{IQ}[m]$, and $r_{QI}[m]$ from (8) and (9). The correlation blocks take the corresponding sample stream, training data, design parameter L , and iteration number m . The training data is linked directly to the decision of which type was selected during timing synchronization. The value of m is based on the design parameter L selected via a multiplexed counter. The sample stream is written to a RAM block addressed by a counter that is count limited to N . For efficiency, the computation of (6) is accomplished fully in parallel with N branches that read the RAM addressed at a given element number and write to a unique register. Considering the number of active branches changes based on the value of k in (6), branches are disabled if their

element number is below a corresponding pre-calculated k value taken from a multiplexer based on the parameters chosen at iteration m . Training data is accessed using a slice block and multiplied to the corresponding received sample. A cascade of additions is used to obtain (8) and (9). To avoid division operations, the scaling factors shown in (6) are pre-calculated and multiplexed based on selected parameters to obtain (6).

- **Correlation Phase Difference:** A CORDIC module is used to calculate the arg or ATAN2 of the results from the modified correlation. The processing delay is accounted for while subtracting the phase output from the current value. The modulo- 2π operation is performed on the result by subtracting a bit sliced version of the result from its original value to obtain (10).
- **Phase Estimate:** The weights used in (11) are pre-calculated and multiplexed based on the chosen parameters N and L . Using the correlation phase difference values it is possible to determine the CFO estimate in (12). To improve performance under low SNR scenarios in which estimates may be unreliable, values outside of the range of $\pm \frac{2\pi}{L}$ are set to either $\frac{2\pi}{L}$ or $-\frac{2\pi}{L}$ based on the sign of the estimate.
- **Data Output:** The length of the payload in terms of OFDM symbols and N are used to align the in-phase and quadrature phase samples so that the pilot symbol is removed from each stream and only the payload remains.

4) CFO Correction:

For the correction subsystem, the starting and ending time indices n_{start} and n_{end} are needed. The enable stream from the input to the CFO estimation block is delayed to reset a free running counter which is used with n_{start} , n_{end} , and v to determine the argument required for (13). The argument is input into a CORDIC to obtain the cosine and sine functions evaluated at the value. The data streams are multiplied by the outputs of the CORDIC and summed in a manner to result in (15) and (16). Through experimental results, it was determined that division by the packet length was not required for correction of individual samples. Obtaining an overall CFO estimate requires the output of the CFO estimation block to be scaled by the ratio of the packet length and N .

5) Resource Utilization:

A summary of the number of estimated resources required for the System Generator model with three sets of training data considered is shown in Table I. The percentage of

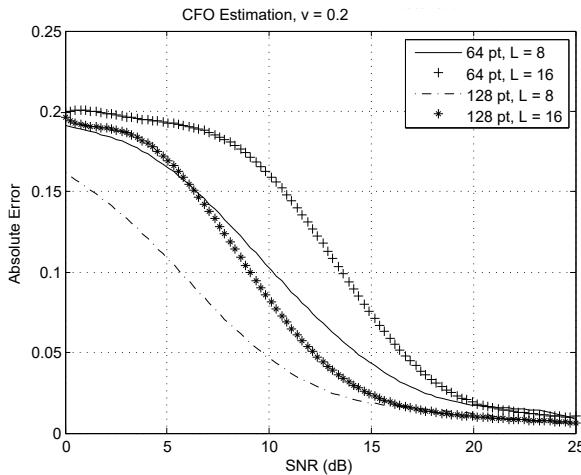


Fig. 4: Simulation— Mean Error estimate from actual CFO over SNR given CFO of 0.2.

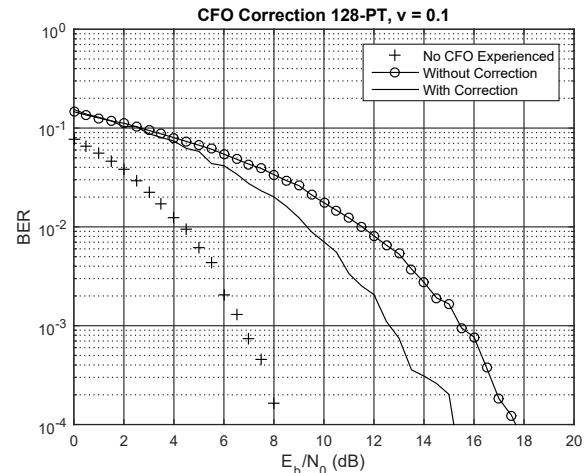


Fig. 6: Simulation— BER over SNR given CFO of 0.1 for 128-PT Symbol.

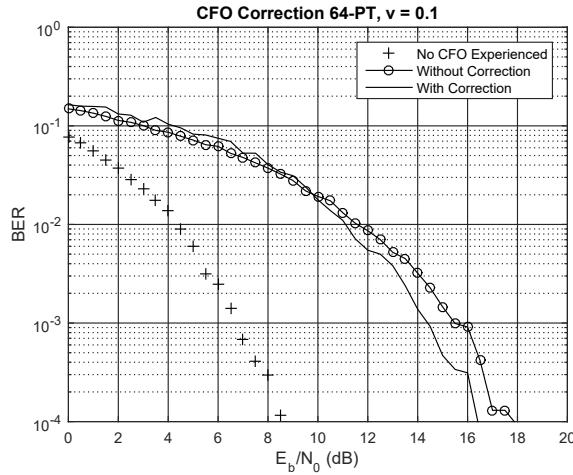


Fig. 5: Simulation— BER over SNR given CFO of 0.1 for 64-PT Symbol.

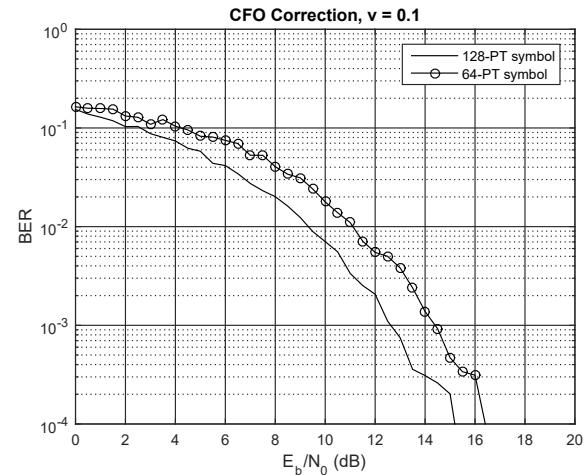


Fig. 7: Simulation— BER over SNR given CFO of 0.1 Comparison.

resources used is based on the ML605 Virtex-6 evaluation board. Overall the number of resources required for the system was significantly reduced due to the parallel nature of the design, as seen by the low number of multipliers and Block RAMs required. The quantity of look-up tables and flip-flops necessary for the system are due to the variable options for design parameters that may be selected. The results shown in Table I show that the design could be part of an overall system and easily adapted to reduce the number of resources it requires.

IV. SYSTEM PERFORMANCE

A System Generator model was simulated to view the performance of the matched filter over an AWGN channel with CFO effects. Preambles of length 32 and 64 were analyzed with and without a constant CFO of 0.2. Probability of detection for each case was determined over various levels of SNR by performing 200 repeated trials for each scenario and determining the percentage of occurrences of proper classification as shown in Figure 3. As expected, there was a

small degradation with CFO effects included, but performance maintained acceptable levels. In addition it was also determined that the 64 sample length preamble slightly outperformed the 32 sample preamble length.

The estimation block was analyzed by determining the relationship between CFO estimate mean error over an AWGN channel through simulation. OFDM signals with FFT sizes 64 and 128, pilot symbol design parameters L of 8 and 16, and 2 OFDM symbols per packet with spacing between packets of one half of the packet length were considered. A constant CFO of 0.2 was attributed to each packet. Different levels of SNR were examined for 200 repeated trials for each different configuration to obtain the results shown in Figure 4. Under very low levels of SNR it may be seen that the system is unable to properly estimate the CFO for all combinations of FFT size and design parameter, which is a result to the vast distortion of the training data. As expected, the mean error of the estimate from the CFO decreased as the SNR increased for all parameters. Using an FFT size of 128 was shown to yield superior results to an FFT size of 64, and a design parameter

of 8 outperformed the selection of 16 for both cases. With regards to the design parameter the results are directly due to the size of the pilot symbols used. For an FFT size of 64, a design parameter of 16 would yield 16 repetitions of 4 symbols, which may hinder the estimation success. The selection of larger design parameters is appropriate for larger FFT sizes.

To determine the performance of the correction system, a separate simulation was performed to analyze the effects of the system on Bit Error Rate (BER) over an AWGN channel. The signal structure described for the results in Figure 4 were used for the configurations with a design parameter of 8, with a constant CFO of 0.1, and varying SNR values. Each packet payload was demodulated from OFDM to QPSK symbols in script. For each frame of QPSK symbols, a decision device with a QPSK decoder was used to determine the received bit stream and were compared to the original bit stream generated to determine BER. The results for the 64-PT pilot symbol configuration are shown in Figure 5 and in Figure 6 for the 128-PT configuration. For each SNR value there were 200 repeated trials considered for BER calculation for the cases of purely AWGN, AWGN with CFO and no correction, and AWGN with CFO and correction on FPGA. As expected, the BER decreased as the SNR increased for all three scenarios, with the presence of CFO causing a decrease in performance from the purely AWGN case for both pilot symbol sizes shown in Figures 5 and 6. There is a fluctuation of the BER curve for the corrected scenario under low SNR due to the accuracy of the CFO estimate as shown in Figure 4. In addition, a comparison of the outcomes obtained for both FFT sizes is shown in Figure 7, where it may be seen that the 128-PT pilot symbol outperformed the 64-PT pilot symbol, mirroring the results shown in Figure 4. Overall the results show that the CFO corrected samples outperform the case without correction, demonstrating that the scheme implemented in this paper is able to improve system performance while using only 1 pilot symbol.

V. CONCLUSION

In this work, a trained timing and coarse CFO estimation and correction system for OFDM signals was implemented on an FPGA using Xilinx System Generator. The signal throughput may be increased from previous implementations due to the requirement of only one pilot symbol. The correction scheme performance for different pilot symbol design parameters was examined. System performance was shown to improve over an AWGN channel given a constant CFO with the implemented correction scheme.

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