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Accumulation-Type Ohmic van der Waals Contacts to Nearly Intrinsic WSe_2 Nanosheet-Based Channels: Implications for Field-Effect Transistors

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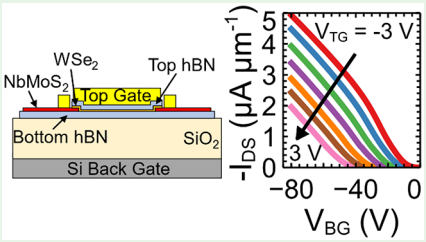
ABSTRACT: We report the fabrication of ohmic van der Waals (vdW) contacts to nearly intrinsic WSe_2 nanosheet-based channels in field-effect transistors (FETs) using degenerately p-doped MoS_2 (p^+-MoS_2) as a contact metal. We demonstrate that accumulation-type ohmic contacts and the high device performance are achievable without electrostatically gating the drain/source contact regions despite the nearly intrinsic nature of WSe_2. Back-gated WSe_2 FETs with p^+-MoS_2 bottom contacts (which screen the back-gate electric field in the drain/source regions) exhibit linear output characteristics, a high on/off ratio of 10^8, and a high two-terminal field-effect mobility up to ~200 $cm^2\ V^{-1}\ s^{-1}$ at room temperature. Our theoretical modeling reveals that the p^+-MoS_2/WSe_2 vdW junction behaves like a metal/semiconductor ohmic contact signified by a vanishingly thin space-charge region of ~1 nm on the p^+-MoS_2 side and a substantial accumulation layer of free holes on the WSe_2 side, which is further verified by additional temperature-dependent and dual-gated measurements of WSe_2 FETs. We attribute the formation of accumulation-type ohmic contacts free of a Schottky barrier to the near absence of Fermi-level pinning at the vdW interface and the work function of p^+-MoS_2 being larger than the ionization energy of WSe_2. This study represents an important step toward achieving low-resistance ohmic contacts to two-dimensional (2D) semiconductors by eliminating the Fermi-level pinning effects, which is expected to have significant implications for next-generation 2D semiconductor-based nanoelectronics.



KEYWORDS: *degenerately doped, MoS_2, WSe_2, two-dimensional, field-effect transistor, Schottky barrier, Fermi-level pinning, ohmic contact*

INTRODUCTION

Two-dimensional (2D) semiconductors such as transition-metal dichalcogenides (TMDs) have captivated the attention of the scientific community for about a decade now because they have demonstrated a multitude of graphene-like properties desirable for flexible electronics and optoelectronics,[1−6] including a moderately high carrier mobility, mechanical flexibility, and chemical and thermal stability, moreover, offering the significant advantage of a substantial band gap essential for digital electronics.[7−12] Field-effect transistors (FETs) with atomically thin 2D channels are also immune to short channel effects.[13] In addition, pristine surfaces of 2D semiconductors are free of dangling bonds, which reduces surface roughness scattering and interface traps. Furthermore, the direct band gap in monolayer TMDs also makes them promising candidates for novel optoelectronic devices.[14,15] However, a major materials challenge of 2D semiconductors is that they tend to form a substantial Schottky barrier with most metals used for making electrical contacts, severely limiting both the fundamental research and electronics/optoelectronics applications of 2D semiconductors.[9,16−19]

Schottky barrier formation is a ubiquitous phenomenon that occurs at metal/semiconductor contacts. When a metal is placed in contact with a semiconductor, charge transfer between them usually creates a surface-charge layer on the metal side and an extended space-charge (depletion) region of equal magnitude and opposite sign on the semiconductor side to produce a macroscopic dipole. Consequently, an energy barrier is formed to prevent carriers from moving between the metal and semiconductor. In ideal metal/semiconductor contacts, the height of this energy barrier, known as the Schottky barrier (SB), is determined by the Schottky−Mott rule: $\Phi_{SB,p} = I - W$ and $\Phi_{SB,e} = W - \chi$, where $\Phi_{SB,p}$ and $\Phi_{SB,e}$ are the Schottky barrier height (SBH) for holes and electrons, respectively, W is the work function of metal, and I and χ are the ionization energy and electron affinity of the semi-

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conductor, respectively. Theoretically, the Schottky−Mott rule also predicts a "negative" SBH for $W > I$ (or $W < \chi$). In the ideal case, an accumulation region of holes (electrons) occurs on the semiconductor side of the metal/semiconductor contact for $W > I$ ($W < \chi$), leading to an accumulation-type ohmic contact free of an energy barrier. Experimentally, however, a finite positive SBH associated with an extended depletion region on the semiconductor side has often been observed at the metal/semiconductor interface (even when $W > I$ or $W < \chi$) since the early days of semiconductor research. As first explained by Bardeen, this phenomenon arises because of the presence of additional electronic states at the interface and is referred to as "Fermi-level pinning".[20] These interface states can absorb charge and, consequently, form an atomically scaled dipole layer at the metal/semiconductor junction in addition to the macroscopic dipole. The strength of Fermi-level pinning is quantified by an S parameter in the range of 0−1, indicating to what degree the experimentally measured SBH deviates from the theoretical prediction based on the Schottky−Mott rule ($S = 1$ in the Schottky−Mott limit, and $S = 0$ in the strong Fermi-level pinning limit).[21] Fermi-level pinning also occurs in semiconductor heterojunctions, arising from an atomic-scale dipole at the interface of two semiconductors. As a result, the band offsets of the two semiconductors deviate from the theoretical prediction of Anderson's rule (also known as the electron affinity rule).[22] In the extreme case where one of the semiconductors forming the junction is degenerately doped, semiconductor heterojunctions become Schottky junctions because the depletion layer on the degenerately doped semiconductor side becomes vanishingly thin (∼1 nm) and virtually all band bending occurs on the other side of the junction.[23]

Ideally, Fermi-level pinning can be avoided by eliminating interface states at the metal/semiconductor contacts. In practice, however, it is extremely challenging to eradicate interface states. The formation of interface states at metal/semiconductor junctions is a complex phenomenon and can have multiple origins.[24] Particularly, structural, chemical, and electronic disorder already present in the semiconductor or created during the metal deposition or induced by the substrate can all generate defect-induced gap states. At a metal/semiconductor interface, the wave function of electrons in the metal can penetrate into the semiconductor, forming a continuum of metal-induced gap states (MIGS). In addition, chemical bonds and strains at metal/semiconductor interfaces may also create interface states.[21] The convolution of multiple factors involved in Fermi-level pinning presents a major challenge to create low-resistance ohmic contacts with vanishing SBHs for semiconductor electronic devices. To circumvent this challenge, low-resistance ohmic contacts in Si-based electronic devices are achieved by thinning the SB width by degenerately doping the semiconductor in the contact regions. This is realized by selective ion-implantation doping of the drain and source contact regions under the metal electrodes. However, the atomic thickness of 2D-layered materials prevents controlled and spatially defined heavy doping by ion implantation. Therefore, it is essential to minimize the SBH in order to achieve low-resistance ohmic contacts. Metals of very low and high work functions have been used in attempts to eliminate the SB for the electron and hole channels of 2D semiconductors, respectively, but yielded only limited success largely because of the Fermi-level pinning effect.[18,25] Various alternative strategies to reduce the contact barrier such as surface and substitutional doping,[9,10,26−28] phase engineering,[29,30] use of graphene contacts,[3,12,31,32] insertion of a work-function-matching buffer layer,[33] and edge contacts[34,35] are still deficient because they have insufficient air or thermal stability and limited spatial definition of the contact regions or do not offer true ohmic contacts.

van der Waals (vdW) contacts have recently emerged as a promising contact-engineering strategy to reduce the interface states and thus minimize the Fermi-level pinning effects at the metal/2D semiconductor contact. The authors were among the first to demonstrate low-resistance vdW contacts by using degenerately doped WSe_2 as the contact metal and intrinsic WSe_2 nanosheets as the channel material.[36] However, the back-gated FETs with top contacts used in our previous study were not capable of unequivocally distinguishing between Schottky contacts with a small SBH and accumulation-type ohmic contacts (which are truly SB-free) because the back-gate simultaneously modulates both the channel and drain/source regions.[36] As the channel is being "turned on" by the back-gate voltage, the small SB at the drain/source contacts is also being thinned down, leading to enhanced tunneling and thermally assisted tunneling currents through the SB. Subsequently, vdW contacts between transferred metals and 2D semiconductors were also reported.[37,38] Electrical contacts formed by transferring prefabricated metal electrodes onto 2D semiconductors demonstrated SBHs approaching the Schottky−Mott limit, which was attributed to the minimization of structural and chemical defects at the interface by avoiding direct metal deposition on the 2D semiconductors.[37] However, these contacts exhibit a notable positive SBH even when the work function of metal is significantly larger than the ionization energy of 2D semiconductors ($W > I$), indicating that Fermi-level pinning is still present (although significantly reduced compared to directly deposited metal contacts). The Fermi-level pinning effects at the interface between the transferred metal and 2D semiconductor may be attributed to the finite surface roughness of transferred elemental metal electrodes and/or MIGS.[39] To date, accumulation-type ohmic contacts completely free of a SB have not been experimentally demonstrated in 2D semiconductor FET devices to the best of our knowledge.

In this paper we demonstrate accumulation-type ohmic contacts formed between a nearly intrinsic 2D semiconductor and a degenerately doped 2D semiconductor acting as a metal. Dual-gated FETs consisting of degenerately p-doped MoS_2 (p^+-MoS_2) underneath a nearly intrinsic (nominally undoped) WSe_2 nanosheet were fabricated as the test structures, where the former serves as bottom contacts and the latter works as the channel material. A degenerately doped Si substrate with a hexagonal boron nitride (hBN)/SiO_2 dielectric stack was used as the back-gate. A metal top gate with a hBN dielectric was also fabricated, covering both the channel and parts of the drain/source regions. In these devices, the top gate is used to control both the contacts and channel, while the back-gate is used to modulate the channel only (due to the screening by the bottom contacts). Linear output characteristics were observed in both the top-gate and back-gate configurations (with the other gate grounded), indicating ohmic behavior. Moreover, back-gated and top-gated transfer characteristics exhibit an equally high on/off ratio exceeding 10^8 and a two-terminal field-effect mobility of ∼130 $cm^2\ V^{-1}\ s^{-1}$ at room temperature, which could be further improved to approach the intrinsic mobility of few-layer WSe_2 (∼200 $cm^2\ V^{-1}\ s^{-1}$) by

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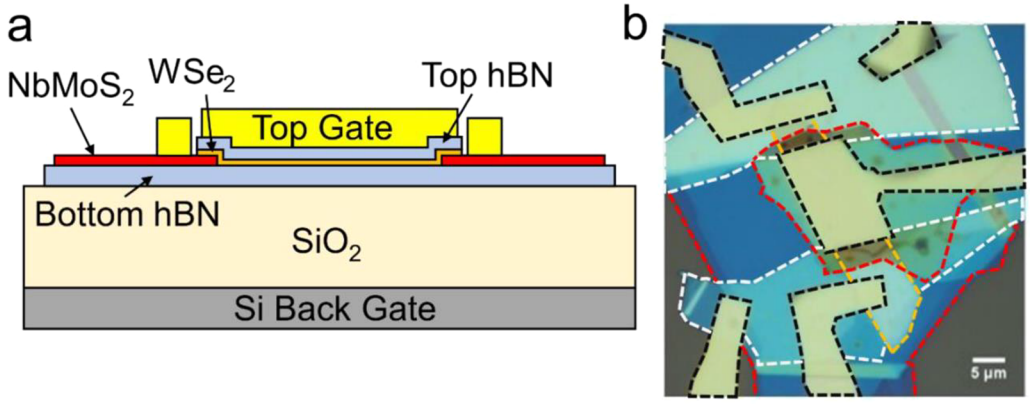

Figure 1. Side-view schematic (a) and optical micrograph (b) of dual-gated WSe_2 FETs with p^+-MoS_2 ($NbMoS_2$) bottom contacts. The white and orange dashed lines outline the p^+-MoS_2 ($NbMoS_2$) contacts and the intrinsic WSe_2 channel, respectively. The red dashed lines are the boundaries of the hBN flakes that sandwich the WSe_2 channel from top and bottom. The black dashed lines represent the outlines of metal electrodes on top of the p^+-MoS_2 contacts and top gate.

minimizing the series resistance of excess p^+-MoS_2 extending from the drain/source contacts. Because the WSe_2 channel is nearly intrinsic and the back-gate is unable to modulate the contact region, the presence of a SB would degrade the device performance in the back-gate configuration, as previously demonstrated in WSe_2 FETs with Pt bottom contacts.[25] The ohmic behavior and excellent device performance observed in the back-gate configuration provides strong initial evidence of SB-free ohmic contacts in our WSe_2 devices. As the temperature decreases, the back-gate drain/source current and two-terminal field-effect mobility increase while the contact resistance remains nearly constant, further indicating the absence of a SB at the drain/source contacts. Additionally, dual-gated transfer characteristics were measured to confirm the accumulation-type contacts. While the back-gated transfer characteristics shift positively (negatively) with an increasingly negative (positive) top-gate voltage due to the dual gating of the channel, the current as a function of the carrier density slightly increases (decreases). This finding is in stark contrast with what is expected for Schottky contacts but consistent with the accumulation-type ohmic contacts for the hole channel. Theoretical modeling shows that a p^+-MoS_2 in contact with an intrinsic (or lightly p-doped) WSe_2 essentially behaves as a metal with a vanishingly thin space-charge region of ~1 nm on the p^+-MoS_2 side and that a relatively large areal density of free holes accumulated on the WSe_2 side of the contact, in good agreement with the experimental results. Moreover, the subthreshold swing (SS) in the top-gated transfer characteristics is insensitive to the concentration and polarity of the back-gate-induced excess carriers in the WSe_2 channel, providing further evidence of accumulation-type ohmic contacts.

RESULTS AND DISCUSSION

Parts a and b of Figure 1 depict respectively a schematic diagram and an optical micrograph of a dual-gated WSe_2 device composed of a nearly intrinsic (nominally undoped) WSe_2 nanosheet-based channel on top of two p^+-MoS_2 bottom contacts. To fabricate the dual-gated FETs, 10−30-nm-thick hBN flakes exfoliated on degenerately doped Si with 280 nm of thermal oxide were used as ultraflat and ultrasmooth substrates to minimize dangling bonds and charge traps. The hBN/SiO_2 stack was also used as the back-gate dielectric. Next, mechanically exfoliated pairs of p^+-MoS_2 flakes (6−12 nm thick) containing 0.5% Nb were placed on the hBN substrates as 2D vdW bottom contacts by a dry transfer method.[36,40,41] TMDs such as WSe_2 and MoS_2 doped with 0.5% Nb have a nearly temperature-independent hole density of $(3-5) \times 10^{19}$ cm^{-3}.[42] When p^+-MoS_2 with such a high carrier concentration forms a vdW heterojunction with nearly intrinsic WSe_2, the space-charge region on the p^+-MoS_2 side becomes vanishingly thin (~1 nm) and almost all of the band-bending occurs on the intrinsic WSe_2 side (see section 4 of the Supporting Information). Therefore, the p^+-MoS_2/WSe_2 junction effectively behaves as a 2D metal/semiconductor contact. We chose 6−12-nm-thick p^+-MoS_2 bottom contacts to ensure that they are thick enough to screen the back-gate electric field, while minimizing the step size at the contact edges. Subsequently, a few-layer intrinsic WSe_2 channel was stacked on top of a pair of p^+-MoS_2 drain/source electrodes also by the dry transfer method, followed by dry transferring another hBN flake on top to cover the WSe_2 nanosheet-based channel and parts of the drain/source contacts serving as a top-gate dielectric. Finally, the metal top gate and interconnects to the p^+-MoS_2 drain/source contacts, consisting of 10 nm Ti and 40 nm Au, were fabricated by electron-beam lithography and electron-beam-assisted metal deposition. A slight overlap between the metal top gate and drain/source contacts was assured to enable electrostatic modulation of WSe_2 in both the channel and drain/source regions by the top gate. By contrast, the back-gate electric field is screened by the bottom contacts and therefore can only tune the channel region. Note that the overlap between one of the metal electrodes and the WSe_2 nanosheet beyond the channel region (i.e., outside the active p^+-MoS_2/WSe_2 vdW contact region) does not alter the carrier injection behavior because the contact resistance of the metal/WSe_2 contact is significantly larger than that of the p^+-MoS_2/WSe_2 contact due to the significant SB at the metal/WSe_2 contact.

We chose p^+-MoS_2 as drain/source electrodes and intrinsic WSe_2 as the channel material for the following reasons. First, the surfaces of the 2D vdW materials are truly atomically flat, while the surfaces of the transferred elemental-metal contacts have a finite surface roughness (~0.3−0.8 nm depending on the metal).[39] Second, degenerately doped 2D semiconductors are chemically and environmentally more stable than most metallic 2D-layered materials (such as $NbSe_2$ and NbS_2). Recent studies on $NbSe_2$ found that thin $NbSe_2$ deteriorates

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greatly under ambient conditions and/or during lithography processing.[43,44] Third, the work function of p^+-MoS_2 with an appropriate doping concentration is larger than the ionization energy of undoped WSe_2, which is needed to achieve a SB-free contact in the absence of Fermi-level pinning (based on the Schottky−Mott rule). It is important to point out that p^+-MoS_2 with a proper doping concentration is critical to the formation of accumulation-type ohmic contacts. While insufficient doping widens the space-charge region on the p^+-MoS_2 side, excessively heavy doping of p^+-MoS_2 may reduce its ionization energy and work function to such a degree that the work function of p^+-MoS_2 becomes smaller than the ionization energy of the nearly intrinsic WSe_2, which can cause a finite positive SBH at the p^+-MoS_2/WSe_2 contact.[45,46] Fourth, because p^+-MoS_2 and WSe_2 have similar crystal and electronic structures, sources of Fermi-level pinning such as MIGS (arising from the wave function in metal penetrating into the semiconductor) are also minimized at their heterojunction. Finally, nearly intrinsic WSe_2 is chosen to maximize the contrast between Schottky and accumulation-type contacts.

A distinctive feature of accumulation-type ohmic contacts is that ohmic behavior and low contact resistance can be achieved without the need of doping or electrostatic gating of the semiconductor in the contact region. By contrast, Schottky contacts (metal/semiconductor contacts with a finite positive SBH) require substantial chemical doping and/or electrostatic gating of the contact regions to thin down the SB in order to achieve ohmic-like behavior and a reasonably good device performance. This distinction between accumulation-type ohmic and Schottky contacts is most pronounced when the semiconductor is intrinsic. To demonstrate accumulation-type contacts, we first compare the back-gated and top-gated output and transfer characteristics of dual-gated FETs with a nearly intrinsic WSe_2 nanosheet-based channel and p^+-MoS_2 bottom contacts. In all measurements except otherwise noted, the top gate is grounded when back-gated transfer and output characteristics are measured and vice versa. Parts a and b of Figure 2 show that both the back-gated and top-gated output characteristics of the device (depicted in Figure 1) are linear at all back-gate voltages, signifying ohmic behavior. Additionally, the transfer characteristics of the WSe_2 device measured at V_{DS} = −100 mV exhibit clear p-type behavior with a high on/off ratio of 10^8 in both the top-gate and back-gate configurations, as shown in Figure 2c,d. The high on/off ratio can be partially attributed to enhancement of the on-current enabled by low-resistance contacts.

To quantitatively compare the top-gated and back-gated transfer characteristics, the field-effect mobility is extracted from the linear regions of the transfer characteristics in Figure 2c,d using the expression

$$\mu_{FE} = \frac{1}{C_G V_{DS}} \frac{L}{W} \frac{dI_{DS}}{dV_G} \quad (1)$$

where C_G is the gate capacitance (49-nm-thick hBN dielectric for the top gate and an equivalent series capacitance of 280 nm SiO_2 and 27-nm-thick hBN substrate/dielectric for the back gate), L is the channel length, and W is the channel width. Interestingly, a nearly identical two-terminal field-effect mobility of ∼130 $cm^2\ V^{-1}\ s^{-1}$ is obtained from both the top-gated and back-gated transfer characteristics. This two-terminal mobility value compares well with prior reports of the field-effect mobilities in few-layer WSe_2[25,46,47] and can be further

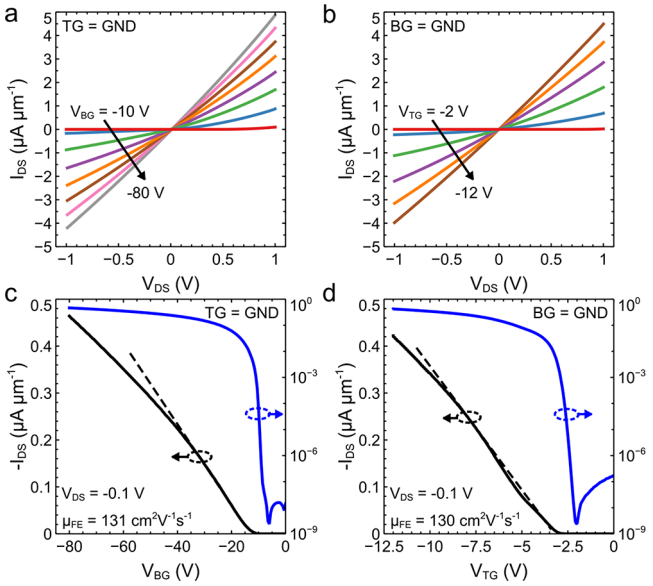

Figure 2. Output (a and b) and transfer (c and d) characteristics of a dual-gated WSe_2 FET with p^+-MoS_2 contacts and a 16-μm-long, 7.6-μm-wide, and 12-nm-thick WSe_2 channel measured in the back-gate (a and c) and top-gate (b and d) configurations. The top gate is grounded for back-gate measurements and vice versa.

improved to approach the phonon-limited hole mobility of few-layer WSe_2 at room temperature (∼200 $cm^2\ V^{-1}\ s^{-1}$) by minimizing the parasitic series resistance of the p^+-MoS_2 (see section 1 of the Supporting Information). The observed linear output characteristics, high on/off ratio, and high two-terminal extrinsic mobility provide initial evidence of low-resistance ohmic contacts in the WSe_2 device. In particular, the ohmic behavior and high two-terminal mobility in the back-gate configuration were achieved without electrostatically doping the nearly intrinsic WSe_2 in the contact regions, which has not been previously demonstrated in 2D semiconductor-based FETs to the best our knowledge.

Ohmic-like behavior is expected for our top-gated WSe_2 FET at sufficiently high top-gate voltages because the top gate electrostatically dopes the contact regions to thin down any small positive SB, if present. Moreover, interface states in WSe_2 at the p^+-MoS_2/WSe_2 contact are minimized because of the relatively weak vdW coupling between p^+-MoS_2 and WSe_2, which not only diminishes the Fermi-level pinning effects but also enhances top-gate control of the contact regions. The operation mechanism of the top-gated WSe_2 FETs with bottom contacts is similar to that of back-gated WSe_2 FETs with degenerately p-doped WSe_2 (p^+-WSe_2) top contacts, as demonstrated in our previous study as well as top-gated WSe_2 FETs with prefabricated Pt bottom contacts.[25,36]

By contrast, the back-gate alone is unable to electrostatically dope WSe_2 in the drain/source regions of the WSe_2 FET because of electrostatic screening by the bottom contacts. If the contacts were of the Schottky type, the presence of a finite positive SB in conjunction with a nearly intrinsic channel material would lead to high contact resistance and consequently degrade the device performance such as the on/off ratio and two-terminal mobility.[25] Therefore, accumulation-type ohmic contacts are essential to achieving good device performance in back-gated WSe_2 FETs with bottom contacts and a nearly intrinsic channel. The equally high performance observed in the back-gate configuration as in the top-gate

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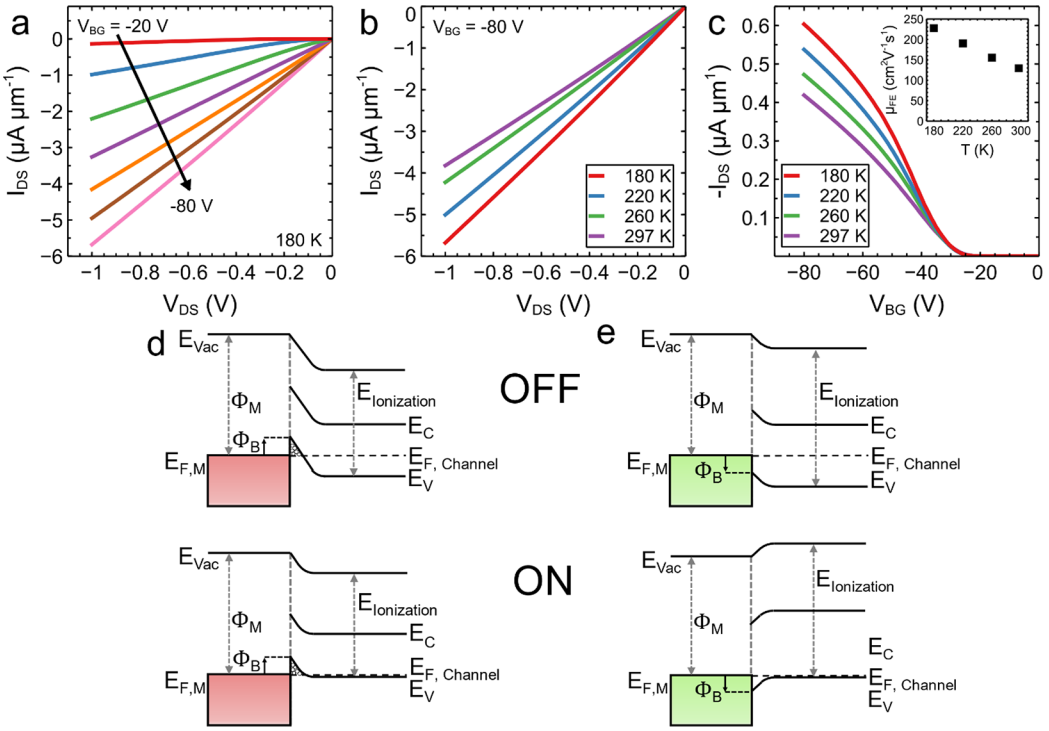

Figure 3. (a) Back-gated output characteristics of a WSe_2 FET with p^+-MoS_2 bottom contacts measured at 180 K. (b) Current−voltage characteristics of the device measured at V_{BG} = −80 V and various temperatures between 180 and 297 K. (c) Back-gated transfer characteristics of the device measured at V_{DS} = −100 mV and various temperatures between 180 and 297 K. The top gate is grounded for all measurements. Band diagrams of the accumulation-type (d) and Schottky (e) contacts.

configuration (with the other gate grounded) is in stark contrast with the behavior of the WSe_2 devices with Schottky contacts reported in the literature,[25,38] providing strong initial evidence of accumulation-type ohmic contacts in the WSe_2 device with p^+-MoS_2 contacts. It is worth pointing out that the relatively low on-current in our device is largely due to the relatively long WSe_2 channel, which dominates the total resistance of the device. We envision that the on-current can be substantially improved by drastically reducing the channel length.

Although vdW contacts formed between transferred or prefabricated metal electrodes and 2D semiconductors were previously reported to show significantly reduced Fermi-level pinning and lower SBH, accumulation-type ohmic contacts have not been reported to the best of our knowledge. Relatively high electrostatic doping of the contact regions (by a gate) was required to thin the SB in order to achieve reasonably good contacts in these prior studies.[25,37,38] In particular, dual-gated WSe_2 FETs with predeposited Pt bottom contacts exhibited a high on/off ratio exceeding 10^7 and a modestly high two-terminal field-effect mobility (~48 cm^2 V^{-1} s^{-1}) at room temperature in the top-gate configuration, but a negligibly small conductance and two-terminal mobility in the back-gate configuration (at zero top-gate voltage) due to the presence of a substantial SB and the intrinsic nature of WSe_2.[25] The nearly identical and relatively high two-terminal field-effect mobilities obtained from the back-gated (with the top gate grounded) and top-gated (with the back gate grounded) transfer characteristics in our WSe_2 devices indicates that the p^+-MoS_2/WSe_2 vdW contacts are ohmic without the need for electrostatic doping of the contact regions and have a negligible impact on the extracted two-terminal field-effect mobility. Ohmic contacts are important to accurately extract the field-effect mobility, and nonohmic contacts can lead to either underestimation or overestimation of the field-effect mobility in nanoscale transistors such as 2D FETs.[48] Overestimation of the field-effect mobility is possible in the presence of a notable Schottky contact that strongly depends on the gate voltage. This can be explained by strong suppression of the drain current by a large SB at low gate voltages, but the current rapidly increases at higher V_{GS} as the SB width is reduced by the gate voltage, resulting in an increased slope of its transfer characteristic and an overestimation of the field-effect mobility, as demonstrated in one of our recent works.[49] This possibility of a field-effect mobility overestimation can be ruled out in our WSe_2 FETs with bottom contact because the contact regions of these devices are not tunable by the back gate.

Another important characteristic that distinguishes accumulation-type ohmic contacts from Schottky contacts is that the contact resistance of the former is expected to be nearly independent of temperature (or may even decrease with decreasing temperature) because of the absence of a SB, while that of the latter drastically increases with decreasing temperature when the semiconductor in the contact region is nearly intrinsic and not electrostatically doped by a gate because of a decrease in thermionic and/or thermally assisted tunneling through a SB. Therefore, if the contacts of our WSe_2 devices were Schottky-type (with a finite positive SB), one would expect the on-current in the back-gate configuration (with the top gate grounded) to be increasingly limited by the contact resistance with decreasing temperature. However, the back-gated output characteristics of the WSe_2 device remain linear, and the drain/source current at the same gate voltage increases with decreasing temperature (Figure 3). This observation indicates that charge transport remains channel-

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limited rather than contact-limited as the temperature decreases. As shown in the inset of Figure 3c, the two-terminal mobility extracted from the linear region of the transfer characteristics (shown in Figure 3c) also increases from ∼130 $cm^2 V^{-1} s^{-1}$ at room temperature to ∼230 $cm^2 V^{-1} s^{-1}$ at 180 K, consistent with the phonon-scattering-limited mobility in the WSe_2 channel.[12,36] Furthermore, the threshold voltage remains essentially unchanged as the temperature decreases (as shown in Figure 3c), which is in stark contrast with 2D semiconductor FETs with Schottky contacts, where the drain/source current is increasingly suppressed by the SB as the temperature decreases, leading to a threshold−voltage shift.[49] It is important to point out that the channel-limited charge-transport properties shown in Figure 3 are achieved in a nearly intrinsic WSe_2 channel without electrostatically doping the contact regions, which is fundamentally different from WSe_2 FETs with vdW contacts in the literature because these previously reported WSe_2 devices require a relatively large gate voltage to "turn on" the contacts.[25,38]

To shed additional light on the nature of the vdW contacts used in our WSe_2 devices, we replaced p^+-MoS_2 with p^+-WSe_2 as the drain/source bottom contact. The primary difference between p^+-MoS_2 and p^+-WSe_2 is that the latter has a smaller work function than the former. In contrast, back-gated WSe_2 FETs with a p^+-WSe_2 bottom contact as the source exhibit increasingly nonlinear output characteristics and decreasing current as the temperature decreases, indicating that the current is limited by the presence of a finite positive SB (see section 2 of the Supporting Information). Indeed, a small positive SBH is obtained for the p^+-WSe_2/WSe_2 contact using a thermionic emission method (see section 3 of the Supporting Information). The SBH is determined as the activation energy extracted from the Arrhenius plot of the current at the flat-band gate voltage, where the activation energy starts to deviate from linear dependence of the gate voltage.[37,50−53] However, this technique is based on the condition that the current is predominantly limited by thermionic emission and thermally assisted tunneling through a finite energy barrier below and above the flat-band voltage, respectively. As the SBH approaches zero, the current becomes increasingly limited by the channel resistance. Because the phonon-limited mobility of WSe_2 decreases with the temperature, the current in the WSe_2 device is also expected to decrease with the temperature. As a result, a negative effective barrier height is predicted if the channel resistance dominates over the contact resistance. As shown in Figure S4, the effective barrier height extracted from the Arrhenius plots of a WSe_2 FET with p^+-MoS_2 contacts is indeed negative, suggesting a vanishing SBH at the p^+-MoS_2/WSe_2 contacts.

The observed qualitative difference between WSe_2 FETs with p^+-MoS_2 and p^+-WSe_2 bottom contacts can be attributed to the larger work function of p^+-MoS_2 in conjunction with the absence of Fermi-level pinning. Parts d and e of Figure 3 schematically show the energy band diagrams of the vdW junctions consisting of a nearly intrinsic WSe_2 channel contacted by p^+-MoS_2 and p^+-WSe_2 bottom contacts, respectively. Here the semiconductor heterojunctions at the drain/source contacts are treated as metal/semiconductor contacts because (i) the space-charge region on the p^+-MoS_2 side of the junction is vanishingly thin (∼1 nm) and thus can be treated as the surface-charge layer and (ii) virtually all of the band bending occurs on the nearly intrinsic WSe_2 side (see section 4 of the Supporting Information). The alignment of the Fermi energy (work function) of the p^+-MoS_2 (or p^+-WSe_2) and the valence-band maximum (ionization energy) of WSe_2 at the contact interface, which determines whether the contact is of the accumulation (ohmic) or Schottky type at the Schottky−Mott limit, depends on both the doping concentration and original valence-band offset before doping. Because degenerate p doping of TMDs such as MoS_2 and WSe_2 reduces their ionization energy, p^+-WSe_2 has a smaller ionization energy than WSe_2.[45] On the other hand, because the ionization energy of MoS_2 is larger than that of WSe_2,[54] it is possible for p^+-MoS_2 with an appropriate doping concentration to have larger ionization energy than WSe_2 as long as the reduction of the ionization energy due to hole doping is smaller than the valence-band offset between MoS_2 and WSe_2. Because the Fermi level of p^+-MoS_2 lies slightly below the valence-band maximum, its work function is expected to be slightly larger than its ionization energy. X-ray photoelectron spectroscopy (XPS) measurement shows that the ionization energy of p^+-MoS_2 is substantially larger than that of p^+-WSe_2 (see section 5 of the Supporting Information). In the Schottky−Mott limit (i.e., in the absence of Fermi-level pinning), an accumulation-type ohmic contact (with a nominally negative SB for holes) is expected when the work function of the metal (Φ_M) is greater than the ionization energy (E_I) of the semiconductor ($\Phi_M > E_I$), as in the case of p^+-MoS_2 contacts (shown in Figure 3d). Although the band offset between p^+-MoS_2 and WSe_2 may be slightly reduced by the possible formation of a quantum dipole at the vdW interface, the band lineup is not expected to change qualitatively (i.e., the work function of the former remains larger than the ionization energy of the latter).[55] On the other hand, a positive SB occurs for $\Phi_M < E_I$ as in the case of p^+-WSe_2 contacts (shown in Figure 3e). In addition, excessively heavy doping may reduce the ionization energy of MoS_2 beyond the valence-band offset between MoS_2 and WSe_2, consequently leading to a positive SBH. Indeed, a positive SBH of ∼41 meV was extracted when p^+-MoS_2 with an order of magnitude higher hole concentration (∼10^{20} cm^{-3}) was used to form the p^+-MoS_2/WSe_2 contact.[46] We attribute the finite SBH in ref 46 to the smaller work function of excessively heavily doped p^+-MoS_2 than the ionization energy of WSe_2.

Next, we quantitatively evaluate the contact resistance and its temperature dependence. Although the transfer length method is widely used to extract the contact resistance of 2D semiconductor transistors, it cannot be conveniently applied to our WSe_2 devices with p^+-MoS_2 bottom contacts because it requires multiple FET devices fabricated on the channel material with uniform contacts, uniform channel width, and varying channel length. Alternatively, we extract the contact resistance of our WSe_2 devices using the Y-function method. For a long-channel 2D semiconductor FET with a gate-independent carrier mobility and a negligible series resistance (R_S) at the contacts (in comparison with the channel resistance), a linear dependence of the drain/current on the gate voltage is expected. The slight sublinearity of the transfer characteristics exhibited by our WSe_2 device measured in the back-gate configuration indicates the presence of a non-negligible R_S at the contacts (Figure 3c). As discussed in detail below, R_S is dominated by the parasitic resistance of excess p^+-MoS_2 extending from the p^+-MoS_2/WSe_2 vdW contacts instead of the contact resistance at the vdW interface. To rule out the possibility of gate-dependent mobility as an alternative cause of the sublinear transfer characteristics,[56] we also carried out Hall-effect measurement on a few-layer WSe_2

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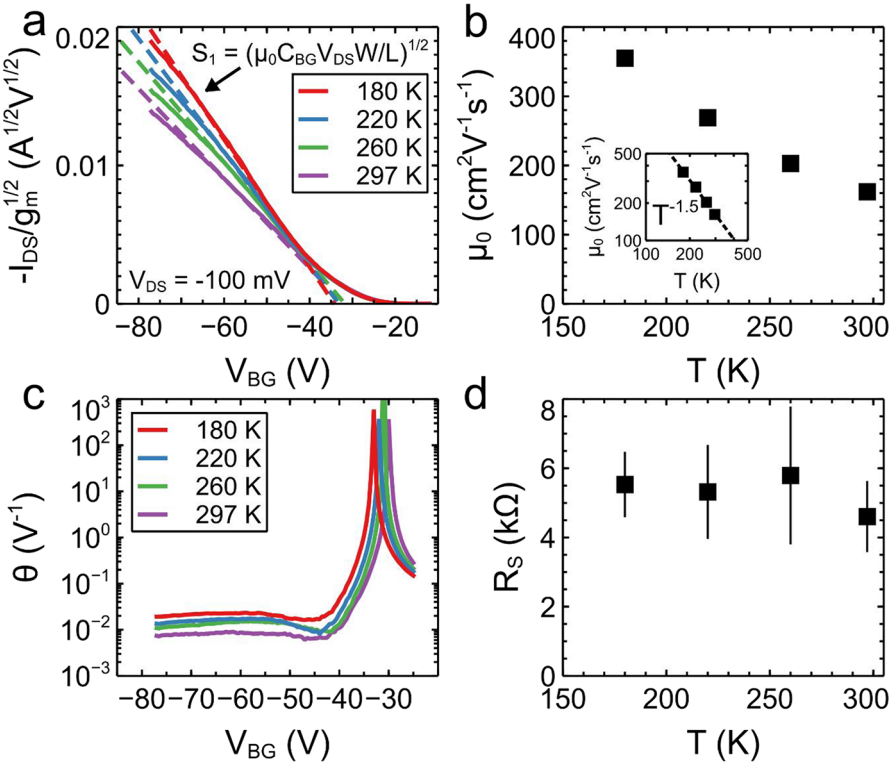

Figure 4. (a) *Y* function versus back-gate voltage plots of the data shown in Figure 3c. (b) Temperature dependence of the intrinsic mobility of the device determined using the *Y*-function method. The inset shows a power-law dependence of the intrinsic mobility on the temperature. (c) Mobility attenuation factor (θ) of the device at different temperatures. (d) Series resistance (R_S) at the contacts estimated from the *Y*-function method at different temperatures. The series resistance here includes the interface resistance (R_I) at the vdW contact and the parasitic resistance of p^+-MoS_2 between the vdW contact and metal electrode, as shown in Figure 1.

and confirmed that the hole mobility is nearly independent of the gate voltage down to 180 K (see section 6 of the Supporting Information). With the presence of a gate-independent R_S at the contacts, the internal drain/source voltage (V_{DS}) applied on the WSe_2 channel is reduced to $V_{DS} - 2I_{DS}R_S$ and the back-gate voltage (V_{BG}) seen by the channel is correspondingly reduced to $V_{BG} - I_{DS}R_S$. The hole current of our back-gated WSe_2 devices in the on state ($|V_{BG} - V_{TH}| \gg V_{DS}$) can then be modeled as

$$I_{DS} = -\frac{W}{L}C_{BG}\frac{\mu_0}{1-\theta(V_{BG}-V_{TH})}(V_{BG}-V_{TH})V_{DS} \quad (2)$$

where θ and μ_0 are the mobility attenuation factor and intrinsic mobility, respectively.[4,35,57,58]

Here, μ_0 and θ are the only parameters in eq 2 that are not known from the device and experimental conditions. We first estimate the mobility from the *Y* function defined as

$$Y \equiv -\frac{I_{DS}}{\sqrt{g_m}} = \left(-\frac{W}{L}C_{BG}\mu_0 V_{DS}\right)^{1/2}(V_{BG}-V_{TH})V_{DS} \quad (3)$$

to eliminate θ in the expression, where $g_m \equiv \partial I_{DS}/\partial V_{BG}$ is the trans conductance of the WSe_2 FET. Figure 4a shows the *Y* function versus back-gate voltage for the data shown in Figure 3c. The intrinsic mobility (μ_0) and threshold voltage (V_{TH}) can be directly determined from the slope (S_1) of the linear fits to the *Y* function: $S_1 = (\mu_0 C_{BG} V_{BG} W/L)^{1/2}$, and $V_{TH} = x$ intercept. As shown in Figure 4b, the estimated μ_0 increases from ~160 $cm^2\ V^{-1}\ s^{-1}$ at room temperature to ~360 $cm^2\ V^{-1}\ s^{-1}$ at 180 K, following a $\mu \sim T^{-\gamma}$ dependence with $\gamma \approx 1.5$, in good agreement with phonon-limited mobility.[36,59−61]

Once μ_0 and V_{TH} are known, the mobility attenuation factor can be determined from

$$\theta = \left[-\frac{I_{DS}}{g_m(V_{BG}-V_{TH})} + 1\right]/(V_{BG}-V_{TH}) \quad (4)$$

Figure 4c shows θ as a function of V_{BG} for the WSe_2 device, from which the series resistance (R_S) can be estimated by $\theta = \theta_0 + 2R_S\ \mu_0 C_{BG} W/L$. Here θ_0 is the intrinsic mobility attenuation factor of the channel, which could be introduced by scattering mechanisms such as remote phonon scattering and surface roughness scattering. Because the Hall mobility of our WSe_2 devices fabricated on ultraclean and ultraflat hBN substrates is nearly independent of the carrier density (gate voltage), θ_0 is expected to be negligible and consequently $\theta \approx 2R_S\mu_0 C_{BG} W/L$. As shown in Figure 4d, the series resistance at each contact is estimated to be $R_S \approx 5\ k\Omega$ from the strong inversion region of the mobility attenuation factor. Note that the series resistance consists of the interface resistance of the p^+-MoS_2/WSe_2 vdW contact (R_I) and a parasitic resistance (R_P) of the excess p^+-MoS_2 between the vdW contact and metal interconnect ($R_S = R_I + R_P$). The interface resistance (i.e., the true contact resistance of the vdW junction) is likely to be much smaller than ~5 $k\Omega$ because the series resistance at the contacts is dominated by the parasitic resistance of excess p^+-MoS_2 between the vdW contact and metal interconnect as discussed below. After the estimated parasitic resistance due to excess p^+-MoS_2 beyond the drain/source vdW contacts is subtracted, the transfer characteristics exhibit a linear depend-

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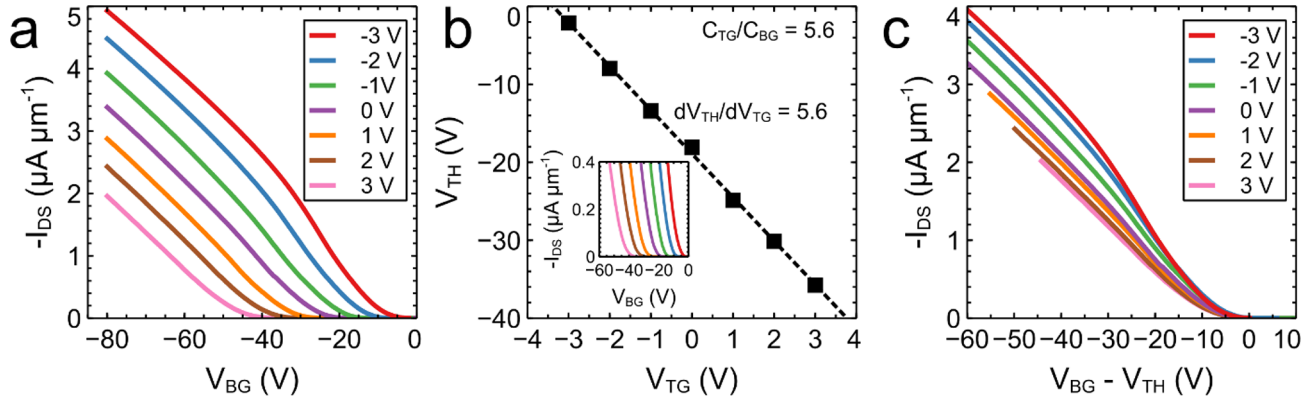

Figure 5. (a) Back-gated transfer characteristics of a WSe_2 FET with p^+-MoS_2 bottom contacts measured at different top-gate voltages. (b) Threshold voltage of the back-gated transfer characteristics plotted as a function of the top-gate voltage. The threshold voltage is determined by linear extrapolation of the transfer characteristics near the threshold voltage, as shown in the inset. (c) Back-gated transfer characteristics in part a replotted as a function of the gate overdrive ($V_{BG} - V_{TH}$).

ence on the back-gate voltage and the two-terminal field-effect mobility approaches the intrinsic mobility extracted from the *Y*-function method, suggesting that R_I is negligibly small compared to the channel resistance and R_P (see section 7 of the Supporting Information). Because the parasitic resistance of the excess p^+-MoS_2 dominates the series resistance extracted from the *Y*-function method, it is not possible to quantitatively determine the actual contact resistance of the p^+-MoS_2/WSe_2 vdW contacts. This finding is also in good agreement with the back-gated WSe_2 device with the p^+-MoS_2 bottom contact as the source shown in Figure S1, which exhibits a high two-terminal mobility of ~200 $cm^2 V^{-1} s^{-1}$. It is worth pointing out that the *Y*-function method is ideally suited for extracting the series resistance at the contacts from the back-gated transfer characteristics in our bottom-contacted WSe_2 FETs because the vdW contact region is not tunable by the back gate because of screening by the bottom contacts.

The dual-gated FET structure offers an additional knob for tuning the device properties. Specifically, back-gated device characteristics measured at different top-gate voltages reveal the electrostatic doping effects of the contact regions on the device performance, which can be used to further distinguish between the accumulation-type ohmic and Schottky contacts. Figure 5a presents back-gated transfer characteristics of a dual-gated WSe_2 FET with p^+-MoS_2 bottom contacts measured at different top-gate voltages ranging from −3 to +3 V. As the top-gate voltage (V_{TG}) is stepped from −3 to +3 V, the threshold voltage (V_{TH}) shifts linearly in the negative direction at a rate of $V_{TH}/V_{TG} \approx 5.6$, as shown in Figure 5b. The rate of threshold voltage shift is in excellent agreement with the top-gate-to-back-gate capacitance ratio, as expected from electrostatic modulation of the channel carriers by both the top and back gates (see section 8 of the Supporting Information). Because a positive (negative) top-gate voltage depletes (induces) holes in the channel, a more (less) negative back-gate voltage is required to turn on the device. However, different from the back gate, which is screened by the bottom contacts, the top gate in our dual-gated WSe_2 device modulates both the channel and contact regions. For instance, a positive top-gate voltage of +3 V is expected to deplete ~1.2×10^{12} cm^{-2} holes out of WSe_2 in both the channel and drain/source contact regions. Unlike in the channel region, the top-gate-induced depletion (or accumulation) of carriers in the contact regions cannot be compensated for by the back gate because of screening by the bottom contacts. In particular, the depletion of holes induced by a positive top-gate voltage would lead to qualitatively different behavior in devices with accumulation-type ohmic and Schottky contacts. If the contacts are of the accumulation type with a sufficiently high concentration of holes on the WSe_2 side of the contacts, the contacts may still remain ohmic even with a positive top-gate voltage. On the other hand, if a positive SB is present at the contacts, application of a positive top-gate voltage would further increase the depletion width of the SB, leading to a rapid increase of the contact resistance and subsequently a drastic reduction of the drain/source current. As shown in Figure 5c, the drain/source current (I_{DS}) as a function of the gate overdrive ($V_{BG} - V_{TH}$) marginally decreases by ~15% at $V_{BG} - V_{TH} = 50$ V as the top-gate voltage increases from zero to +3 V, which can be attributed to the slight increase of the sheet resistance of WSe_2 at the vdW contacts. Conversely, a negative top-gate voltage induces additional holes on the WSe_2 side and the vdW contacts and consequently decreases the sheet resistance of WSe_2 in the contact regions, leading to a slight increase of the drain/source current. These results are consistent with our theoretical modeling, which shows a significant areal density of at least 4×10^{12} cm^{-2} accumulated holes on the WSe_2 side of the p^+-MoS_2/WSe_2 junction and a vanishingly thin (~1 nm) space-charge region on the p^+-MoS_2 side of the contact (which resembles a surface-charge layer on the metal side of a metal/semiconductor junction; see section 4 of the Supporting Information). Therefore, our combined experimental and theoretical results provide compelling evidence that the p^+-MoS_2/WSe_2 contact behaves as an accumulation-type metal/semiconductor ohmic contact. Qualitatively similar behavior is observed in another dual-gated WSe_2 FET with a thinner WSe_2 channel and similar p^+-MoS_2 contacts (see section 9 of the Supporting Information). By stark contrast, back-gated transfer characteristics of otherwise similar dual-gated WSe_2 FETs with Pt bottom contacts exhibited a negligibly small current at $V_{TG} = 0$, which was attributed to the prohibitively large contact resistance due to the presence of a significant SB.[25] In order to reduce the contact resistance and enable efficient injection of holes at the Pt/WSe_2 contacts, a significant negative top-gate voltage was required to overcome the SB and turn on the device.[25]

In order to further verify that the relatively weak dependence of the back-gated transfer characteristics on the top-gate

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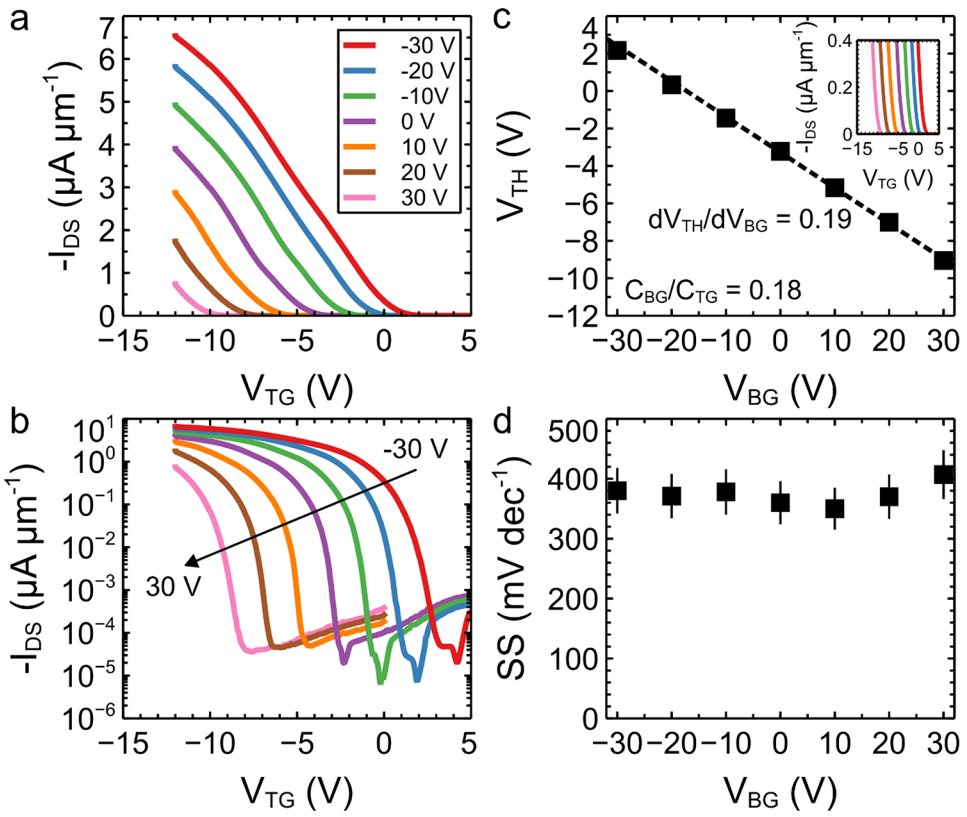

Figure 6. Top-gated transfer characteristics of the device in Figure 5 measured at different back-gate voltages plotted on linear (a) and semilogarithmic (b) scales. (c) Threshold voltage of the top-gated transfer characteristics as a function of the back-gate voltage. The threshold voltage is determined by linear extrapolation of the transfer characteristics near the threshold voltage, as shown in the inset. (d) SS of the top-gated transfer characteristics measured at different back-gate voltages.

voltage is due to accumulation-type ohmic contacts, it is important to rule out other possibilities, particularly the edge-injection scenario. On the basis of a two-trajectory current-injection model for 2D semiconductor FETs, carriers can be injected from the source contact to the channel in two possible trajectories: (i) carriers are vertically injected from the source contact to the channel material in direct contact with the source material and subsequently driven to the channel; (ii) carriers are laterally injected from the source-contact edge to the channel.[62] These two different injection mechanisms are expected to manifest differently in our dual-gated WSe_2 FETs with bottom contacts. If carriers are primarily injected via the first trajectory, the back-gated transfer characteristics should weakly depend on the top-gate voltage in the case of accumulation-type ohmic contacts so long as the areal density of the accumulated carriers at the contacts is substantially larger than that from the electrostatic modulation by the top gate but strongly depend on the top-gate voltage in the case of Schottky contacts. On the other hand, if the carriers are primarily injected via the second trajectory, the back-gated transfer characteristics are expected to be insensitive to the top-gate voltage for both accumulation-type and Schottky contacts. To rule out edge injection (the second mechanism) as a possible cause of the relatively weak dependence of the back-gated transfer characteristics on the top-gate voltage in our WSe_2 FETs with p^+-MoS_2 bottom contacts, we have also investigated dual-gated WSe_2 FETs with p^+-WSe_2 bottom contacts, where a small positive SB is known to be present. By sharp contrast, the back-gated transfer characteristics of WSe_2 FETs with p^+-WSe_2 bottom contacts exhibit a strong dependence on the top-gate voltage, which is similar to dual-gated WSe_2 with Pt bottom contacts[25] (see section 10 of the Supporting Information). This finding indicates that the carriers in our WSe_2 devices with vdW bottom contacts are primarily injected vertically through the vdW contact from the source electrode to the channel material and therefore confirms that the contacts between nearly intrinsic WSe_2 and p^+-MoS_2 are accumulation-type ohmic contacts.

Because p^+-MoS_2 and p^+-WSe_2 have nominally the same doping concentration and very similar electronic structures, the qualitatively different nature of the contacts can only be attributed to the higher work function of p^+-MoS_2 than that of p^+-WSe_2, as confirmed by theoretical modeling (see section 4 of the Supporting Information). This result strongly suggests that the SBH in the 2D/2D vdW contacts sensitively depends on the work function of the contact metal and Fermi-level pinning is nearly absent. By contrast, a finite positive SB is still present at the vdW contacts between predeposited/transferred Pt and a nearly intrinsic WSe_2 despite the fact that the work function of Pt is much larger than the ionization energy of WSe_2, indicating the presence of a Fermi-level pinning effect.[25,38]

Top-gated transfer characteristics measured at different back-gate voltages are also expected to behave differently for accumulation-type ohmic and Schottky contacts, especially in the subthreshold region. A sufficiently large negative (positive) back-gate voltage is expected to populate the channel with excess holes (electrons), which may lead to different switching mechanisms for accumulation-type ohmic and Schottky contacts.[25] Parts a and b of Figure 6 show the top-gated

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transfer characteristics of the WSe_2 device as V_{BG} is stepped from −30 to +30 V on linear and semilogarithmic scales, respectively, where a negative (positive) V_{BG} shifts V_{TH} positively (negatively) due to the dual gating of channel.

As shown in Figure 6c, the threshold voltage (V_{TH}) shifts linearly with V_{BG} in the negative direction at a rate of $V_{TH}/V_{BG} \approx 0.19$, which is consistent with the back-gate-to-top-gate capacitance ratio. At $V_{BG} = -30$ V, the on/off switching occurs at a positive $V_{TH} \approx 2$ V because a positive top gate is needed to deplete the excess holes induced by the negative V_{BG} in the channel to "turn off" the device. Because the back-gate electric field is screened by the bottom contacts and unable to induce excess holes in WSe_2 at the contacts, the on/off switching mechanism in the top-gated transfer characteristics at $V_{BG} = -30$ V is determined by the nature of the contacts, depending on whether they are Schottky or accumulation-type ohmic contacts. For WSe_2 FETs with Schottky contacts, the on/off switching occurs at the contact regions because of the lower hole density of WSe_2 in the contact region than in the channel region, which would consequently lead to the degradation of SS (or reduced switching sharpness) in comparison with the SS resulting from the channel on/off switching.[49] By contrast, the on/off switching for WSe_2 FETs with accumulation-type ohmic contacts is expected to be limited by the thermionic emission of carriers over the channel barrier as long as the accumulated holes are only partially depleted by the positive top-gate voltage at the threshold voltage. At $V_{BG} = +30$ V, the on/off switching occurs at a large negative $V_{TH} \approx -10$ V, which can be attributed to the accumulation of excess electrons in the channel induced by the positive V_{BG}. In this case, the contact regions are electrostatically p-doped by the negative top-gate voltage in the subthreshold region, and therefore the SS is primarily determined by the thermionic emission over the channel barrier for both Schottky and accumulation-type ohmic contacts. As a result, the SS of WSe_2 FETs with accumulation-type ohmic contacts is expected to be nearly independent of the back-gate voltage so long as the contact regions are accumulated with a sufficiently high density of holes. On the other hand, the SS of WSe_2 FETs with Schottky contacts is expected to be substantially larger at $V_{BG} = -30$ V than at $V_{BG} = +30$ V.

As shown in Figure 6d, the SS extracted from Figure 6b is nearly independent of the back-gate voltage, indicating that the SS is determined by the thermionic emission over the channel barrier for the entire back-gate voltage range between −30 and +30 V and therefore that the p^+-MoS_2/WSe_2 contact is accumulation-type. Back-gate independence of the SS in the top-gated transfer characteristics is confirmed by another WSe_2 FET with p^+-MoS_2 bottom contacts (see section 11 of the Supporting Information). By stark contrast, the SS extracted from the top-gated transfer characteristics of dual-gated WSe_2 FETs with p^+-WSe_2 bottom contacts increases by more than a factor of 4 as the back-gate voltage changes from $V_{BG} = 10$ V to $V_{BG} = -30$ V, which is characteristic of Schottky contacts (see section 12 of the Supporting Information). This result provides further evidence that the p^+-MoS_2/WSe_2 vdW contact is of the accumulation type and free of a SB. As a result, holes can be effectively injected from the p^+-MoS_2 source to the nearly intrinsic WSe_2 channel even when the accumulated holes on the WSe_2 side of the contacts are partially depleted by a positive top-gate voltage.

The accumulation-type vdW ohmic contacts demonstrated in this study are expected to have significant implications for the practical application of 2D semiconductor nanosheets in high-performance flexible electronics. Lowering the SB and increasing the carrier concentration in the contact regions of 2D semiconductor nanosheet-based FETs have been proven to be two of the most effective approaches to reducing their contact resistance and enhancing their device performance.[36,37,49,63] We envision that elimination of the SB using accumulation-type ohmic contacts in conjunction with proper doping could achieve low contact resistance in 2D semiconductor nanosheet-based FETs even when their lateral dimensions are aggressively downscaled, which may lead to the development of commercial 2D semiconductor nanosheet-based high-performance electronics.

CONCLUSIONS

In conclusion, we fabricated dual-gated FETs by vdW assembly of an intrinsic WSe_2 nanosheet-based channel on top of p^+-MoS_2 bottom contacts to demonstrate the formation of accumulation-type ohmic contacts free of a SB. Fundamentally different from Schottky contacts, the accumulation-type ohmic contacts demonstrated in this study exhibit ohmic behavior and low contact resistance without the need of doping or electrostatically gating the channel material in the drain/source contact regions. We attribute the accumulation-type ohmic contacts to the ideal metal/semiconductor interface of a vdW junction consisting of 2D materials with similar crystalline and electronic structures. Such an ideal metal/semiconductor contact is free of Fermi-level pinning effects. Therefore, its SBH is fundamentally determined by the work function of the metal and ionization energy of the semiconductor for holes, as dictated by the Schottky−Mott rule. Because p^+-MoS_2 behaves as an 2D metal and its work function is slightly larger than the ionization energy of WSe_2, a strong hole accumulation region develops on the WSe_2 side of the vdW contact, as predicted by the Schottky−Mott rule. Contrary to Schottky contacts, accumulation-type ohmic contacts are completely free of a SB. The diminishing SBH at the vdW contacts demonstrated in this study is expected to lead to low contact resistivity, which, in turn, enables low contact resistance in 2D-semiconductor-based FETs even when the contact length is aggressively down-scaled. The 2D vdW contacts with negligible Fermi-level pinning can also be used as the baseline to study the mechanism of Fermi-level pinning at the metal/2D semiconductor interface, for which remains a key challenge to achieve low-resistance ohmic contacts in 2D-semiconductor-based nanoscale electronic devices. Various possible Fermi-level pinning factors can be controllably introduced to quantitatively understand their roles in Fermi-level pinning, which may be a topic for future research.

METHODS

To fabricate dual-gated WSe_2 FETs with p^+-MoS_2 bottom contacts, 10−30-nm-thick hBN flakes were first exfoliated on degenerately doped Si with 280 nm of thermal oxide by a mechanical exfoliation method. Next, mechanically exfoliated pairs of p^+-MoS_2 flakes (6−12 nm thick) containing 0.5% Nb were mechanically exfoliated on SiO_2/Si substrates and then picked up from the SiO_2/Si substrates and placed on the hBN substrates by a dry transfer method using a polycarbonate/poly(dimethylsiloxane) stamp on a glass microscope slide. Subsequently, a 6−12-nm-thick intrinsic WSe_2 channel was stacked on top of a pair of p-doped MoS_2 drain/source electrodes also by the dry transfer method, followed by dry transferring another hBN flake on top to cover the WSe_2 channel and parts of the drain/source contacts serving as a top-gate dielectric. Finally, the metal top gate

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and interconnects to the p-doped MoS_2 drain/source electrodes, consisting of 10 nm Ti and 40 nm Au, were fabricated by electron-beam lithography and electron-beam-assisted metal deposition. A slight overlap between the metal top-gate electrode and the drain/source contacts was assured to enable electrostatic modulation of WSe_2 in both the channel and drain/source regions by the top gate.

Thin flakes of intrinsic WSe_2, p^+-MoS_2, p^+-WSe_2, and hBN were all produced by mechanical exfoliation of bulk crystals and identified using optical microscopy and non-contact-mode atomic force microscopy (Park-Systems XE-70). Bulk crystals of intrinsic WSe_2, p^+-MoS_2, and p^+-WSe_2 were synthesized by chemical vapor transport by adding 0.5% Nb as a hole dopant.[36,42]

The electrical properties of the devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station under high vacuum (1×10^{-6} Torr) or in a Quantum Design Physical Property Measurement System.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsanm.1c01138.

Comparison of WSe_2 FETs with p^+-MoS_2 and p^+-WSe_2 as bottom and top contacts, SBH extraction, theoretical modeling of the vdW heterojunction between intrinsic WSe_2 and p^+-MoS_2/p^+-WSe_2, ionization energy of p^+-MoS_2 and p^+-WSe_2 determined by XPS, Hall mobility of WSe_2 as a function of the hole concentration, parasitic resistance of excess p^+-MoS_2, calculation of the top- and bottom-gate capacitances, and additional WSe_2 FETs with p^+-MoS_2/p^+-WSe_2 bottom contacts (PDF)

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Author Contributions

M.R.K., J.Y., and D.G.M. worked on the synthesis and basic characterization of bulk crystals. P.-Y.C. carried out theoretical modeling. K.A., U.R., A.B., and H.-J.C. fabricated devices. K.A. and U.R. performed the electrical measurements. K.A., U.R., and Z.Z. analyzed the data. K.A. and Z.Z. discussed the results and wrote the manuscript, with input from all authors. Z.Z. supervised the project.

Notes

The authors declare no competing financial interest.

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