Variation-Aware Inter-Device Matching in Silicon Photonic Microring Resonator Demultiplexers

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***Abstract*—We present a design optimization framework to enhance inter-device matching in silicon photonic microring resonator (MR) demultiplexers under correlated fabrication process variations. Results indicate considerable improvement in channel spacing accuracy in a multi-channel demultiplexer even when the MRs are positioned 300 μm apart on a chip.**

I. Introduction

Dense wavelength-division multiplexing (DWDM) is a common solution to boost the bandwidth performance in silicon photonic (SiPh) integrated circuits, where microring resonator (MR) filters have been widely employed for optical channel (wavelength) demultiplexing. Such densely integrated circuits are possible due to the high refractive-index contrast in silicon-on-insulator (SOI) platforms. Nevertheless, the same contrast has made SiPh devices susceptible to inevitable fabrication process variations (PVs), where nanometer(nm)-scale deviations in the critical dimensions of a device can considerably impact its functionality [1]. For example, a width and thickness variation of only 1 nm in an MR filter can shift its wavelength response by several nms [2]. Such a wavelength drift calls for active tuning (compensation) for inter-device matching in today's DWDM systems with a typical channel spacing of <1 nm. However, active compensation is complex and imposes area and power overheads (e.g., $\approx$10°C for 1 nm shift) [2], necessitating efficient design solutions to minimize the effect of different PVs at the design time in a fabless ecosystem.

In this paper, we propose a design optimization framework to improve inter-device matching (i.e., channel spacing accuracy) in MR-based wavelength demultiplexers under different PVs. In particular, our optimization framework considers actual layout information and fundamental variations in SOI thickness and waveguide width present on different length scales (i.e., correlations in variations) [3]. By minimizing deviations in the channel spacing in MR-based demultiplexers, we can compensate for wavelength shifts by collectively tuning all the MRs, hence simplifying the tuning and improving its efficiency. Our fabrication and simulation results demonstrate the promise of our variation-aware optimization solution: using a case study of a wavelength demultiplexer with two MRs, we indicate channel spacing accuracy within 0.2–0.5 nm even when the MRs are positioned far apart (300 μm) on a chip.

II. Variation-Aware Design Optimization

We start by formulating the variation-aware optimization problem in the two-channel MR-based demultiplexer case study in Fig. 1. The channel spacing (c_s) is the frequency space between the two MRs' consecutive resonant wavelengths (λ_R): $c_s = |\lambda_{R2} - \lambda_{R1}|$, where $\lambda_{R2}>\lambda_{R1}$. The resonant wavelength in an MR is determined by several geometric parameters, including the waveguide width, thickness, and radius, slight variations in which will result in a resonant wavelength shift in the MR [4]. Here, we focus on fundamental PVs in the SOI thickness and the waveguide width [2], which are present on different length scales and are correlated [3], necessitating one to incorporate the actual layout information into the variability analysis. As a result, we consider MR layout design parameters that will be affected by these variations as well as the distance between the two MRs in our variation-aware design optimization solution for the demultiplexer in Fig. 1.

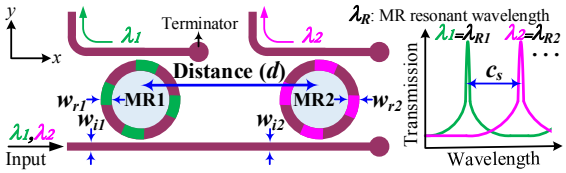

Fig. 1. A two-channel MR-based wavelength demultiplexer with two MRs placed at a distance d and with a channel spacing c_s. Here, w_i and w_r are the input/drop waveguide width and the MR waveguide width, respectively.

Given $\nu_t(x,y)$ and $\nu_w(x,y)$ to be the variations in the thickness and width at a position (x,y) on a die (same $\nu_{t/w}$ in the input/drop and MR waveguide), we model the resonant wavelength shift ($\Delta\lambda_R$) in an MR located at (x,y) as:

$$\Delta\lambda_R(x,y) = \frac{\partial\lambda_R}{\partial_t}\nu_t(x,y) + \left(\frac{\partial\lambda_R}{\partial_{w_i}} + \frac{\partial\lambda_R}{\partial_{w_r}}\right)\nu_w(x,y), \quad (1)$$

where $\frac{\partial\lambda_R}{\partial_t}$ ($\frac{\partial\lambda_R}{\partial_{w_{i/r}}}$) is the rate of change in the MR resonant wavelength with respect to the variations in the SOI thickness (waveguide width). Note that while we consider SOI thickness variations, we do not consider the thickness as a design parameter as it is limited by the hosting wafer and cannot be optimized during the design time. Hence, we study the impact of input/drop waveguide width (w_i) and MR waveguide width (w_r) on the effective index and hence λ_R in the MR (see Fig. 1). Given $\Delta\lambda_R$, we can model the channel spacing in our two-channel MR-based demultiplexer under PVs (c_s') as $c_s' = c_s + \Delta c_s$. Here, Δc_s denotes changes in the channel spacing and can be calculated as $\Delta c_s = \Delta\lambda_{R2}(x+d,y) - \Delta\lambda_{R1}(x,y)$ (see Fig. 1), where $\Delta\lambda_{R1/R2}$ can assume a blue or a red shift.

$$\min\Delta \quad c_s = \Delta\lambda_{R2}(x+d,y) - \Delta\lambda_{R1}(x,y) \quad (2)$$
$$\text{s.t.} \quad \kappa \geq \kappa_m \;\;,\;\; Q \geq Q_m \;\;,\;\; w_{i/w} \in [w_l, w_u].$$

Considering c_s' and different variations, the channel spacing accuracy can be improved iff we minimize Δc_s during design

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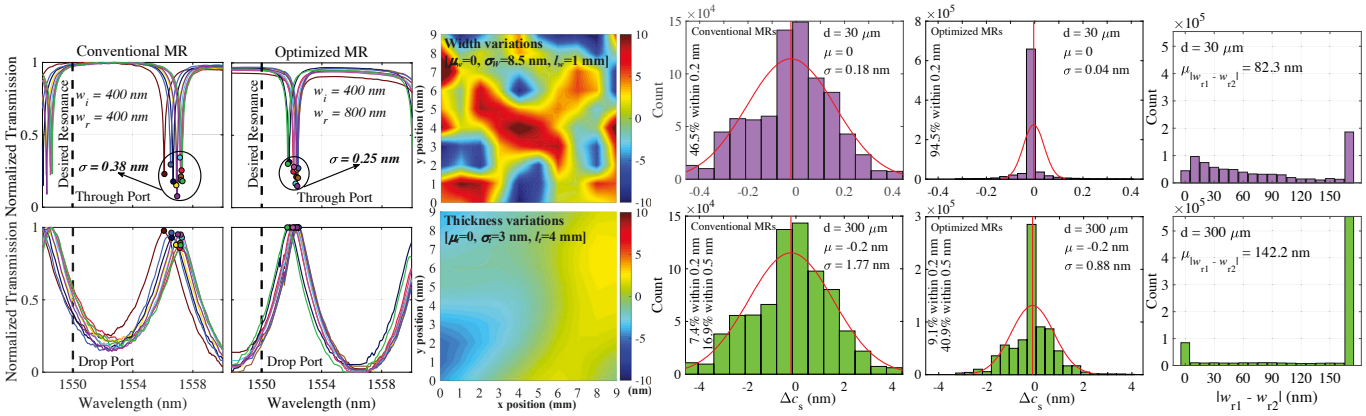

(a) Fabrication results (b) Variation maps (c) Channel spacing variations (Δc_s) (d) Width difference

Fig. 2. (a) Measurement results for fabricated conventional (ten) and optimized (ten) MRs; (b) Correlated width and SOI thickness variation maps; (c) Statistical analysis of channel spacing variations in the demultiplexer in Fig. 1 when using conventional and optimized MRs by applying (2) and with different distances (d) between the two MRs; and, (d) Difference between MR1 and MR2 waveguide widths ($w_{r1/r2}$) optimized together to minimize Δc_s in Fig. 2c.

time. Therefore, we can formulate the optimization problem as (2), in which κ_m and Q_m are, respectively, the minimum coupling and Q-factor in MRs that can be determined by the designer. Moreover, w_l and w_u are, respectively, the lower and upper bound of the input/drop and MR waveguide width. Considering (1) and (2) and leveraging a fast design exploration technique proposed in [4], our optimization engine explores the design space of each MR (i.e., $w_{i1/r1}$ and $w_{i2/r2}$ in Fig. 1) to minimize Δc_s while satisfying Q-factor and coupling efficiency constraints in the demultiplexer.

III. Results and Discussion

Employing different variation maps (see below), we applied our optimization method to the design of a TE-polarized MR with a radius, gap, and central resonant wavelength of 10 μm, 100 nm, and 1550 nm, respectively. Our optimization found w_i and w_r to be, respectively, 400 nm and 800 nm for an SOI thickness of 220 nm. We fabricated this optimized MR and also a conventional MR with $w_i = w_r = 400$ nm using electron beam lithography (EBeam) where ten identical copies of each MR were located at different locations, but with same distances, on a small 1.5×0.6 mm^2 chip. Fig. 2a indicates the drop and through port responses of the conventional MR and our optimized MR. As can be seen, the resonant peaks (ten in total) are not only closer to the desired resonant wavelength (1550 nm) in the optimized MRs, they are also closely matched with a standard deviation (σ) of 0.25 nm. According to Fig. 2a, one may argue that the inter-device matching in our optimized MRs is not significantly better than that in the conventional MRs. This is indeed due to the small size of the chip in which similar width and thickness variations are present on a small length scale. Nevertheless, even in such a small chip, our optimization has realized better inter-device matching among the optimized MRs (>50%, compare σ values in Fig. 2a).

Considering Fig. 1 and our objective in (2), our optimization takes correlated thickness and width variation maps and positioning of the MRs (i.e., d), to optimize design parameters in MR1 and MR2 (i.e., $w_{i1/r1}$ and $w_{i2/r2}$) while applying the limit $\Delta\lambda_{R1} \to 0$ and $\Delta\lambda_{R2} \to 0$, or $\Delta\lambda_{R2} \to \Delta\lambda_{R1}$, both minimizing Δc_s (see (1) and (2)). First, we generate correlated width (subscript w) and thickness (subscript t) variation maps (see Fig. 2b) with mean (μ_w and μ_t), standard deviation (σ_w and σ_t), and correlation length (l_w and l_t) of $\mu_w = \mu_t = 0$, $\sigma_w = 8.5$ nm, $\sigma_t = 3$ nm, $l_w = 1$ mm, and $l_t = 4$ mm [3], [5]. Note that such statistics can be provided by the foundry and our optimization is independent of these assumed values. Leveraging these maps, we apply our optimization to find optimum design parameters in MR1 and MR2 uniformly positioned at every location on the chip, where we statistically analyze the channel spacing variations (Δc_s) in the demultiplexer while considering the MRs to be in proximity ($d = 30$ μm) and also far apart ($d = 300$ μm). For simplicity, we considered $w_{i1} = w_{i2} = 400$ nm, and let the optimization find $w_{r1/r2}$ with $w_l = 400$ nm and $w_u = 900$ nm (see (2)). Fig. 2c indicates Δc_s for our demultiplexer with conventional (no optimization) and optimized MRs when $d = 30$ μm and $d = 300$ μm and for 8×10^5 design samples. As can be seen, our design optimization can effectively explore and optimize the design of each MR to minimize Δc_s. Fig. 2d indicates the difference between w_{r1} and w_{r2} (see Fig. 1) optimized together to minimize Δc_s in all the design samples. When $d = 30$ μm, both MRs experience variations on a smaller length scale, hence intuitively matching is already higher and the resulting $|w_{r1} - w_{r2}|$ is smaller. However, when $d = 300$ μm, MRs experience much different variations and on a larger length scale, hence matching is more challenging and the resulting $|w_{r1} - w_{r2}|$ increases (see Fig. 2d). Yet, as shown in Fig. 2c, our optimization has successfully maintained the channel spacing accuracy in >94% (>40%) of design samples within 0.2 nm (0.5 nm) when $d = 30$ μm ($d = 300$ μm).

In summary, our proposed optimization solution enables efficient inter-device matching even for devices that are placed far apart on a chip, hence considerably simplifying the device placement and routing in silicon photonic integrated circuits.

References

[1] M. Nikdast *et al.*, *IEEE JLT*, vol. 34, no. 16, pp. 3682–3695, 2016.
[2] W. Bogaerts *et al.*, *IEEE JSTQE*, vol. 25, no. 5, pp. 1–13, 2019.
[3] Z. Lu *et al.*, *Optics express*, vol. 25, no. 9, pp. 9712–9733, 2017.
[4] A. Mirza *et al.*, in *ACM/IEEE DATE*, 2020.
[5] Y. Xing *et al.*, in *IEEE GFP*, 2018, pp. 91–92.