A Wideband Isolated Real-to-Complex Impedance Transforming Uniplanar Microstrip Line Balun for Push–Pull Power Amplifier

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***Abstract*— In this article, a three-port uniplanar microstrip line balun is proposed to transform the balanced complex load termination to 50-Ω unbalanced port impedance. The proposed device is designed based on a symmetric four-port network with an open-ended transmission line inserted between branch lines in the middle of structure. To improve the isolation and match the complex termination, a resistive network is proposed and inserted between the two balanced ports. In addition, the theoretical analysis is carried out for the even and odd mode circuits to expand the bandwidth of the proposed real–complex impedance transforming balun. With the proposed design theory, the impedance trajectory follower splitting and combining baluns are designed for wideband push–pull power amplifier (PPPA). To verify the design concept, first, a real–complex impedance transforming uniplanar microstrip line balun is designed and characterized at 1 GHz. Then, a prototype for the wideband PPPA with impedance trajectory follower microstrip baluns is designed, fabricated, and validated in experiment. For the proposed balun, the simulated and measured results agree well with each other to prove the design concept. From the experimental results, the PPPA with the proposed balun shows a gain of 10.2–12.2 dB, output power of 42.7–44.7 dBm, and a drain efficiency of 59.8%–74.6% within the frequency range of 1.8–2.7 GHz.**

***Index Terms*— Isolation, microstrip line balun, power amplifier, push–pull, real–complex impedance transforming, wideband.**

I. Introduction

BALUN is a three-port device to convert a single-ended signal into the double-ended signal and vice versa. It is mainly applied in push–pull power amplifier (PPPA) [1]–[12], balanced mixer [13], and dipole antenna feeding [14], [15]. There are many types of balun, and the microstrip line-based baluns are categorized into Marchand balun, Wilkinson power divider balun, and branch line configuration, which are vastly investigated in previous literatures. The dual band/wideband modified Marchand balun are presented in [16]–[26], where the coupled line structures are applied to enhance the bandwidth. The strong coupling requires high precision fabrication process, and it features low isolation and causes mismatch at balanced ports. To resolve these issues, in [27], a Marchand balun with vertically installed structure is proposed to achieve good isolation and port impedance matching. The Wilkinson power divider baluns combine a Wilkinson power divider and a 180° phase shifter. In [28], a Wilkinson power divider balun is designed to achieve wideband and planar layout. However, the grounded stubs applied in the proposed device cause DC short and degrade the overall efficiency, especially for the PPPA design. Similarly, in [29], a lumped element metamaterial phase shifter is combined with Wilkinson power divider to increase the operating bandwidth of the balun. But the parasitic effect from lumped element causes performance degradation at higher frequencies. The branch line-based planar baluns are proposed in [30] and [31], and the corresponding wideband baluns are implemented using the SIW technology [32], multilayer PCB [33], and open coupled line [34]. But all of them did not consider the input impedance matching for balanced ports as well as isolation of the balanced ports. In [35] and [36], a balun with impedance transforming is proposed to match complex to complex impedance between unbalanced and balanced ports, and the additional impedance transformer is required to match to 50-Ω termination. The coupled line baluns are proposed in [37]–[39] to transform the unbalanced real port impedance to balanced real impedance. In all those designs, the balanced ports input matching and the isolation are not addressed. Overall, the conventional microstrip line baluns feature: 1) the balanced port and unbalanced ports must have same real impedance or real–real impedance transforming; 2) the isolation between balanced ports are not considered; 3) the impedance looking into balanced ports are not matched; and 4) multilayer designs cause challenges for planar integration and increase the cost for system-level integration.

Beyond the balanced port impedance matching and isolation, in RF/microwave circuits, we often deal with matching of complex-to-real impedances. For example, the optimum output or input impedance of high-power RF power devices

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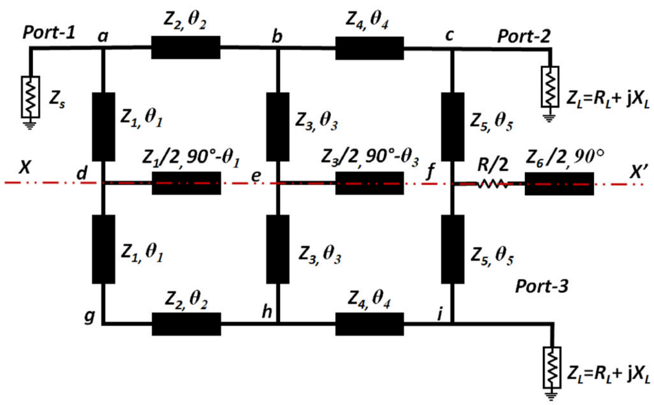


Fig. 1. Schematic of the proposed microstrip line balun.

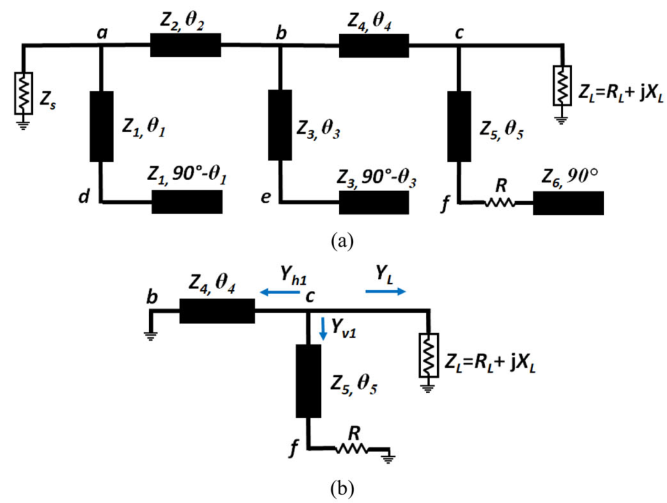


Fig. 2. (a) Even-mode circuit diagram. (b) Simplified even-mode circuit.

are low-valued complex impedance, and the antenna input impedance is tuned by surrounding obstacles to present a complex impedance for its feeding network. Therefore, to overcome the issues of conventional microstrip line baluns, a balun featuring real–complex impedance matching will greatly reduce the circuit size by obviating frequency sensitivity impedance transformer. In IMS 2019 [40], we presented a novel microstrip line-based uniplanar balun structure to transfer the balanced complex termination impedance to unbalanced 50 Ω. Our proposed balun features: 1) complex balanced load impedance is transformed to standard 50-Ω unbalanced impedance; 2) all three ports are matched ($S_{ii} = 0$, $i = 1$, 2, and 3); 3) more than 10-dB isolation between its balanced ports is obtained with novel resistivity network; 4) no short stubs are required in the circuit to avoid dc power loss; and 5) uniplanar structure of the proposed design enables easy integration with the RF power device. With the above-mentioned characteristics, in this article, the in-depth theoretical study is carried out to analyze the operating bandwidth of the proposed balun and provide optimum approach for wideband design. In addition, a novel PPPA with novel impedance trajectory follower splitting and combining balun is designed to connect the RF power transistors directly to the balanced ports of balun for enhancing the bandwidth and efficiency of conventional PPPAs, where the input and output impedance matching are required to transform the complex RF device impedances to balanced ports impedance of conventional balun.

This article is organized as follows. In Section II, we discuss the analysis of the balun and derive the design equations for wideband planar balun, and its trade-offs in the even and odd mode circuits are analyzed as well. Section III describes the design of PPPA with the proposed splitting and combining baluns, and the simulation and measurement of the prototypes are summarized in Section IV.

II. Real–Complex Microstrip Line Planar Balun Design

The schematic of the proposed microstrip planar balun is illustrated in Fig. 1. By treating the circuit as a four-port network with the open fourth port at node g, the even–odd mode method is applied to analyze it.

The governing equations for the balun follow the theory in [30] and [37], which are

$$\text{Even mode } T = 0 \tag{1}$$

$$\text{Odd mode } Z_{in} = 2Z_s \tag{2}$$

where T is the forward transmission and $Z_s = 50$ Ω. To achieve impedance matching for balanced ports, the additional equation must be satisfied [39]

$$S_{22e} = 0. \tag{3}$$

Here, $S_{22\mathrm{e}}$ is the reflection coefficient at port 2 under even mode excitation.

A. Even-Mode Circuit Analysis

Fig. 2(a) shows the even mode circuit, where the open stub (Z_1, $90° - \theta_1$) at node d combines with the transmission line (TL) (Z_1, θ_1) to present short at the node a. Similarly, the node b is shorted by stub with length $90° - \theta_3$ and TL with length θ_3. Here, the series 90° open-stub Z_6 provides short circuit for the resistor. Considering above, the equivalent simplified circuit is shown in Fig. 2(b). It is obvious that the short at node a will automatically satisfy the condition in (1). For the ease of analysis, all the impedances are converted into the admittances, and the load impedance $Z_L = R_L + jX_L$ is converted to admittance $Y_L = G_L + jB_L$.

From Fig. 2(b), the admittance looking into two branches are

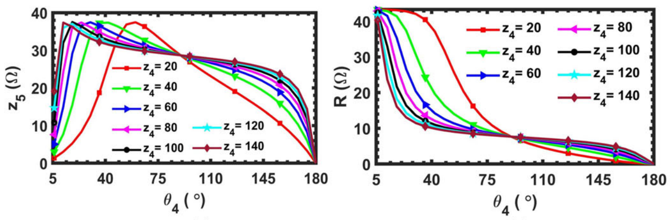
$$Y_{h1} = -jY_4 \cot\theta_4 \tag{4}$$

$$Y_{v1} = Y_5 \frac{G + jY_5 \tan\theta_5}{Y_5 + jG \tan\theta_5}. \tag{5}$$

Here, $G = 1/R$ and $Y_5 = 1/Z_5$. The real and imaginary parts of the Y_{v1} are given as

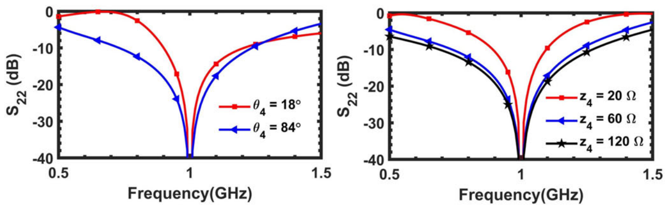
$$\mathrm{Re}[Y_{v1}] = \frac{2GY_5^2}{Y_5^2 + G^2 + (Y_5^2 - G^2)\cos(2\theta_5)} \tag{6}$$

$$\mathrm{Im}[Y_{v1}] = \frac{Y_5(Y_5^2 - G^2)\sin(2\theta_5)}{Y_5^2 + G^2 + (Y_5^2 - G^2)\cos(2\theta_5)}. \tag{7}$$



(a) (b)

Fig. 3. Calculated values of (a) Z_5 and (b) R for $\theta_5 = 30°$ and different values of θ_4 and Z_4.



(a) (b)

Fig. 4. (a) S_{22} for $\theta_4 = 18°$ and $\theta_4 = 84°$. (b) S_{22} for $Z_4 = 20\ \Omega$, $Z_4 = 60\ \Omega$, and $Z_4 = 120\ \Omega$.

In order to satisfy (3), at node c, the following equations are derived as:

$$\mathrm{Re}[Y_{v1}] = G_L \tag{8}$$

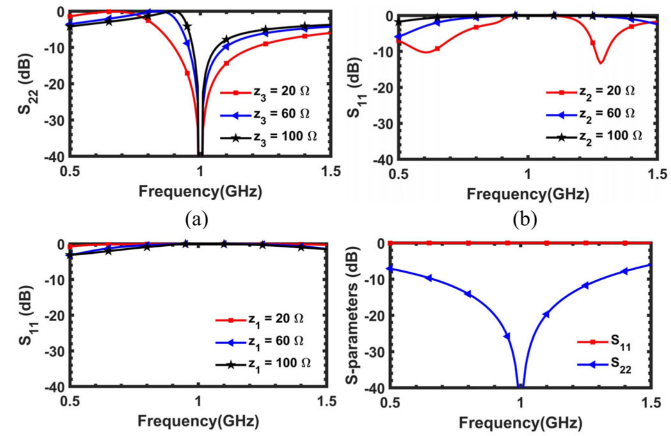
$$\mathrm{Im}[Y_{v1}] + \mathrm{Im}[Y_{h1}] = -B_L. \tag{9}$$

There are five unknown parameters (i.e., Y_4, Y_5, θ_4, θ_5, and G) in these two equations, and various sets of solutions exist to satisfy the conditions in (8) and (9). By limiting the characteristic impedance for each TL between 20 and 140 Ω, we can assume any three variables from the five unknowns and solve the rest two, which provides us the design freedom for configuring the proposed circuit. Since Z_6 does not contribute in (8) and (9), we can assume any value for it.

With the multiple variables, it is necessary to analyze all the design parameters that could provide wide operating bandwidth. To this end, we assume $Z_L = 10 - j15\ \Omega$ as an example, and the θ_5 is set to 30°. Fig. 3 shows all the possible solutions of Z_5, R, θ_4, and Z_4 that satisfy (8) and (9). From Fig. 3, with $Z_4 = 60\ \Omega$, we analyze two cases of $\theta_4 = 18°$ and $\theta_4 = 84°$, where the corresponding values for Z_5 are 29.15 and 29.27 Ω and for R are 35.31 and 8.11 Ω, respectively. With the ideal TL, the simulation results are plotted in Fig. 4(a), where the higher θ_4 support wide bandwidth.

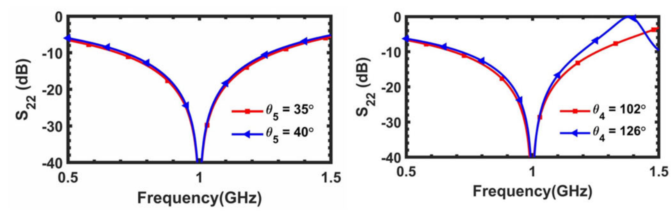
By observing Fig. 3(a) and (b), it is found that Z_5 and R are independent of Z_4 when $\theta_4 = 90°$, which is obvious as the 90° TL transfers the short to the open circuit. To evaluate the bandwidth, Fig. 4(b) plots S_{22} with different Z_4 under $\theta_4 = 90°$, and it concludes that higher Z_4 provides wide bandwidth.

In all the above analysis, we assume perfect short at node b [in Fig. 2(a)]. But the frequency sensitive TL will not present short across the band. Therefore, further analysis is carried out to evaluate the bandwidth varied by the all the TL sections left of the node b. Within the range of 20–100 Ω for Z_1, Z_2, and Z_3, Fig. 5 shows various plots of S-parameters across the frequency. From the analysis, the bandwidth decreases with the increase in Z_3 and Z_1 and increases with the higher Z_2.



(a) (b) (c) (d)

Fig. 5. (a) Variation of S_{22} with Z_3. (b) Variation of S_{11} with Z_2. (c) Variation of S_{22} with Z_1. (d) S-parameters for maximum bandwidth.



(a) (b)

Fig. 6. (a) S_{22} for $\theta_5 = 35°$ and $\theta_5 = 40°$. (b) S_{22} for $\theta_4 = 102°$ and $\theta_4 = 126°$.

Taking all the results into account, a circuit is designed with $\theta_5 = 30°$, $Z_5 = 28.92\ \Omega$, $\theta_4 = 84°$, $Z_4 = 140\ \Omega$, $Z_3 = 20\ \Omega$, $Z_2 = 140\ \Omega$, $Z_1 = 20\ \Omega$, and $R = 7.86\ \Omega$, and the simulated S-parameters are shown in Fig. 5(d), where 624-MHz bandwidth is achieved in the even mode for the load of $10 - j15$. Considering $Z_1/2$ and $Z_3/2$ in Fig. 1, the minimum impedance for Z_1 and Z_3 is 40 Ω, which causes bandwidth degradation from the above analysis. To see the effect of θ_5 further, we have considered two more cases of θ_5. Compared to the previous case of $\theta_5 = 30°$ in Fig. 5(d), Fig. 6(a) suggests as we increase θ_5 to 35° and 40° the bandwidth decreases. For some load impedances, the higher value of θ_5 might be the only possible solution for the realizable value of Z_5 which would reduce the even-mode bandwidth. Fig. 6(b) suggests if we use a value of θ_4 greater than 90°, bandwidth decreases to 569 MHz at $\theta_4 = 102°$ to 476 MHz at $\theta_4 = 126°$.

B. Odd-Mode Circuit Analysis

The odd-mode circuit is shown in Fig. 7. From Fig. 7(a), the admittance Y_{h2} and Y_{h3} are derived as

$$Y_{h2} = Y_L - jY_5 \cot\theta_5 \tag{10}$$

$$Y_{h3} = Y_4 \frac{Y_{h2} + jY_4 \tan\theta_4}{Y_4 + jY_{h2} \tan\theta_4}. \tag{11}$$

From the even-mode analysis, the values for Y_4, Y_5, θ_4, θ_5, and G have been determined to provide wide operating bandwidth. Consequently, we can calculate Y_{h3} and denote

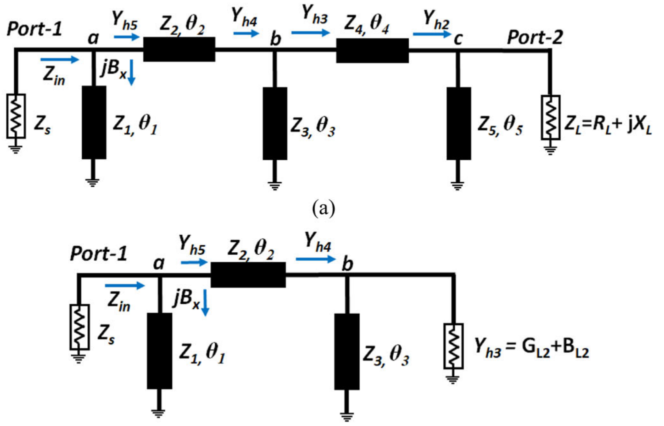


Fig. 7. (a) Odd-mode circuit diagram. (b) Reduced circuit diagram.

it another impedance as $Y_{h3} = G_{L2} + jB_{L2}$. With this assumption, the circuit is simplified as in Fig. 7(b), and the admittances at each node are derived as

$$Y_{h4} = Y_{h3} - jY_3 \cot\theta_3 \tag{12}$$

$$Y_{h5} = Y_2 \frac{Y_{h4} + jY_2 \tan\theta_2}{Y_2 + jY_{h4}\tan\theta_2}. \tag{13}$$

To satisfy (2) with 50-Ω input port termination, at node *a* in Fig. 7(b), it must be

$$\mathrm{Re}[Y_{h5}] = 1/2Z_s = 0.01 \tag{14}$$

$$\mathrm{Im}[Y_{h5}] = -B_x \tag{15}$$

where

$$B_x = -Y_1 \cot\theta_1. \tag{16}$$

In order to satisfy (14), there are many combinations of variables, namely Y_2, Y_3, θ_2, and θ_3, which provides another degree of design freedom. In other words, this is the specialty of this circuit that it allows us to choose from multiple solutions pools in both the even and odd modes. Once we find the values for these parameters, by using (16), we can design the short stub present at node *a* to satisfy (15) with a suitable combination of Z_1 and θ_1.

With the optimum set of values for even-mode case ($\theta_5 = 30°$, $\theta_4 = 84°$, $Z_5 = 29.12\ \Omega$, and $R = 8\ \Omega$), the even-mode bandwidth is 492 MHz when $Z_2 = 80\ \Omega$ and $Z_3 = 50\ \Omega$. With these values, $Z_{h3}(1/Y_{h3})$ is $232.75 - j37.7\ \Omega$ which features $Q \geq 6$, and Z_2 versus θ_3 for different θ_2 are plotted in Fig. 8 for $Z_3 = 50\ \Omega$. It is clear that no solution exists for $\theta_2 = 20°$, $\theta_2 = 40°$, and some values of θ_3. A similar plot for imaginary part of Y_{h5} is shown in Fig. 9.

After adding the TL section of length θ_3 (node b in Fig. 7), in 900 MHz–1 GHz range, the input impedance Z_{h4} (=1/Y_{h4}) spreads out with lower value of Z_3 as evident from the smith chart in Fig. 10. This indicates that higher value of Z_3 will provide more bandwidth, which is opposite of even mode analysis for bandwidth improvement as in Fig. 5(a). Hence, there exists a tradeoff bandwidth in even–odd mode analysis. For example, Table I shows six cases of design parameters. It can be observed that although lower θ_4 value is better, but

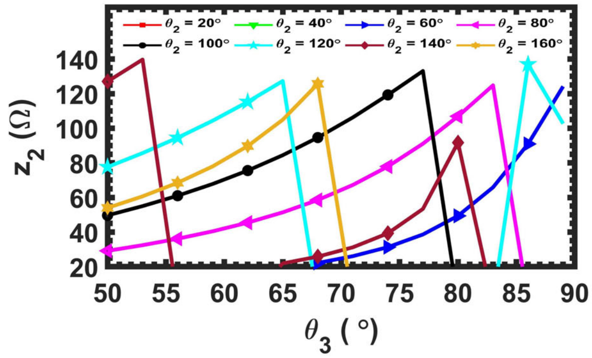


Fig. 8. Z_2 versus θ_3 for a range of θ_2.

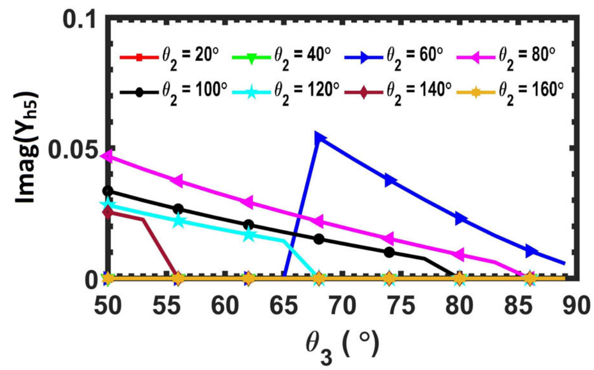


Fig. 9. Imaginary part of Y_{h5} versus θ_3 for a range of θ_2.

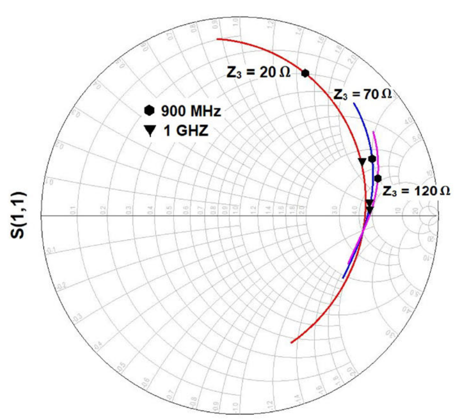


Fig. 10. Variation of Z_{h4} with Z_3 over a frequency range of 900 MHz–1 GHz.

the values in the even-mode do not alone decide the odd-mode bandwidth. In fact, from cases 4–6, subsequent TL section (with length θ_1, θ_2, and θ_3) have great impact on the bandwidth as well where the higher values of θ_1, Z_1, and Z_3 provide more bandwidth. However, it contradicts from the even-mode results where the lower values of Z_1 and Z_3 provide more bandwidth. Therefore, the intermediate values as in the range of 50–70 Ω are selected for these impedances.

Although, the even and odd mode analysis are carried out for the load impedance of $10 - j15$ as an example, the circuit's behavior may be entirely different for different loads depending on the solutions of different governing equations in even and odd modes. Therefore, similar analysis may be performed for a given impedance to find the best solutions.

TABLE I

DESIGN PARAMETERS FOR ODD MODE CASES WITH $Z(\Omega)$, θ (°), AND $R(\Omega)$

	Z_1/θ_1	Z_2/θ_2	Z_3/θ_3	Z_4/θ_4	Z_5/θ_5	R	Z_{h3}	BW (MHz)
1	20/68.89	56.78/50	100/89	80/84	29.12/30	8	232.7-j37.7	87
2	20/78.36	55.08/110	100/89	60/30	21.43/60	11.64	23.07+j13.02	112
3	20/85.35	43.93/70	100/89	100/21	20/60	9.935	25.34+j20.98	139
4	20/72.88	97.08/140	100/89	100/21	20/60	9.935	25.34+j20.98	86
5	20/78.46	54.44/100	100/89	100/21	20/60	9.935	25.34+j20.98	120
6	50/87.5	43.72/60	50/89	100/21	20/60	9.935	25.34+j20.98	249

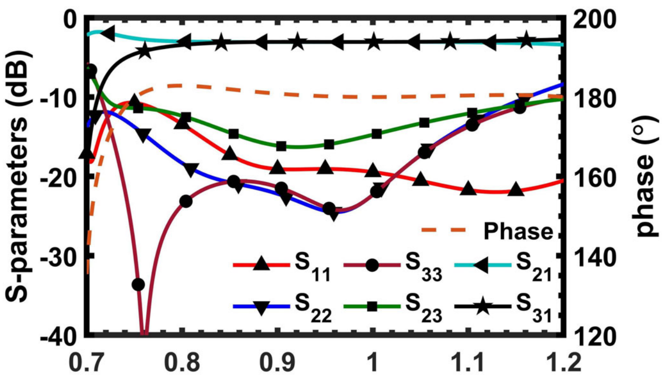


Fig. 11. Simulated S-parameters for a load impedance of $10 - j15$.

It is observed from the even and odd mode analyses that there are various parameters that conflicts in two modes. As a result, the intermediate values may be chosen for actual design. Finally, the length and impedance can be further optimized to balance the even and the odd mode values. Based on the above analysis, for the load impedance $10 - j15$, the parameter values are $Z_1 = 82.9\ \Omega$, $\theta_1 = 84.11°$, $Z_2 = 57.1\ \Omega$, $\theta_2 = 86.9°$, $Z_3 = 21.44\ \Omega$, $\theta_3 = 87°$, $Z_4 = 36\ \Omega$, $\theta_4 = 65$, $Z_5 = 43.82\ \Omega$, $\theta_5 = 25$, and $R = 21.96\ \Omega$. The simulated S-parameters of the proposed balun are plotted in Fig. 11, where a bandwidth of more than 410 MHz is realized at a frequency of 1 GHz.

C. Design Steps for Wideband Proposed Balun

In order to design a wideband microstrip balun transforming complex to 50-Ω termination impedance, the following steps are summarized to obtain optimum performance at any frequency and for any load impedance.

1) Start with choosing a low value for θ_5.
2) Solve (8) and (9) for Z_5 and R as in Fig. 3.
3) If Z_5 values are not in the range of 20–140 Ω then increase the θ_5 and repeat step-2 until the realizable values are found.
4) Select the intermediated values for Z_4 (around 70 Ω) and θ_4 (around 60°) and then find values of Z_5 and R from the plot.
5) Set-up the odd mode circuit as in Fig. 7(a) and find Y_{h3}.
6) Choose an intermediate value of Z_3 and solve (14). The values can be plotted as in Fig. 8. Choose θ_2 and find θ_3 and Z_2 and find the imaginary part of Y_{h5} from Fig. 9 for the chosen values.
7) Select an intermediate value of Z_1 and use (16) to find value of θ_1.

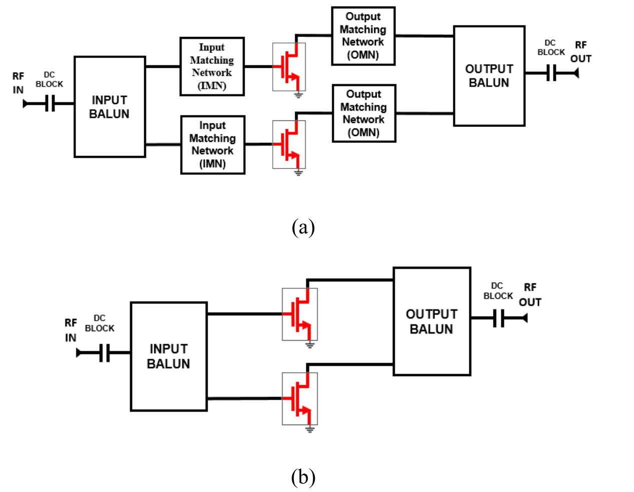


Fig. 12. (a) Conventional push–pull amplifier. (b) Proposed push–pull power amplifier.

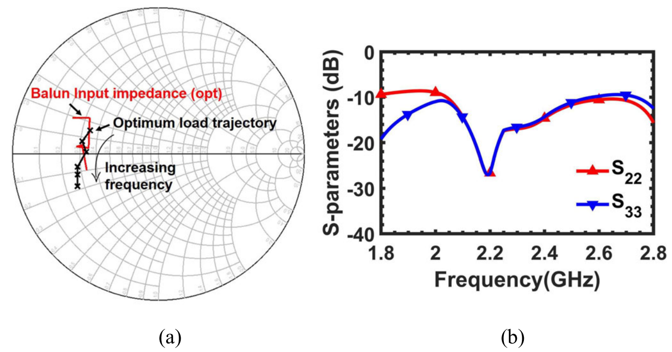


Fig. 13. (a) Optimum load impedance trajectory of GaN device and combining balun's balanced port impedance trajectory across the frequency band. (b) Balanced ports reflection coefficient for combing balun.

8) If bandwidth is not satisfactory then repeat from step 4 with different values of θ_4.

III. DESIGN OF WIDEBAND PUSH–PULL POWER AMPLIFIER

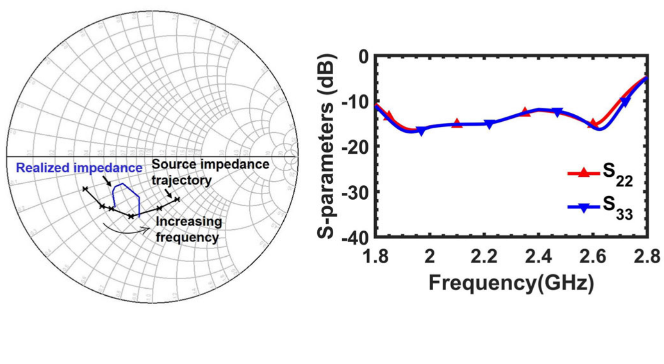
The conventional PPPA comprises input matching network (IMN), output matching network (OMN), input balun, and output balun, as shown in Fig. 12(a). The frequency selective matching networks in conventional PPPA cause additional power loss and limit the operating bandwidth. Therefore, in this article, a novel PPPA topology is proposed as in Fig. 12(b) to relax the impedance matching network by applying our wideband real-to-complex impedance transforming microstrip line balun. To be specific, our proposed PPPA features: 1) eliminating IMN/OMN from conventional PPPA and 2) wide bandwidth with planar layout.

Based on the previous wideband analysis of the proposed microstrip line balun, a PPPA is designed applying the Wolfspeed 10-W GaN device CGH40010F [42]. The transistor is biased in class-AB mode with −3.1 V gate voltage and 28-V drain voltage. First, the load pull simulation is carried out across the frequency1.8–2.6 GHz with the 200-MHz step, and the optimum fundamental load impedance trajectory of the GaN device is plotted on smith chart as in Fig. 13(a).

TABLE II
COMPARISON TABLE FOR THE BALUN

Reference	Frequency (GHz)	S_{11} (dB)	S_{22}/S_{33} (dB)	S_{23} (dB)	S_{21} (dB)	S_{31} (dB)	Fractional Bandwidth (%)	Phase deviation	Amplitude Imbalance (dB)	Impedance Transformation type[€]
[18]	2	<-10	No	No	-4.24	-4.22	36.3	<1°	1.1	R-R
[39]	1/2.6	-10	-20/-35	-22	3.5	-3.5	11	±5°	1	R-R
[36]	2.8	<-10	No	-14.2	-3.21	-3.28	35	±5°	<1	C-C
[27]	2	-15.78	-24.6	-23.25	-3.45	-3.45	<15	<±2°	NA	R-R
[30]	1	<-40	No	No	-3	-3	10.5	5°	1	R-R
[17]	2.4/5.2	<-19	No	No	-4.16	-4.17	5.1	2°	0.34	R-R
This work[μ]	**1**	**<-10**	**<-10**	**<-10**	**-3.06**	**-3.06**	**41**	**<2.8°**	**<1.3**	**R-C**

[μ] Simulated results, [€]R-R- Real to Real, R-C- Real to Complex, C-C- Complex to Complex



(a) (b)

Fig. 14. (a) Optimum input impedance trajectory of GaN device and splitting balun's balanced ports impedance trajectory. (b) Balanced ports reflection coefficient for splitting balun.

Here, the second and third harmonic load sweeps are simulated to avoid the low performance region. From the load trajectory, the intermediate impedance $16 + j0.6$ is selected at a center frequency of 2.2 GHz, and the combining balun is designed following the steps described in Section II with the selected complex impedance. Combining the biasing network and balun, the optimization is applied with relaxed matching condition, which turns out to be the balanced ports impedance of the proposed balun that follows the load impedance trajectory of transistor across the frequency. From Fig. 13(b), S_{22} and S_{33} are below -10 dB in the frequency range of 1.8–2.8 GHz.

A similar procedure is applied to design the input splitting balun for the proposed PPPA. The input impedance trajectory is found from the input large signal reflection of load pull simulation and plotted on the smith chart as in Fig. 14(a). The balanced ports impedance of splitting balun seem slightly off from ideal impedance trajectory of the GaN device which may cause gain variation of power amplifier. However, S_{22} and S_{33} are below -10 dB showing impedance matching across the frequency from 1.8 to 2.8 GHz.

To stabilize the circuit across the bandwidth, the resistors and capacitors network is added on the input side, and the quarter-wave transformer is designed to bias the gate of transistors. The schematic of PPPA with the proposed microstrip line balun is shown in Fig. 15. The output combining balun with biasing network has $\theta_5 = 72.87°$, $Z_5 = 21.6\ \Omega$, $\theta_4 = 17.32°$, $Z_4 = 48\ \Omega$, $\theta_3 = 88.9°$, $Z_3 = 48\ \Omega$, $\theta_2 = 39.8°$, $Z_2 = 39.83\ \Omega$, $\theta_1 = 71.85°$, $Z_1 = 69.7\ \Omega$, and $R = 38.86\ \Omega$. The input splitting balun has $\theta_5 = 92.85°$, $Z_5 = 76.92\ \Omega$, $\theta_4 = 85.66°$, $Z_4 = 67.5\ \Omega$, $\theta_3 = 88.54°$, $Z_3 = 48.31\ \Omega$, $\theta_2 = 98.17°$, $Z_2 = 90\ \Omega$, $\theta_1 = 88.9°$, $Z_1 = 48\ \Omega$, and $R = 119\ \Omega$.

IV. SIMULATION AND MEASUREMENT RESULTS

In the IMS paper [40], the real–complex microstrip line balun is simulated and measured. From the results, the measurement agrees well with simulation to prove the design concept. The comparison Table II is summarized to address the differences between previous works. It is clear that our proposed microstrip line balun features real–complex impedance transforming, uniplanar layout, high isolation, balanced ports impedance matching, and wide bandwidth. To prove the wideband characteristic of the proposed real–complex microstrip line balun, a wideband PPPA using the proposed balun as splitter and combiner is designed and fabricated on Rogers RO 6002 with a $\varepsilon_r = 2.94$, a loss tangent of 0.0012, and a substrate thickness of 20 mil, and the prototype is shown in Fig. 16(a). The Keysight's ADS is used to simulate the circuit, and the optimization is applied to tune the circuit achieving trade-off performance across the bandwidth.

The EM simulated and continuous wave (CW) measured results of PPPA are shown in Fig. 16. With 32.5-dBm input power, the simulated gain varies from 11.59 to 12.25 dB across the frequency 1.8–2.7 GHz, while the measured gain varies from 10.21 to 12.27 dB as in Fig. 16(b). The simulated output power varies from 44.1 to 44.86 dBm, and the measured output power varies between 42.71 to 44.77 dBm across the frequency 1.8–2.7 GHz as in Fig. 16(c). The simulated drain efficiency is 55.57%–70.37%, and the measured drain efficiency varies between 59.88% and 74.66% in the frequency range of 1.8–2.7 GHz as in Fig. 16(d). Comparing the simulation to the measurement results, there are the slight difference between the two results, which are attributed to soldering, fabrication tolerance, modeling of transistor, condition for measurement, and cooling approach for transistor.

The power sweep measurement at frequencies 1.84, 2.18, and 2.59 GHz are shown in Fig. 17. With the 3-dB compression, the output power is 44.7 dBm, and the efficiency is 71.1% at 1.84 GHz. With the same compression level, at 2.18 GHz, the output power is 42.95 dBm, and the efficiency is 64.5%. At 2.59 GHz, the output power is 44.2 dBm, and the efficiency is 63.8% for the designed PPPA with the same compression level.

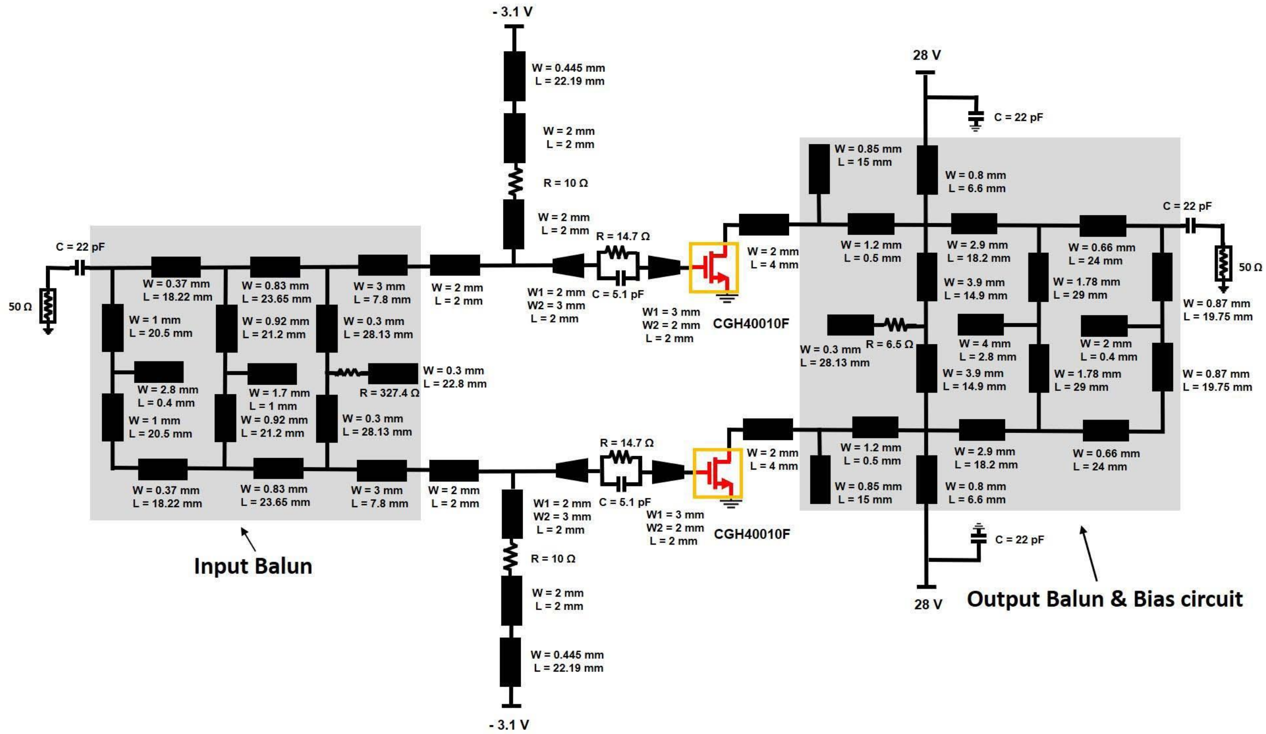
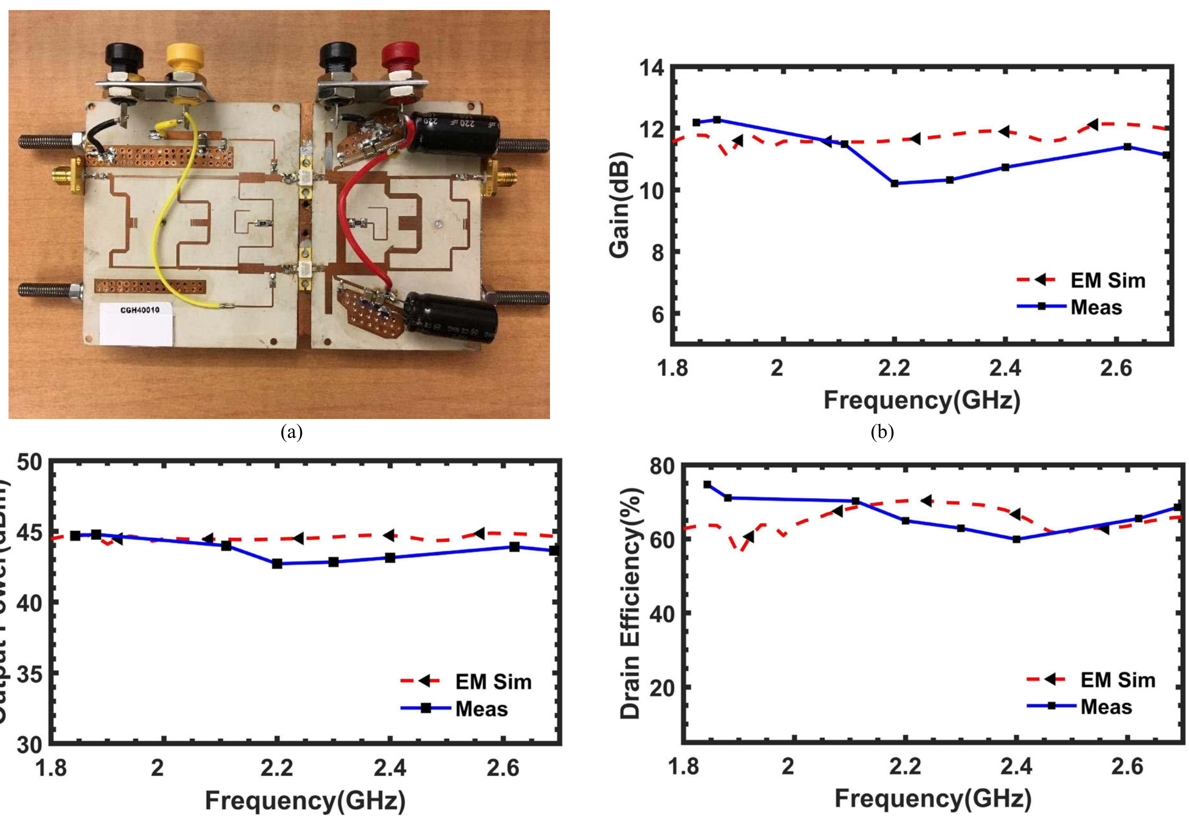


Fig. 15. Schematic for push–pull power amplifier with the proposed splitting and combining wideband real–complex microstrip line baluns.



(c) (d)

Fig. 16. (a) Prototype of PPPA with proposed splitting and combining microstrip baluns. (b) Simulated and measured gain of PPPA under CW. (c) Simulated and measured output power of PPPA under CW. (d) Simulated and measured drain efficiency of PPPA under CW.

To verify the linearity of the proposed PPPA, a 20-MHz WCDMA signal with 7.2-dB PAPR is generated to measure the modulated signal performance. Fig. 18(a) shows the measured adjacent channel power ratio (ACPR) which has been evaluated for an output power of lower than 38 dBm. It can be seen that the ACPR is below −31.3 dBc

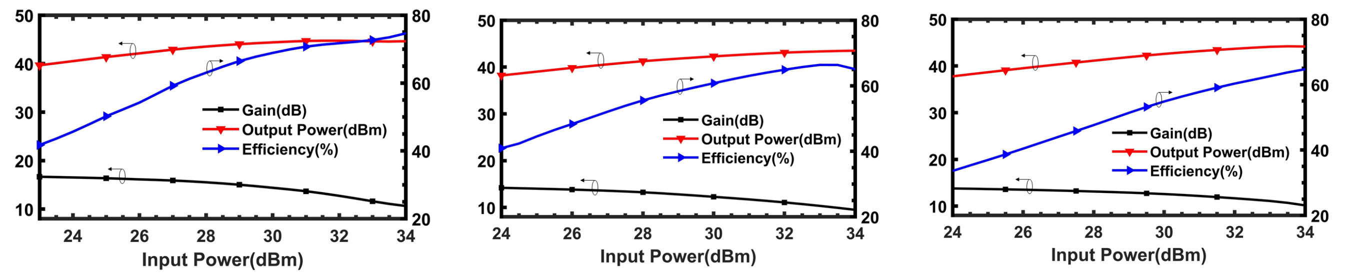


Fig. 17. Power sweep results of proposed PPPA at (a) 1.84, (b) 2.18, and (c) 2.59 GHz.

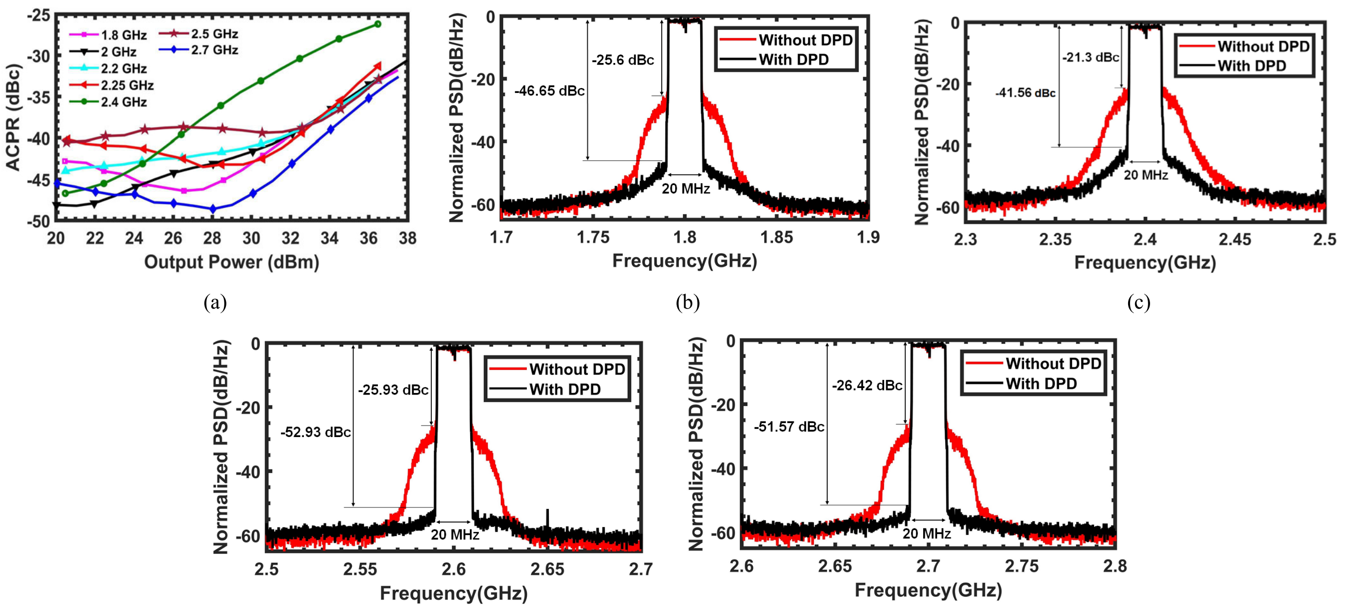


Fig. 18. Measured modulated signal performance. (a) ACPR versus output power (dBm) with 20-MHz WCDMA signal at 1.8, 2, 2.2, 2.25, 2.4, 2.5, and 2.7 GHz; output spectra with a 20-MHz LTE signal with and without the DPD at (b) 1.8, (c) 2.4, (d) 2.6, and (e) 2.7 GHz.

TABLE III

COMPARISON TABLE FOR PUSH–PULL POWER AMPLIFIER

Reference	Frequency Range (GHz)	Gain (dB)	Gain Variation	Output Power (dBm)	Efficiency (%)	Bandwidth (%)	PCB Layer	Balun	Coaxial Balun	B.w.I$^{\zeta}$	Without DPD	With DPD	I.T.T$^{¥}$
[1]	0.45 – 1.95	~13 - 20	~7	46.6-49.3	45-85$^{\$}$	125	Double	In/Out	No	No	-33, -29, -31	-48, -47, -47	R-R
[5]	8-12	10	NA	42-44	55-60$^{\$}$	40	Multi	In/Out	No	No	NA	NA	R-R
[6]	5.4 – 5.6	11.5 – 12.5	1	37.5 – 38.5	48.7$^{\#}$	3.63	Multi	In/Out	No	No	NA	NA	R-R
[7]	2.35- 2.56	7-12	5	42$^{\#}$	48$^{\#}$	8.57	Multi	In/Out	No	No	NA	NA	R-R
[8]	0.5-2.5	16-18	2	41-43	47-63$^{£}$	134	Single	In/Out	No	No	NA	NA	R-R
[9]	4-9	4-8	4	30-32	15-25$^{£}$	76.92	Double	In/Out	No	No	NA	NA	R-R
[10]	4-8.5	4-7	3	31-35.5	14-42$^{£}$	72	Single	In/Out	No	No	NA	NA	R-R
[12]	0.25-3.1	9-21	12	40-46	35-73$^{\$}$	170.14	Single	Out	Yes	No	NA	NA	R-R
This work	**1.8 – 2.7**	**10.21 – 12.27**	**2.07**	**42.71 – 44.77**	**59.88 – 74.66$^{\$}$**	**40.9**	**Single**	**In/Out**	**No**	**Yes**	**-25.6, -21.3, -25.93, -26.42**	**-46.65, -41.56, -52.93, -51.57**	**R-C**

$^{\#}$ Peak value, $^{\$}$ Drain Efficiency, $^{£}$ Power Added Efficiency, $^{\zeta}$ Balun with Isolation, $^{¥}$ Impedance transformation type, R-R- Real to Real, R-C- Real to Complex

for 1.8, 2, 2.2, 2.25, 2.5, and 2.7 GHz while it is below −26.2 for 2.4 GHz. The different "sweet spot" location across the frequency band is mainly caused by the different third- and fifth-order coefficients, variation of out of the band termination impedances including baseband and second harmonic, and frequency-dependent nonlinear parasitic capacitors. To validate the linearization performance of the proposed PPPA, a 20-MHz LTE signal with 7.2-dB PAPR is generated and linearized by Wolfspeed Digital Predistortion (DPD) system [41]. Fig. 18(b)–(e) illustrates the performance before and after the DPD, where the adjacent channel leakage ratio achieves −46.65, −41.56, −52.93, and −51.57 dBc after the DPD at 1.8, 2.4, 2.6, and 2.7 GHz respectively.

In Table III, some recent works are summarized and compared with the proposed PPPA with novel microstrip line balun. It can be noticed that the presented PPPA implements with baluns that provide isolation between its output ports, and direct real-to-complex impedance transformation. Therefore, separate matching network is not required with this PPPA. Moreover, for some applications, the nonplanar structure is not compatible with system level integration, and hence for those cases this PA is more suitable. The other advantage of planar structure is that it is easy to install the heat sink beneath the structure. The presented work also provides high output power, high efficiency, and less gain variation comparing to the other reported works on PPPA. In the next step, different types of planar coupling structures will be investigated to replace the microstrip lines, which can further improve the bandwidth of the proposed balun. Also, the harmonic impedance alignment will be investigated to boost the performance of the PPPA.

V. Conclusion

In this article, a novel microstrip line balun is proposed to transform complex balanced impedance to 50-Ω unbalanced impedance. The even–odd mode method is applied to analyze the proposed balun, and the rigorous study is presented to improve the bandwidth of the proposed design. To prove the wideband characteristics, a PPPA with the proposed microstrip line baluns is designed, fabricated, and measured. The simulation and measurement results agree well with each other to validate the design theory.

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