Domain wall-magnetic tunnel junction spin– orbit torque devices and circuits for inmemory computing

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ABSTRACT

There are pressing problems with traditional computing, especially for accomplishing data-intensive and real-time tasks, that motivate the development of in-memory computing devices to both store information and perform computation. Magnetic tunnel junction memory elements can be used for computation by manipulating a domain wall, a transition region between magnetic domains, but the experimental study of such devices has been limited by high current densities and low tunnel magnetoresistance. Here, we study prototypes of three-terminal domain wall-magnetic tunnel junction in-memory computing devices that can address data processing bottlenecks and resolve these challenges by using perpendicular magnetic anisotropy, spin-orbit torque switching, and an optimized lithography process to produce average device tunnel magnetoresistance TMR = 171% and average resistance-area product $RA = 29 \ \Omega \mu m^2$, close to the RA of the unpatterned film. Device initialization variation in switching voltage is shown to be curtailed to 7%–10% by controlling the domain wall initial position, which we show corresponds to 90%–96% accuracy in a domain wall-magnetic tunnel junction full adder simulation. Repeatability of writing and resetting the device is shown. A circuit shows an inverter operation between two devices, showing that a voltage window is large enough, compared to the variation noise, to repeatably operate a domain wall-magnetic tunnel junction circuit. These results make strides in using magnetic tunnel junctions and domain walls for in-memory and neuromorphic computing applications.

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Computing today faces walls when processing data-intensive and unstructured tasks. Memory access in modern computers can dominate as much as 96% of computing time.¹ SRAM idle leakage can consume over 20% of the total power of a computation.^{2,3} For Internetof-things applications, there is a large bottleneck in analog to digital conversion, where analog readout can consume over 70% of the active power.⁴ The development of in-memory computing magnetic devices could alleviate the memory wall between computation and memory onchip, as well as between devices and the cloud by allowing more computation to be performed on the device, with a subset of information going to the cloud.⁵ The nonvolatility of such elements would reduce idle leakage. The radiation-hardness of magnetic in-memory computing devices would also be attractive for space applications.⁶ Three leading device types that use magnetic tunnel junctions (MTJs) and domain walls (DWs) for in-memory computing are majority logic,^{7–9} mLogic,^{10–14} and three-terminal domain wall-magnetic tunnel junctions (DW-MTJs).^{15–19} However, these devices have suffered from challenges: switching of a DW can require high current, and the multiple etch steps needed to create an MTJ pillar on top of a DW track have led to reduced tunnel magnetoresistance (*TMR*).^{20,21} These issues have limited experimental study of devices and circuits. The DW-MTJ is a candidate in-memory computing device, with previous prototypes showing fanout and concatenation in circuits.¹⁶ Simulation work has shown that a single DW-MTJ can perform a NAND function; the devices can be cascaded to build a one-bit adder,¹⁵ and, recently, a 32-bit adder with registers was simulated

entirely from DW-MTJs.¹⁹ Versions of DW-MTJ devices have also found application in neuromorphic computing circuits for artificial intelligence.^{22–26} If the challenges of this class of devices could be resolved, they could remove the bottleneck between computation and memory.

Figure 1(a) shows a schematic of the studied DW-MTJ device. A heavy metal/ferromagnet/oxide trilayer, e.g., Ta/CoFeB/MgO, is patterned into a DW track with an output MTJ centered on top of the track. Voltage *V* applied between the *IN* and *CLK* terminals moves the position of a DW in the DW track. The DW position determines the centered MTJ resistance and therefore the output current from the *OUT* terminal to the next DW-MTJ device in the circuit.^{15,16} The MTJ resistance $R_{\text{MTJ}} = R_{\text{P}}$ when the magnetic layers are parallel (P) and $R_{\text{MTJ}} = R_{\text{AP}}$ when antiparallel (AP). *Oe*₁ to *Oe*₂ is an Oersted field electrode used to nucleate the initial DW position entirely with the current.^{27,28}

The MTJ stack was grown by Applied Materials in an Endura CloverTM physical vapor deposition system²⁹ with layers Si(substrate)/SiO₂(100)/Ta(10)/CoFeB(1.2)/MgO(1)/CoFeB(1.9)/[Co/Pt](5)/Ru(0.9)/[Co/Pt](6.9)/Ta(1)/Ru(3); numbers are in nm and brackets represent multilayers. See Ref. 29 for growth details of a similar stack. Using a physical property measurement system, the average film properties were $TMR = 168 \pm 6\%$ and resistance-area product $RA = 35 \pm 2 \Omega \mu m^2$.

The film stack was patterned using electron beam lithography and ion beam etching (for fabrication methods, see the supplementary material). Example scanning electron microscope images of the devices are shown in Figs. 1(b) and 1(c); DW tracks of widths w = 250, 350, and 450 nm were patterned. To facilitate keeping the DW from exiting the device, a notch is fabricated on each side of the track.

The out-of-plane major hysteresis loop of the unpatterned film, Fig. 2(a), shows perpendicular magnetic anisotropy (PMA). To better understand the switches, the magnetization vector of the four ferromagnetic layers of the stack is depicted by arrows: the bottom green arrow is the free layer CoFeB (1.2 nm), the second-from-bottom blue arrow is the reference layer CoFeB (1.9 nm), and the top two gray arrows are the two layers of the synthetic antiferromagnet (SAF), each composed of Co/Pt multilayers. Starting from saturation at the positive field, as the field decreases first, the SAF unravels due to its antiparallel coupling. The thin reference layer is able to stay in the field direction, despite the SAF unraveling, until below +86 mT, when the reference layer now aligns with the bottom SAF layer. At 1 mT, the free layer switches (green arrow), and at -190 mT, the reference layers switch together.

Figure 2(b) shows the minor hysteresis loop of the unpatterned film, where the field is kept low enough that only the free layer switches. The offset shows field coupling between the free and reference layers. Figure 2(c) and 2(d) shows R_{MTJ} vs out-of-plane magnetic field $H(\hat{z})$ for device 1 of w = 450 nm and device 6 of w = 250 nm (see the supplementary material for additional devices' field loops). The properties of six prototypes are summarized in Table I compared to that of the unpatterned film. The average device $TMR = 171 \pm 21\%$, close to the unpatterned average $TMR = 168 \pm 6\%$, but with increased standard deviation. The device average $RA = 29 \pm 3 \ \Omega \ \mu m^2$, close to the unpatterned average $RA = 35 \pm 2 \ \Omega \ \mu m^2$. These results show that both the TMR and RA are maintained after patterning and that we have up to 203% TMR, close to the expected highest TMR (\sim 200%) seen in PMA CoFeB-MgO MTJs.²⁹ This is a large improvement over previous results where the patterning degraded the TMR to 10%-40%,^{20,21,26} and overcoming this degradation has been the focus of other recent domain wall-based logic research.³⁰ High TMR is important in MTJs for logic applications since it determines the current separation between the 0 and 1 states.¹

The average switching field of the patterned reference layer in the major loop $H_{c,pinned} = -186 \pm 25$ mT, close to the unpatterned film (-190 mT). This shows that the interfacial anisotropy of the reference layer is stronger than the shape anisotropy of patterning it into a 250–450 nm diameter pillar. For the device experiments that follow, all fields are kept under $H_{c,pinned}$ such that the reference and SAF magnetizations are fixed, and the free layer is switched to obtain $R_{\rm MTJ} = R_{\rm P}$ or $R_{\rm MTJ} = R_{\rm AP}$.

The average coercive field of the patterned free layer in the major loop $H_{c,free} = -114 \pm 7$ mT, showing that the free layer coercivity has significantly increased from the unpatterned $H_{c,free} = 5$ mT. It has been shown that in PMA films, field reversal is dominated by DW nucleation at impurities and defect sites and subsequent DW propagation.^{31,32} The higher coercivity is evidence that there are low imperfections in the w = 250-450 nm track for DW formation.

In the minor loop [e.g., Fig. 2(d)], the average AP to P switch $H_{c,AP-P} = 2.5 \text{ mT} \pm 2 \text{ mT}$ and average $H_{c,P-AP} = -114 \text{ mT} \pm 7 \text{ mT}$. The field offset shows that the coupling between the free layer DW track and pillar-structure reference layer is still present, requiring the use of a DC applied magnetic field $H_{\rm B}$ during device testing to overcome this coupling. Both an in-plane and out-of-plane applied field direction worked to compensate for the stray field, and the bias field also assisted spin–orbit torque switching. This field could be removed in the future by further optimizing the film stack.



FIG. 1. DW-MTJ device. (a) Schematic of the three-terminal DW-MTJ device with *IN*, *CLK*, and *OUT* terminals. The DW track is composed of Ta (gray)/CoFeB (blue/red with a white domain wall)/MgO (white), and the output MTJ is shown as a blue circle. Red and blue represent the domains in $\pm z$. Only essential layers are shown and not to scale. The *4P* terminal is used to measure the four-point resistance of the MTJ; Oe₁ to Oe_2 is an Oersted field electrode. (b) Top-down scanning electron microscope image of w = 450 nm and (c) w = 350 nm device prototypes with patterned DW track and output MTJ labeled.



FIG. 2. Film and device switching behavior. (a) Unpatterned film out-of-plane major field loop. The switching behavior is explained using four arrows to depict the four ferromagnetic layers of the stack: bottom green = free layer, second-from-bottom blue = reference layer, and top two gray = SAF layers. (b) Minor field loop of the free layer. (c) R_{MTJ} vs out-of-plane magnetic field (1 mT field steps) for half of the major loop and (d) for the minor loop where only the free layer is switched, for device 1 and device 6 in Table I. Example R_{MTJ} vs $V(1 \ \mu s$ pulses of increasing amplitude, with voltage step size 0.5 V) between *IN* and *CLK* terminals for 5 cycles (e) for device 2 and (f) for device 3, with $H_B = -100 \text{ mT}$.

We first study the DW-MTJ switching behavior vs V when an external magnetic field is used to saturate the initial magnetization of the free layer, i.e., with no initial DWs present. First, saturation field $H_{\text{SAT}}(\hat{z}) = 50 \text{ mT}$ is applied to set the free layer magnetization out of plane. Then, H_{B} is applied. V is then applied between the *IN* and *CLK* terminals to switch the free layer magnetization (1 μ s pulses of increasing amplitude, with voltage step size 0.5 V). Figures 2(e) and 2(f) show the example R_{MTJ} vs V for five cycles for two of the devices, with the field conditions applied between cycles to re-saturate the free layer. A cycle-to-cycle distribution of switching voltage V_C is observed. The relatively large range in switching voltage is consistent with DW nucleation at different defect sites each cycle. It is clear that V_C depends on

the energy landscape of the DW track, showing a varying but not fully random switching voltage distribution. Converting V_C to current density $J_C = \frac{V_C}{R_w A_w}$, where R_w is the measured resistance between *IN* and *CLK* and A_w is the cross-sectional area of the patterned Ta/CoFeB wire, results in $J_C = 1.0-4.8 \times 10^{11} \text{ A/m}^2$, reduced from STT IMA prototypes with $J_C \approx 2 \times 10^{12} \text{ A/m}^{2.20}$

We then study the DW-MTJ switching behavior vs V when the electrical current is used to nucleate the DW at an initial position. After applying $H_{\text{SAT}} = -120 \text{ mT}$ to bring a device to the AP state, $V_{\text{Oe}} = 2 \text{ V}$ (50 ns) is applied through the additional Oersted field line electrode (Oe_1 to Oe_2) that is centered on top of the left notch in the DW track, shown in Fig. 1. Over 50 cycles, $V_{\text{Oe}} = 2 \text{ V}$ has 100%

#	w (nm)	TMR (%)	RA (Ω - μ m ²)	$\mathrm{R}_{\mathrm{P}}\left(\Omega\right)$	$R_{AP}\left(\Omega\right)$	$ H_C AP \rightarrow P (mT)$	$ H_C P \rightarrow AP (mT)$	$ H_C $ reference (mT)
Unpatterned Film		168 ± 6	35 ± 2			0.5	5	190
Device 1	450	203	26	164	497	5	113	198
Device 2	450	185	27	169	481	4	120	220
Device 3	450	168	32	199	534	1	110	170
Device 4	350	155	30	313	800	0.5	120	200
Device 5	350	146	33	347	855	0.5	120	150
Device 6	250	166	27	548	1456	4	104	176
Devices Avg.		171 ± 21	29 ± 3			2.5 ± 2	114 ± 7	186 ± 25

TABLE I. Device properties. Switching behavior of the six devices compared to that of the unpatterned film.

probability of switching $R_{\rm MTT}$ from $R_{\rm AP}$ to $R_{\rm P}$. This is evidence that a DW is nucleated at or near the left notch in the device, which is underneath the Oersted field line. Since $V_{\rm Oe}$ switches $R_{\rm MTJ}$, most likely a 180° DW is nucleated that changes the magnetization under the MTJ. Next, V=0-6 V is applied (1 μ s pulses, amplitude step size 0.1 V) from *IN* to *CLK*, to switch the DW that has been nucleated. See the supplementary material for a step-by-step visualization of the magnetization setup and reversal.

Figure 3(a) shows the initialization cycle-to-cycle variation of device 1 over 10 cycles, where the DW is re-initialized using the Oersted field line between each cycle. Defining the percent variation $var = \frac{1}{2} * \frac{V_{C,mux} - V_{C,min}}{V_{C,ang}}$, var = 10.7%, decreased from 44% to 75% in Figs. 2(e) and 2(f) when the DW is allowed to nucleate randomly. Initialization cycle-to-cycle variation testing over 10 cycles was also done on device 3 (see the supplementary material) and showed var = 7%. The average depinning voltage is 4.22 V, on the higher end of the voltage range [see in Figs. 2(e) and (f)]. This agrees with a DW being nucleated at the notch with a lithographically-designed pinning location that will increase V_C at the expense of better controlling the DW position, important for device design considerations. This shows the all-electrical operation of DW-MTJ devices, besides the DC bias field.

Device success depends on viability in a functional circuit. We have simulated a DW-MTJ 32-bit adder; see Ref. 19 for details. In the simulation, parameter variation is increased from 0 to 25% and the full adder accuracy (% correct data output) is calculated, with results shown in Fig. 3(b). Two *TMR* values are used: the average device *TMR* = 170% and lower *TMR* = 165% to show how *TMR* variation affects the overall accuracy. For *TMR* = 170%, device 1 *var* = 10.66% corresponds to an adder accuracy of 90%; device 3 *var* = 7% corresponds to an adder accuracy of 96%. Further optimization to *var* = 5% would produce almost no errors.

In an operating circuit, it is expected that the DW will not have to be often nucleated since once created, it will be pushed back and forth, with nucleation used to refresh the data when needed. The write/reset cycle-to-cycle behavior is shown in Fig. 3(c). After nucleation with the Oersted field line, V=0-5.5 V (1 μ s, 0.1 V steps) is applied from *IN* to *CLK* to write the device, switching $R_{\rm MTJ}$ from $R_{\rm P}$ to $R_{\rm AP}$. Then, V = -(0-5.5) V (1 μ s, 0.1 V steps) is applied to reset the device, switching $R_{\rm MTJ}$ from $R_{\rm AP}$ to $R_{\rm P}$. This is repeated for four back/ forth cycles, showing that the DW-MTJ can be repeatably written and reset. Here, after the 8 total switches, we had to re-initialize the DW, and more work is needed to increase the cycling endurance before re-initialization.

A two-device circuit is set up by wire bonding *OUT* of device A (here, device 6 was used) to *IN* of device B (here, device 1 was used) to show an inverter circuit. After the same initialization protocol as Fig. 3(a), both devices are in the P state with DWs nucleated on the left, as depicted in Fig. 4(a). Since device A has $R_{\text{MTJ},A} = R_{\text{P}}$, it is in a Bit 1 state. To then read device A while writing device B, a voltage pulse is applied between CLK_A and CLK_B . Figure 4(b) shows, for 10 re-initialization cycles, that the current through device A switches $R_{\text{MTJ},B}$ from P (Bit 1) to AP (Bit 0), with $V_{\text{C,avg}} = 4.06 \text{ V}$ and var = 10%. The inset shows $R_{\text{MTJ},A}$ over the 10 cycles.

Conversely, when device A is written to its AP state by switching its DW, $R_{\text{MTJ},A} = R_{\text{AP}}$ and it is in a Bit 0 state, depicted in Fig. 4(c). Figure 4(d) shows, for 10 re-initialization cycles, that the current through device A switches $R_{\text{MTJ},B}$ from P (Bit 1) to AP (Bit 0), with $V_{\text{C,avg}} = 4.61 \text{ V}$ and var = 15%. Thus, a supply voltage window has opened up between 4.06 and 4.61 V, where on average, the circuit will act as an inverter. For example, if V = 4.4 V is applied to both cases, on average, when $R_{\text{MTJ},A} = R_{\text{P}}$ (Bit 1), then device B will switch from R_{P} (Bit 1) to R_{AP} (Bit 0); when $R_{\text{MTJ},A} = R_{\text{AP}}$ (Bit 0), then there is not enough current to switch device B and it will remain R_{P} (Bit 1).

While single inversion events have been shown in previous work for perfectly matched devices and switching conditions,¹⁶ here a voltage window has opened up enough, compared to the variation noise, to repeatably operate a circuit. This shows a path for further film stack and device engineering to widen this operation window, both through better matched resistances in the circuit and even lower variation.

In conclusion, DW-MTJs are an emerging class of magnetic random-access memory-like devices for in-memory computing, artificial intelligence, and radiation-hard applications. This work overcomes major challenges in DW-MTJ devices by showing high *TMR* and maintained *RA* after patterning, measuring feasible switching current densities using SOT, characterizing the variation in switching behavior and that it can be low enough cycle-to-cycle variation for circuit applications, and showing bit propagation in an inverter circuit. The work provides design parameters for DW-MTJ circuits and for improved future device and circuit design. It motivates film growth and device



FIG. 3. Cycle-to-cycle variation. (a) Device 1 initialization cycle-to-cycle variation over 10 cycles, when the DW is re-initialized each cycle using the Oersted field line. $H_B = -100 \text{ mT}$. (b) Simulated full adder accuracy vs device parameter variation, for two TMR values. (c) Device 1 write/reset cycle-to-cycle variation over 8 cycles, where the DW is initialized using the Oersted field line at the start of the first cycle, and then the DW is moved back and forth. $H_B = -100 \text{ mT}$ when it switches from P to AP, and $H_B = 2 \text{ mT}$ when it switches back from AP to P.

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FIG. 4. Two-device inverter circuit. (a) Cartoon of the circuit just before *V* is applied to read device A and write device B, with *OUT* of device A connected to *IN* of device B. Device 6 was used for A and device 3 for B. The DW has been nucleated on the left of each device, and before the switch $R_{\text{MTJ,A}} = R_{\text{P}}$ (Bit 1) and $R_{\text{MTJ,B}} = R_{\text{P}}$ (Bit 1). Bias field $H_{\text{B}} = -100 \text{ mT}$ is shown by a black arrow. (b) Resistance of device B vs applied voltage pulse (1 μ s, 0.1 V steps) between *CLK*_A and *CLK*_B, measured over 10 reinitalization cycles, showing the switch from R_{P} (Bit 1) to R_{AP} (Bit 0). Average switching voltage is shown by the black thicker curve. Device A resistance over the same 10 cycles is shown in the inset. (c) Cartoon of the circuit when device A has been switched to $R_{\text{MTJ,A}} = R_{\text{AP}}$ (Bit 0), just before *V* is applied to read device A and write device B. (d) Resistance of device B vs applied voltage pulse (1 μ s, 0.1 V steps) between 20 carbon of the circuit when device A has been switched to $R_{\text{MTJ,A}} = R_{\text{AP}}$ (Bit 0), just before *V* is applied to read device A and write device B. (d) Resistance of device B vs applied voltage pulse (1 μ s, 0.1 V steps) between 20 carbon of the circuit when device A has been switched to $R_{\text{MTJ,A}} = R_{\text{AP}}$ (Bit 0), just before *V* is applied to read device A and write device B. (d) Resistance of device B vs applied voltage pulse (1 μ s, 0.1 V steps) between CLK_{A} and CLK_{B} , measured over 10 reinitalization cycles, showing that the average switching voltage (black thicker curve) from R_{P} (Bit 0) is 0.55 V higher than in the first case, due to the higher resistance of device A in the AP state. Device A resistance over the same 10 cycles is shown in the inset.

optimization to remove the need for external DC fields, as well as larger statistical measurements of the cycle-to-cycle and device-todevice variability.

See the supplementary material for experimental methods, additional field switching data, step-by-step visualization of the device setup and writing, and additional cycle-to-cycle variation data.

AUTHORS' CONTRIBUTIONS

M.A. and T.L. contributed equally to this work.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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