REVIEW SUMMARY

QUANTUM COMPUTING

Materials challenges and opportunities for quantum computing hardware

Nathalie P. de Leon, Kohei M. Itoh, Dohun Kim, Karan K. Mehta, Tracy E. Northup, Hanhee Paik*, B. S. Palmer, N. Samarth, Sorawis Sangtawesin, D. W. Steuerman

BACKGROUND: The past two decades have seen intense efforts aimed at building quantum computing hardware with the potential to solve problems that are intractable on classical computers. Several hardware platforms for quantum information processing (QIP) are under active development. To realize large-scale systems based on these technologies, we must achieve error rates much lower than have been demonstrated thus far in a scalable platform, or devise a new platform entirely. These activities will require major advances in materials science and engineering, new fabrication and synthesis techniques, and new measurement and materials analysis techniques. We identify key materials challenges that currently limit progress in five quantum computing hardware platforms, propose how to tackle these problems, and discuss some new areas for exploration. Addressing these materials challenges will necessitate interdisciplinary approaches from scientists and engineers beyond the current boundaries of the quantum computing field.

ADVANCES: This Review constitutes a roadmap of the current challenges and opportunities for materials science in quantum information processing. We provide a comprehensive review of materials issues in each physical platform by describing the evidence that has led to the current understanding of each problem. For each platform, we present reasons for particular material choices, survey the current understanding of sources of noise and dissipation, describe materials limitations to scaling, and discuss potential new material platforms. Despite major differences among physical implementations in each hardware technology, there are several common themes: Material selection is driven by heterogeneity, impurities, and defects in available materials. Poorly controlled and characterized surfaces lead to noise and dissipation beyond limits imposed by bulk properties. Scaling to larger systems gives rise to new materials problems that are not evident in single-qubit measurements.

OUTLOOK: We identify three principal materials research frontiers of interest in this context. First, understanding the microscopic mechanisms that lead to noise, loss, and decoherence is crucial. This would be accelerated by developing high-throughput methods for correlating qubit measurement with direct materials spectroscopy and characterization. Second, relatively few material platforms for solid-state QIP have been explored thus far, and the discovery of a new platform is often serendipitous. It is thus important to develop materials discovery pipelines that exploit directed, rational material searches in concert with high-throughput characterization approaches aimed at rapid screening for properties relevant to QIP. Third, there are several materials issues that do not affect single-qubit operations but appear as limitations in scaling to larger systems. Many problems faced by these platforms are reminiscent of some that have been addressed over the past five decades for complementary metal-oxide semiconductor electronics and other areas of the semiconductor industry, and approaches and solutions adopted by that industry may be applicable to QIP platforms. Materials issues will be critical to address in the coming years as we transition from noisy intermediate-scale systems to large-scale, fault-tolerant systems. Quantum computing began as a fundamentally interdisciplinary effort involving computer science, information science, and quantum physics; the time is now ripe for expanding the field by including new collaborations and partnerships with materials science. ■

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Cite this article as N. P. de Leon *et al.*, *Science* **372**, eabb2823 (2021). DOI: 10.1126/science.abb2823

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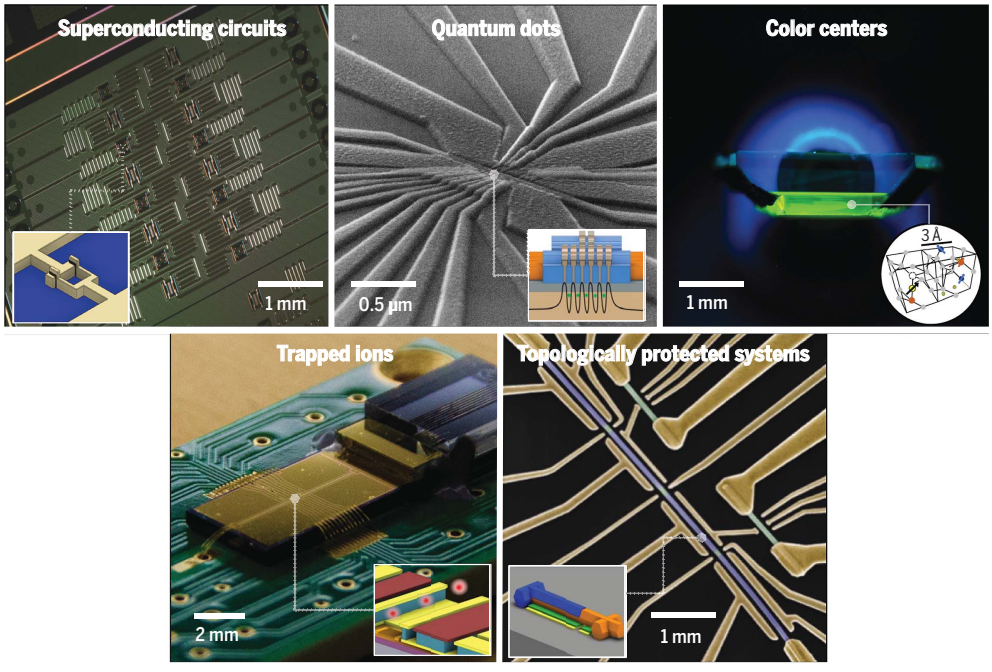
https://doi.org/10.1126/science.abb2823



Five quantum computing hardware platforms. From top left: Optical image of an IBM superconducting qubit processor (inset: cartoon of a Josephson junction); SEM image of gate-defined semiconductor quantum dots (inset: cartoon depicting the confining potential); ultraviolet photoluminescence image showing emission from color centers in diamond (inset: atomistic model of defects); picture of a surface-electrode ion trap (inset: cartoon of ions confined above the surface); false-colored SEM image of a hybrid semiconductor/superconductor [inset: cartoon of an epitaxial superconducting Al shell (blue) on a faceted semiconducting InAs nanowire (orange)].

REVIEW

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Materials challenges and opportunities for quantum computing hardware

Nathalie P. de Leon[1], Kohei M. Itoh[2], Dohun Kim[3], Karan K. Mehta[4], Tracy E. Northup[5], Hanhee Paik[6]*, B. S. Palmer[7,8], N. Samarth[9], Sorawis Sangtawesin[10], D. W. Steuerman[11]

Quantum computing hardware technologies have advanced during the past two decades, with the goal of building systems that can solve problems that are intractable on classical computers. The ability to realize large-scale systems depends on major advances in materials science, materials engineering, and new fabrication techniques. We identify key materials challenges that currently limit progress in five quantum computing hardware platforms, propose how to tackle these problems, and discuss some new areas for exploration. Addressing these materials challenges will require scientists and engineers to work together to create new, interdisciplinary approaches beyond the current boundaries of the quantum computing field.

The promise of quantum information processing (QIP) that outperforms classical supercomputers for tasks such as simulation of quantum systems and particular algorithms including factorization, search, and optimization (*1*–*4*) has spurred the recent development of different physical platforms for quantum processors. The advantage of quantum systems arises from the fundamentally different way in which information is encoded and processed in quantum computers as compared to classical computers (*4*). An N-bit classical register can encode information in N coefficients (0 or 1), but a register of N quantum two-level systems (quantum bits, or qubits) can exist in a superposition of any of the 2^N possible combinations of each qubit state. A full description therefore requires 2^N coefficients, each of which is a complex, continuous quantity (Fig. 1A).

Loosely speaking, this exponentially larger information-storing capacity arising from quantum coherence and entanglement underpins the ability to execute certain tasks that are intractable on classical computers. Appropriately designed quantum algorithms can result in constructive interference that encodes the solution, whereas other possible outputs ideally undergo destructive interference. The computational power of such operations comes at the cost of fragility, however. Quantum states can decay and decohere during computation, resulting in errors that accrue more rapidly in larger systems. Because measurements on quantum systems change their states, classical error correction is not directly applicable. Quantum error correction provides a means to account for and make use of these changes to enable low-error computations (*5*), but it requires significantly increased system scale and highly precise operations. These problems make quantum computing difficult to physically implement (Fig. 1B).

Many proof-of-principle demonstrations of quantum algorithms (*6*) have been executed on small, noisy quantum computers (*7*) with dozens of qubits and error rates that preclude quantum error correction. Recently, a quantum computer based on 53 superconducting qubits was shown to outperform the world's largest classical computers in calculating a random circuit (*8*). Other demonstrations include implementing quantum approximate optimization algorithms on trapped-ion processors (*9*) and using bosonic modes to perform calculations that are computationally hard, such as calculating the vibronic spectra of small molecules by using the bosonic modes of microwave cavities controlled by qubits (*10*, *11*). Variational quantum algorithms such as variational quantum eigensolvers (*12*) and quantum circuit learning (*13*) have been used to calculate energies of simple molecules (*14*–*16*), simulate lattice models (*17*), and improve efficiency of machine learning (*18*).

The next frontier in QIP is to achieve quantum advantage (*19*, *20*) for useful problems, which will require reducing system errors and advancing physical platforms to larger scale. Materials science has informed the development of current solid-state qubits, primarily through down-selection of material platforms for favorable material properties. For example, current implementations of superconducting qubits rely on the high-quality, kinetically limited oxide of aluminum as a tunnel barrier in the Josephson junction. Recent progress in quantum dot spin qubits has been enabled by the selection of nuclear spin–free materials and their isotopic purification, as well as the development of new growth processes to optimize silicon/germanium interfaces. Color centers were developed as qubits after decades of advances in the synthesis of high-purity diamond.

Beyond material selection, however, there has been comparatively little work toward using the tools of materials science to improve and scale quantum hardware. Most activity so far has instead focused on developing quantum control schemes and device architectures that circumvent sources of noise, loss, and decoherence, rather than directly measuring and tackling the underlying material systems limitations. Ultimately, building large quantum systems capable of quantum error correction will require scaling physical qubits through miniaturization and high-density integration while eliminating noise to ensure high-fidelity control. Both efforts necessitate significant advances in improving and understanding materials, devising new fabrication processes, and discovering new material systems.

Below, we outline the current materials challenges in five technological platforms for QIP (Table 1): superconducting qubits, semiconductor gate-defined quantum dots, color centers, ions, and topologically protected Majorana modes. First we introduce some key figures of merit to parameterize performance in different platforms. Then, for each platform, we introduce the basic qubit scheme and current fabrication methods, followed by challenges arising from various sources of noise and dissipation in the material systems, the materials limitations to scaling that technology, and efforts to find alternative material systems. Finally, we discuss how new approaches to materials science for QIP, such as high-throughput characterization of devices and materials, can lead to the next generation of quantum hardware.

Metrics

The basic performance of qubits is captured with a few key parameters. The first metric characterizes the time interval within which information stored in a single qubit is lost, generally referred to as the coherence time, T_2. One limit on coherence is dissipation: The qubit loses energy to its environment with a characteristic relaxation time T_1 (*21*)—for

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example, by spontaneous emission. This relaxation places an upper bound on the coherence time $T_2 < 2T_1$ for all qubits. In addition to relaxation, qubits can experience dephasing that arises from uncontrolled changes to the energy splitting between qubit levels.

The relevant qubit dephasing time depends on the QIP task at hand, and some noise can be mitigated with additional control. The inhomogeneous dephasing time, T_2^*, arises from quasi-static inhomogeneity in the transition frequency—for example, from magnetic field variations that change the Zeeman energy in spin-based qubits. This dephasing can be corrected by driving the qubit with a Hahn echo sequence, in which a pulse reverses the evolution of the qubit, thus canceling the effects of inhomogeneity (*22*). The resulting, extended coherence time is referred to as $T_{2,\mathrm{echo}}$. More complex sequences of multiple pulses, known as dynamical decoupling, may extend the coherence to longer times, denoted as $T_{2,\mathrm{DD}}$. Conversely, such pulse sequences can also serve as a valuable tool for probing the environmental noise spectrum, and these techniques have been deployed in superconducting (*23*), ion trap (*24*), color center (*25*), and gate-defined quantum dot (*26*–*28*) systems.

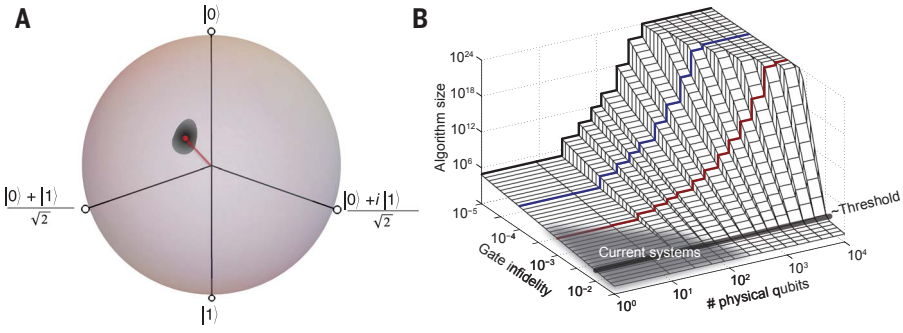

Fig. 1. Errors in quantum bits. (**A**) Bloch-sphere representation of a single-qubit state; a superposition of 0 and 1 is described by a complex amplitude with magnitude and phase, which can be viewed as residing on the surface of the unit sphere. Errors from imperfect gates or decoherence result in deviations (shaded region) from the ideal vector, thereby decreasing fidelity. As a result, quantum error correction (QEC) is likely essential for most applications of quantum computation. (**B**) Theoretical overheads associated with QEC in a specific case of the surface code (*32*). The number of error correction cycles achievable (proportional to the number of operations possible on logical qubits) is plotted against the number of physical qubits required for each single logical qubit and the limiting two-qubit gate infidelity, $1 - \mathcal{F}$. For systems with errors below a threshold infidelity, larger computations are possible at the cost of increased physical qubit counts. Threshold, error scaling, and overhead requirements depend strongly on choice of code (*31*) and on the physical nature of the error. [Image courtesy of Ying Li and Simon Benjamin]

In addition to the storage time in a qubit, the time required to implement logic gates and the fidelity of logic gates are important metrics to consider. Logic gates are implemented in most platforms by the application of electromagnetic radiation, such as microwave or optical pulses. The gate fidelity $\mathcal{F}$, expressed as a percentage, is a metric that assesses how accurately the physical realization of a gate implements the desired transformation (*4*), and hence the approximate number of gates that can be implemented before introducing some total error. Logic gates are executed over a finite time, during which decoherence from the underlying noise affecting qubits imposes one limit on $\mathcal{F}$. The ratio of the gate duration to coherence time bounds approximately what gate fidelities can be expected given the underlying noise in physical qubits.

Beyond decoherence, limits to achievable fidelities can arise from imperfections in the

Table 1. Five quantum computing hardware platforms and associated sources of noise.

Platform	Where the quantum information is stored	Known sources of noise	
		Bulk materials	Surfaces and interfaces
Superconducting qubits	Energy eigenstates of Josephson junction–based electronic resonant circuits	• Substrate dielectric loss • Excess quasiparticles in superconducting metal cause dissipation and dephasing	• Uncontrolled oxides and contaminants host two-level systems, causing dissipation and dephasing • Surface spins and charges cause flux noise and charge noise, respectively
Gate-defined quantum dots	Spin states of electrons or holes confined in electrostatic potential	• High mobility required for individual dot formation • Nuclear spins limit T_2	• Charge traps and magnetic impurities at the dielectric interfaces • Interface inhomogeneity: Variation in valley splitting and spin-orbit coupling
Color centers	Electronic orbital and spin states	• Paramagnetic impurities and nuclear spins limit T_2 • Extended defects lead to strain and limit T_2^*	Dangling bonds and electron traps at the surface affect T_2 and optical coherence for shallow NV centers
Ion traps	Electronic transitions within individual atomic ions	(Not a significant noise source)	Electric-field noise heats ion motion
Majorana zero modes	Non-Abelian topological phase of Majorana zero modes	Defect density in nanowires	Semiconductor-superconductor nanowire interface that creates a proximity hard gap

control signals that implement logic gates, or from excitation to undesired energy levels. Gates that operate on single qubits, together with those that implement interactions and generate entanglement between two qubits, are sufficient for universal quantum computation (*29*); the latter require physical mechanisms for interactions between distinct qubits, and they can be sensitive to sources of noise that may not affect operations on individual qubits. In any platform, two-qubit gates typically operate with lower fidelity than single-qubit gates.

Lower error rates generally allow for more sophisticated algorithms on current hardware (*8*, *30*), and future error-correcting quantum computers will likely require fidelities far beyond 99.9% across a large-scale device (*31*–*33*); higher-fidelity operations translate to reduced overheads associated with quantum error correction (Fig. 1B). Reliably achieving such low error rates in a scalable platform will undoubtedly require exquisite control over the constituent materials in any platform.

Coherence times and gate fidelities are useful in assessing basic physical hardware but do not capture the requirements for operation of large-scale systems. As QIP systems mature, various groups are working to identify new metrics to capture complex systems; for example, the metric of quantum volume parameterizes computational capacity in a scalar value that incorporates qubit number, fidelities, connectivity, and cross-talk (*34*).

For most solid-state qubits, improvements in single-qubit coherence—potentially driven by materials science—will have a direct impact on quantum computing capabilities. For other platforms, such as trapped ions, single-qubit coherence times are unaffected by materials considerations and are already long enough that they do not limit current systems; however, materials issues can pose problems for multiqubit operations and for scaling. Such problems are likely to play an increasing role in all platforms as systems mature.

Here, we introduce five quantum computing hardware platforms and describe the current understanding of noise and dissipation in each system. For each platform we discuss future directions, including prospects for scaling and seeking new materials. In each case, bulk properties can limit material choice and can place stringent constraints on material synthesis and purity. Additionally, surfaces and interfaces introduce sources of noise and loss, an understanding of which is important for guiding fabrication schemes and qubit design.

Superconducting qubits

Superconducting qubits encode information in the energy eigenstates of Josephson junction–based electronic circuits (*35*–*37*). There are several types of superconducting qubits with differing circuit construction and therefore different sensitivities to material-related noise: The transmon (*38*) and x-mon (*39*) consist of a capacitively shunted Josephson junction where the junction acts as a nonlinear inductor (Fig. 2A). The fluxonium qubit (*40*) consists of an inductively shunted Josephson junction. By changing the applied magnetic flux through a superconducting loop, its potential well structure can be substantially changed, resulting in changes in its matrix elements and its sensitivity to different sources of decoherence. The capacitively shunted flux qubit (*41*, *42*) consists of three Josephson junctions forming a superconducting quantum interference device (SQUID) loop (*43*), shunted by a large capacitor where the qubit state is an energy eigenstate of the persistent current in the SQUID loop (the magnetic flux through the loop). A relatively new superconducting qubit, the gatemon, uses a voltage-tunable semiconductor weak-link barrier for the Josephson junction (*44*). In all these devices, Josephson tunnel junctions play a crucial role as the nonlinear element, providing anharmonicity to the energy levels of the circuit, and therefore allowing the isolation of just two levels within a larger Hilbert space (*45*).

Superconducting qubits are one of the most mature QIP platforms, and state-of-the-art processors based on superconducting transmon qubits have been scaled up to 65 fully programmable qubits on one chip (*46*). Record fidelities include a single-qubit gate fidelity of 99.97% (*47*), readout fidelity of 99.8% (*47*),

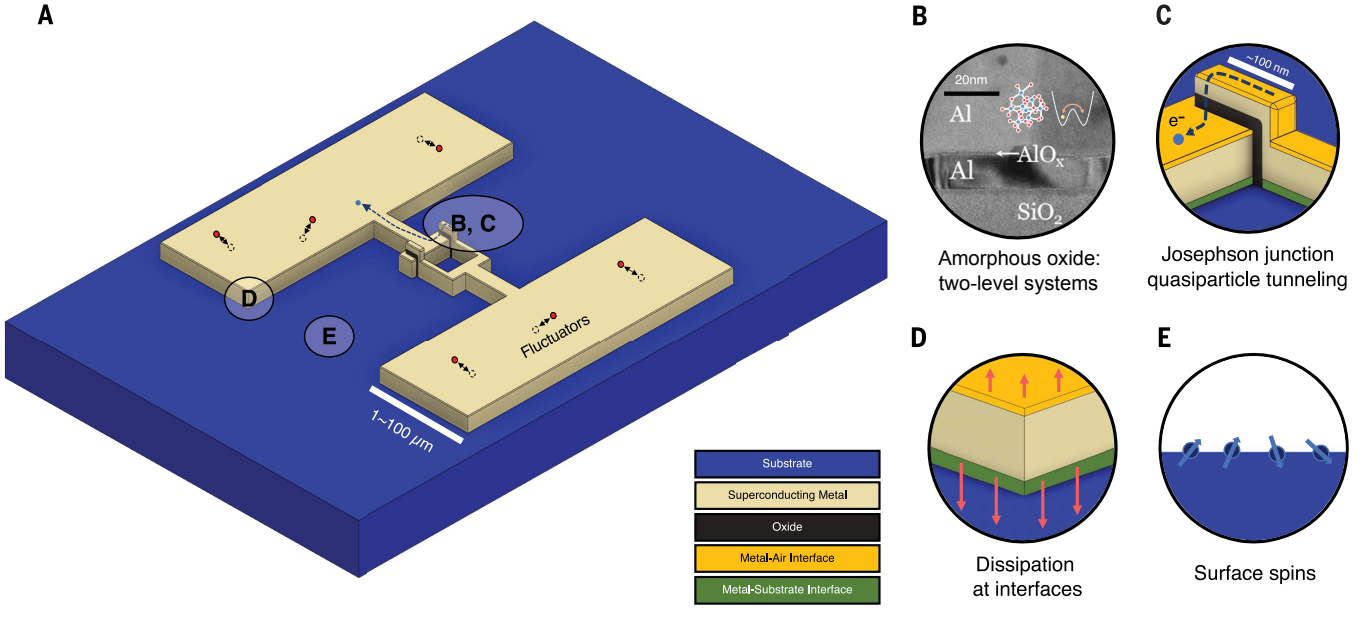

Fig. 2. Superconducting qubit. (**A**) Schematic illustration of a superconducting transmon qubit. A transmon is an anharmonic microwave resonator created by capacitively shunting a Josephson tunnel junction (or junctions). The qubit state is controlled by applying a resonant microwave signal. (**B**) Typical cross section scanning electron micrograph of a Josephson junction (*120*). Insets: Two-level systems may arise from the amorphous AlO_x. (**C**) QP tunneling through the junction leads to dissipation and dephasing, and QP transport across the surface of the superconductor leads to dissipation. (**D**) Electromagnetic energy in the capacitor can be absorbed by lossy dielectrics in the substrate, the metal-substrate interface, the metal-air interface, or the substrate-air interface. (**E**) Surface spins contribute to flux noise.

and two-qubit gate fidelity of 99.5% (47). T_1 times are typically ~100 μs (45). For fixed-frequency transmon qubits, $T_{2,\mathrm{echo}} \approx T_1 \approx$ 100 μs, and typical gate times are around a few hundred nanoseconds (48, 49). Tunable transmons or capacitively shunted flux qubits can allow for much faster gate times, around tens of nanoseconds (45), but their tunability also renders them more susceptible to flux noise, typically resulting in faster decoherence $T_{2,\mathrm{echo}} \approx 20$ μs (8, 45). This trade-off leads to similar two-qubit gate fidelities for these two architectures.

Material choices

Josephson junctions in superconducting qubits are typically fabricated from aluminum and aluminum oxide (Al/AlO_x/Al) because a thin insulating thermal barrier is desired, and the thickness of AlO_x is kinetically limited during growth to a few nanometers (Fig. 2B). To avoid dissipation by defects in the junction (50–52), the typical junction has lateral dimensions on the order of 100 nm and is formed by first creating a shadow stencil in a polymer resist by electron-beam (e-beam) lithography. After the resist is developed, two layers of Al are evaporated at two different angles with an oxidation step between the two depositions, and the small overlap from the two evaporation steps forms the junction (53, 54) (Fig. 2C).

This material system has several advantages: (i) Thin AlO_x layers have few pinholes and therefore produce low current leakage in the junction (55); (ii) aluminum has a low-temperature melting point that makes metal deposition compatible with lithography resists and lift-off (56); and (iii) AlO_x can be formed on Al in a self-limiting manner that allows deposition of all three layers (Al/AlO_x/Al) in situ during a single pump-down. Aside from the junction itself, capacitors and inductors are patterned with lateral extents up to a few hundred micrometers (Fig. 2A) and have been made with aluminum as well as other superconducting metals and alloys via photo- or e-beam lithography. Other common metals for these components include elemental superconductors (Nb) and nitride-based alloys (TiN and NbTiN) (57).

Superconducting qubits can store a substantial fraction of their electric field energy in the substrate, so it is important to select a substrate material that has low dielectric loss. Approximating the qubit as a harmonic oscillator, its lifetime T_1 can be expressed in terms of the quality factor $Q = 2\pi f T_1 = 1/\tan(\delta)$, where f is the resonant frequency of the qubit and $\tan(\delta)$ is the loss tangent of the material (50, 58). In the gigahertz frequency range, this loss is typically the result of absorption by charged ions or dipoles followed by reemission as phonons. Common low-loss substrates include sapphire [$\tan(\delta) < 10^{-8}$] (59) or high-resistivity silicon [$\tan(\delta) < 10^{-6}$] (60).

Sources of noise and dissipation

Researchers working on superconducting qubits have primarily focused on two models for loss and dissipation, namely two-level systems (TLSs) in dielectrics and non-equilibrium quasiparticles (QPs) in the superconductor. Here, we outline some of the key experimental observations that suggest the relevance of these models. Interestingly, the observed microwave loss in superconducting quantum circuits increases with decreasing microwave power at cryogenic temperature (50). This observation points to a loss mechanism different from known bulk dielectric loss mechanisms, such as nonlinear optical processes or coupling to phonons (61, 62).

One microscopic model for these observations is the discrete TLS model (Fig. 2B, inset), which was originally formulated to explain a number of properties of amorphous solids at low temperature and has been applied to explain some results associated with superconducting qubit devices (63, 64). In this model, the qubit's electric field couples to a discrete TLS, resulting in a shorter T_1 for the qubit. At larger electric fields and higher temperatures, the TLS can be saturated, resulting in less loss; the predicted power dependence from the TLS loss model has been observed in a variety of systems and device geometries (50, 65–70). A comprehensive list of measured loss tangents at low power and low temperature for various materials is compiled in (71). Discrete TLSs can be observed in the qubit spectrum when they strongly couple to the modes of the circuit. Several studies have focused on characterizing the dipole moment, density, and lifetime of strongly coupled TLSs (50, 51, 72–75). However, it has not yet been well established whether these observed strongly coupled TLSs are the primary loss mechanism, and their origins in the fabrication process are still unknown.

Another microscopic model for the observed loss is the presence of broken Cooper pairs, termed nonequilibrium QPs (Fig. 2C). QPs can exchange energy with the qubit when they tunnel through the Josephson junction, or they can give rise to resistive losses in the superconducting metal. If the superconducting device were in thermal equilibrium with the refrigerator at temperatures $T < 100\ \mathrm{mK} << T_c$, where T_c is the superconducting transition temperature, the QP density should be negligibly small (76). However, a number of experiments studying single–Cooper pair devices, microwave kinetic inductance detectors, and superconducting qubit devices estimate a QP density on the order of 1 QP per cubic micrometer arising from unknown excitation above the superconducting gap (77–84). Non-equilibrium QPs in both resonators and qubits absorb the stored microwave energy; for the densities estimated above, models suggest that the qubit T_1 would be limited to a few hundred microseconds ($Q = 10^6$ to 10^7), comparable to the quality factors of current state-of-the-art devices (81, 83, 85).

For superconducting resonators, the loss associated with QPs decreases with an increase in applied microwave power, making it difficult to experimentally distinguish QP-related loss from loss associated with TLS behavior (80, 86). Although the cause of non-equilibrium QPs is not known, potential mechanisms include stray infrared or optical photons, high-energy phonons, or cosmic rays (80, 87–90). Without the exact cause identified, one material solution to reduce the effect from QPs is to engineer the superconducting gap in the junction structure (77, 91) or manufacture surface traps (92) to reduce dissipation from QPs.

Despite extensive study of the dependence of dissipation on device parameters and geometry, the exact microscopic origins of dissipation in superconducting qubits remain unknown. State-of-the-art qubits exhibit T_1 much shorter than the limits imposed by bulk dielectric loss (93–95), which suggests that surfaces and interfaces are likely major limiting factors. Although surfaces and interfaces (Fig. 2D) comprise small volumes and have low overlap with the electromagnetic mode in a superconducting qubit, they can become a dominant source of loss if they house materials with high loss tangent. The energy participation ratio of an interface can be used to estimate a limit for T_1 (60). For example, if an interface contains a material with loss tangent $\tan(\delta) \sim 10^{-2}$ to 10^{-3} (values that are typical for oxides and polymers), an energy participation of 100 parts per million at that interface (a typical value for qubits with long coherence times) (96) will limit the qubit T_1 to a few hundred microseconds ($Q = 10^6$ to 10^7), which is comparable to experimental observation in state-of-the-art qubits.

Much work in improving coherence over the past decade has focused on systematically varying the qubit geometry to change the degree of overlap between the electromagnetic mode and the interfaces or surfaces of the device (60, 94, 97–101) and preparing surfaces to reduce lossy oxides before growth or deposition of the superconducting metal (97, 102). Surface-related loss could arise from uncontrolled surface states, oxides, or contamination. Several investigations of surface loss have used superconducting resonators (without junctions) to enable rapid exploration and a wider range of microwave power and temperature. Interface cleaning such as O_2 plasma etching or weak-ion milling before metal deposition improves the quality factors of Al superconducting resonators on sapphire (97).

More recently, superconducting qubits with tantalum shunting capacitors deposited on sapphire have shown T_1 and $T_{2,DD}$ exceeding 0.3 ms and represent a factor of ~3 improvement over the prior state of the art (*95*). Tantalum forms thin, kinetically limited, chemically robust oxides, in contrast to niobium. These recent advances suggest that optimizing constituent materials and systematically improving and passivating surfaces will be a critical frontier in the improvement of superconducting qubits.

In addition to dissipation, dephasing can be caused by low-frequency material-related magnetic and charge noise, particularly for frequency-tunable qubits. Magnetic noise (or flux noise) primarily couples to the qubit through SQUID loops used in tunable qubits. As a result, $T_{2,echo}$ times in tunable qubits are typically ≤50 μs and are limited by a background flux noise of a few $\mu\Phi_0/\sqrt{\text{Hz}}$ at 1 Hz, where the magnetic flux quantum $\Phi_0 = h/(2e)$, h is Planck's constant, and e is the electron charge (*84*, *103*–*107*). This flux noise, which exhibits a $1/f$ spectrum, is universal in SQUIDs regardless of their inductance, geometry, or choice of metal (*108*). Most models and experiments point to randomly oriented electron spins (Fig. 2E) as the source of flux noise, clustered locally within and around the SQUID loop (*108*–*113*). Because flux noise is nearly independent of the type of metals used and is of greater magnitude than the noise predicted from the abundance of nuclear spins in the metal and Si substrate, it is unlikely to be caused by nuclear spins (*114*). The estimated spin density for the observed flux noise is roughly $5 \times 10^{17}/\text{m}^2$ (*114*, *115*). Recent studies showed that the flux noise can be reduced by preventing adsorption of gas species on the metal surfaces and formation of the native oxide (*105*, *116*). The materials science underlying flux noise is a long-unresolved question that has been studied for decades in SQUID detectors and now merits systematic investigation in the context of advanced superconducting qubit technology.

Low-frequency $1/f$ charge and offset drift noise observed with superconducting qubits also shows a power spectral density on the order of $(10^{-3}e)^2/f$ (*117*–*119*). The microscopic origin of this noise has not been identified (*117*–*119*). Instead, the issue has so far been addressed through qubit design by adding a large shunting capacitor (*38*) or an inductor (*40*) to suppress the sensitivity to charge noise. As a result, the investigation of charge noise in superconducting qubits has not made much progress in recent decades.

Materials limitations to scaling

Superconducting qubits are typically fabricated with large lateral dimensions (≥100 μm) to reduce the surface participation ratio and thereby achieve long coherence times (*93*). This general trade-off between size and coherence poses a problem for scaling systems to large numbers of qubits. Future-generation processors with thousands or more qubits will require solving the surface noise issue to enable scaling up to high-density quantum processors.

One of the major roadblocks to scaling qubits will be qubit-to-qubit variation. Specifically, the temporal or spatial (on-chip) variation in qubit frequencies can reduce the yield of the device or complicate the calibration of quantum gates. The junction critical current that governs the inductance of the qubit is exponentially sensitive to the thickness of the tunnel barrier (*76*), which is typically an amorphous AlO_x layer (Fig. 2B). As a result, angstrom-scale variation of the barrier thickness (*120*) can yield a few percent variation in the critical current (*120*–*122*), which in turn causes a few percent variation in the qubit frequency. In addition, the junction barrier can "age" either by diffusion of oxygen or change of chemical composition after thermal cycling or after storage in ambient conditions for many days (*123*–*125*). Variation in the observed coherence times T_1 and T_2 can also affect the gate fidelity. The coherence times can drift or change suddenly over hours and days, even while the device is held at cryogenic temperatures (*89*, *95*, *126*, *127*). The origin of this instability is unknown, but recent work suggests either interaction with a TLS (*126*, *127*) or incident cosmic rays as potential contributors (*89*).

Scaling to a large number of qubits can introduce new challenges even with high-quality individual qubits and two-qubit gates. For example, routing control and readout signals to and from each qubit can introduce additional errors and cross-talk. Microwave fields extend away from the qubit plane by ~100 μm, and the additional dielectrics and defects implicated in typical three-dimensional (3D) wiring structures can form a major dissipation source. The various electromagnetic modes supported by a complex qubit array and/or wiring structure can form additional loss channels (*128*). One approach to mitigate these problems relies on 3D wiring structures separated from the qubit layer by interposers; such interposers must be composed of low-loss crystalline materials, thereby presenting new fabrication challenges (*129*, *130*).

New material platforms

New material development for superconducting qubits has focused on improving interface quality or finding more reproducible and stable junction barriers. In the past decade, epitaxially grown materials have been explored in order to improve the junction interface (*131*–*134*) or to improve the quality of the interface between the substrate and superconducting film (*102*, *135*–*138*). Such efforts have not yet shown improvement of the device coherence beyond the state of the art established almost 10 years ago, presumably because the dominant loss mechanism in those previous efforts was not related to the interface under study. However, given that advances in design, packaging, and characterization techniques have yielded improvements in and greater understanding of the qubit environment, it is an opportune time to revisit material platforms for superconducting qubits. Recent results showing improved coherence with tantalum-based planar transmons (*95*) suggest that a systematic exploration of other materials may also yield improvements in qubit coherence time. As another example, the demonstration of the "gatemon" with a semiconducting tunnel barrier is an excellent example of new material platforms leading to a new capability of voltage-based frequency tuning (*44*, *139*). Separately, improving substrates for low dielectric loss or low flux noise is another possible area of study. So far, sapphire and silicon substrates have been essentially the only substrates deployed in superconducting qubits with long coherence times (*56*). There has not yet been a systematic study of the impact of different synthetic methods and different surfaces and interface preparations on dielectric loss at low powers and low temperatures, or a wide-ranging exploration of alternative substrate materials. It will be beneficial to collaborate with researchers from bulk crystal and thin-film growth, as well as from other QIP systems such as semiconducting qubits or color centers, who have uncovered analogous sources of noise in potential substrate materials.

Quantum dots

Gate-defined quantum dots in semiconductors (Fig. 3A) store qubits primarily in spin states of quantum confined electrons or holes. The needed confinement is created by potential landscapes that are shaped by voltages applied to electrodes. Position-dependent electric dipoles, or charge states, could be used to form qubit states (*140*, *141*), but strong coupling to charge noise creates rapid decoherence, and we do not consider this type of qubit here. In 1998, Loss and DiVincenzo first proposed a universal set of single- and two-qubit gates based on the individual electron spins in tunnel-coupled semiconductor quantum dots (*142*). Here, the single qubit is controlled by resonant microwave pulses, whereas the two-qubit quantum gate relies on the Heisenberg exchange interactions enabled by interdot coupling. Because of this seminal proposal, a variety of more sophisticated qubit schemes have been proposed that exploit mixing among spin, charge, and orbital degrees of freedom of quantum confined electron states in semiconductor quantum dots and include two electron spin states in a double quantum dot (singlet-triplet) (*143*), as well as three electron

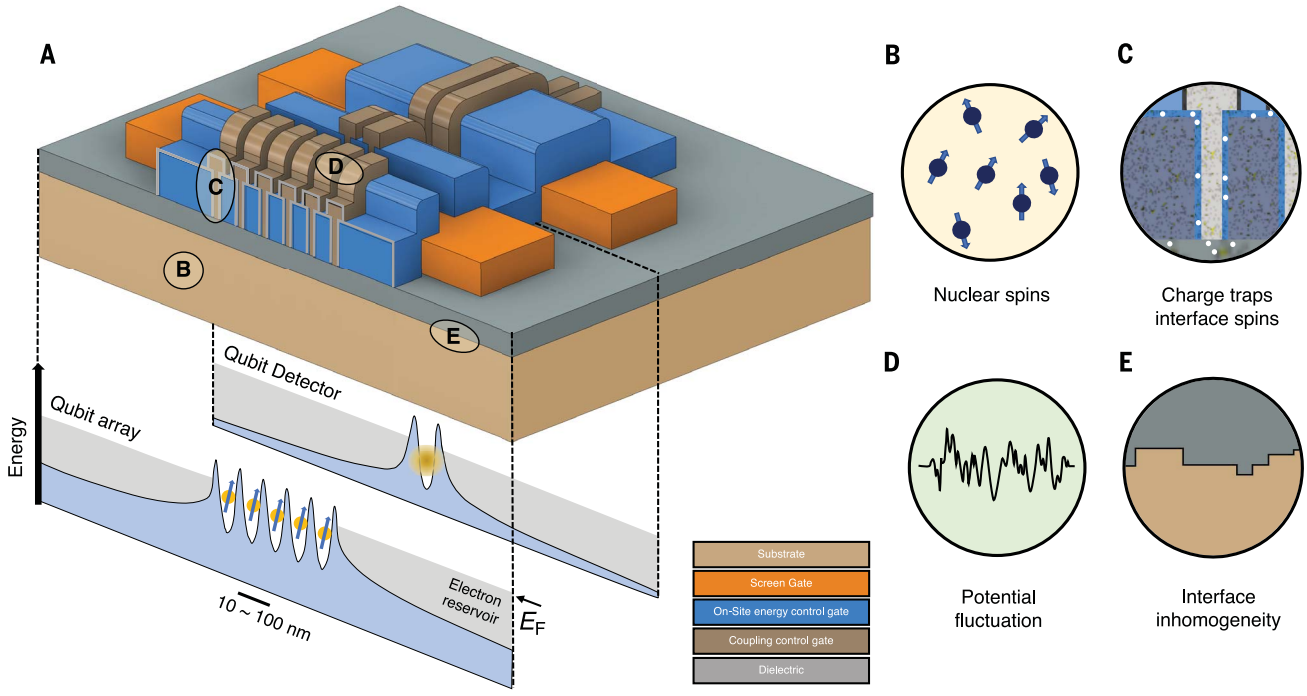

Fig. 3. Semiconductor quantum dot spin qubit. (**A**) Schematic illustration of a gate-defined quantum dot spin qubit device. Semiconductor quantum dot spin qubits use electrostatically confined single-electron or single-hole spin states and exchange coupling between spins for single- and two-qubit operations. Control pulses are superposed with DC voltages to implement quantum gates. The main layers of the gate structure include screening (orange), onsite energy control (blue), and interdot tunnel coupling control (brown) gates electrically isolated from each other by thin dielectric layers (gray). (**B**) Nuclear spin fluctuations in the substrate can be a dominant noise source for spin qubits, particularly in materials with no nuclear spin–zero isotopes. (**C**) Charge traps and two-level fluctuations can reside at the dielectric interface. (**D**) Electrical noise from the environment (materials, cryogenic system, control electronics, etc.) affects dot energy detuning and tunnel coupling. (**E**) Imperfect interface quality between the substrate and upper layer leads to inhomogeneity in the potential and the valley splitting.

spin states in both triple quantum dots (*144*) and double quantum dots (*145*). Currently, the implementation of the single spin and singlet-triplet schemes in silicon-based quantum dots has led to state-of-the-art single- and two-qubit gate times on the order of 100 and 200 ns (*146*) with $\mathcal{F}$ exceeding 99.6% and 98%, respectively (*147*, *148*).

Typical semiconductor qubit chips use a high-mobility 2D charge carrier gas formed either by chemical doping or electrostatic accumulation. A stack of electrodes with nanometer-scale dimensions is used to control on-site and interdot coupling energies. A single-electron transistor proximal to a qubit array acting as a highly sensitive electrometer (Fig. 3A) is used to perform qubit readout primarily by spin-to-charge conversion methods such as Pauli spin blockade (*143*) or energy-selective tunneling (*149*). As summarized recently (*150*, *151*), fabrication relies on physical mesa formation with reactive ion etching, ohmic contact formation by ion implantation and rapid thermal annealing, metallization and dielectric isolation primarily using e-beam evaporation and low-temperature oxidation, and metallization and gate region patterning with ~10-nm dimensions by means of e-beam lithography.

Overlapping gate stack structures with interface dielectric layers have become widely used in fabricating processors with larger numbers of qubits (*150*–*154*). These structures are especially important for silicon quantum dots, in which the relatively large effective mass requires a substantial reduction in lithography feature size (pitch < 100 nm, width < 50 nm) relative to larger-scale quantum dot designs in III-V semiconductors (*143*, *155*). Although we focus on gate-defined quantum dots, other technologies based on semiconductors, such as shallow donor quantum dot devices (*26*, *156*), generally follow similar fabrication procedures. Hybrid quantum systems with superconducting cavities integrated with semiconductor quantum dots (*157*, *158*) also show promising results for realizing long-range qubit interactions (*159*–*161*), but we focus on materials issues in spin qubit arrays using nearest-neighbor interactions.

Material choices

Initial demonstrations of quantum control of spins in semiconductor quantum dots were implemented in GaAs/AlGaAs heterostructures (*143*, *155*). Among various noise sources that limit the coherence time of spin qubits, the dephasing in GaAs was mainly limited by magnetic-field fluctuations arising from nuclear spins in isotopes such as ^{69}Ga, ^{71}Ga, and ^{75}As (*162*, *163*). Indeed, advanced dynamical decoupling and fast Hamiltonian estimation techniques improved qubit performance, with $T_{2,\mathrm{DD}} > 300\ \mu s$ (*164*), $T_2^* > 2\ \mu s$ (*165*), and single-qubit $\mathcal{F} \geq 99\%$. However, all stable isotopes of Ga and As have nonzero nuclear spin, so it is impossible to eliminate the source of fluctuating hyperfine fields in this material. This limitation has motivated the recent intense effort to implement quantum dots in Si, which has a much lower natural abundance of spin-½ isotopes (^{29}Si, 4.7%) that can be further suppressed by semiconductor isotope engineering (*166*).

The current state of the art is implemented in Si/SiGe heterostructures, Si metal-oxide semiconductor (Si-MOS) structures, and complementary MOS (CMOS) structures. In addition, early work exploiting spin-orbit interaction to enable fast electric control of spin states (*167*, *168*) has led to the active exploration of hole spin-orbit qubits in Ge and Si-CMOS quantum dot devices (*169*, *170*).

Sources of noise and dissipation

Various decoherence sources exist in semiconductor quantum dot devices, including

pure dephasing by fluctuating nuclear spins through the hyperfine interaction, paramagnetic impurities in the bulk material or interfaces, and charge fluctuation–induced decoherence mediated by the spin-orbit interaction.

Figure 3B schematically shows nuclear spins around a confined-electron spin qubit as a primary noise source. This noise source can be suppressed by isotopic purification of the host material, which is possible for any element with stable zero–nuclear spin isotopes (*166*). To fully make use of the limited amount of separated spin-free isotopes, such isotopes are used to grow thin single crystalline layers on top of natural substrates by means of chemical vapor deposition (CVD) and/or molecular beam epitaxy (MBE) (*166*). Single-electron spin qubits using enriched ^{28}Si CVD epilayers formed on natural silicon substrates have demonstrated more than an order of magnitude improvement in coherence relative to natural silicon, leading to T_2^* ~ 120 μs for gate-defined MOS quantum dots (*147*), T_2^* ~ 20 μs for gate-defined Si/SiGe quantum dots (*27*), and $T_{2,\mathrm{DD}}$ ~ 500 ms for electrons bound to phosphorus donors (*26*). Dynamical decoupling measurements reveal a noise spectrum consistent with $1/f$ noise in these studies (*27*), indicating that decoherence in these systems is limited by noise sources other than background nuclear spins. Indeed, with isotopic enrichment, Si/SiGe triple quantum dot devices have shown coherence times limited by surface or interface paramagnetic impurities, presumably introduced inadvertently during the device fabrication process (*171*). Isotopically pure ^{28}Si (>99.92%) epilayers grown on 300-mm wafers are currently moving toward industry-level production (*172*). It is also possible to isotopically purify Ge by removing 7.8% abundant ^{73}Ge that has a spin of 9/2 (*173*).

The density of carrier scattering sites in the bulk directly affects the ability to form a stable quantum dot at an intended location. It is common to use ultrahigh-purity bulk semiconductor substrates with a low-temperature electronic mobility exceeding a few square meters per volt-second (*174*). Even for high-mobility samples, T_1 can be limited by charge fluctuations in a strongly coupled electronic reservoir (see E_F in energy landscape of Fig. 3A) (*175*). Slow charge background drift or TLS behavior in the vicinity of a quantum dot can also hinder sensitive charge stability measurements (*176*) and limit coherence times. Through charge noise spectroscopy, root-mean-square (rms) charge noise on the order of a few microelectron volts is typically observed (*177*).

Charged defects—for example, in an insulating layer on the silicon—can lead to localization of electrons in unintentional parasitic quantum dots at low temperature and low electron density (*178*). In addition, trapped charges can be introduced to the gate oxide and other dielectric layers (Fig. 3C) during various high-energy processing steps, including ion implantation and plasma-based processes. Likewise, strain fields stemming from elastic distortions at metal/semiconductor interfaces can induce quantum dots at unintentional locations or even deplete carriers in nearby regions, motivating the use of polysilicon gates in some studies to reduce the strain field (*179*).

Modern gate-defined semiconductor quantum dots use Heisenberg exchange or capacitively mediated nearest-neighbor interactions (*146*, *148*, *180*) to achieve single- and two-qubit gates, and uncontrolled charge fluctuation (Fig. 3, C and D) sets the ultimate limit on the single- and two-qubit $\mathcal{F}$ as these interactions lead to electric coupling. Although little is known about microscopic sources and relative contributions stemming from bulk, interface/surface, or cryogenic equipment (*181*), recent work in Si/SiGe quantum dot devices (*182*) identified the role of nonuniform distribution of TLS near the surfaces in contributing to low-frequency charge noise, underscoring the importance of controlling defect densities in the gate stack.

Materials limitations to scaling

Although operating parameters such as qubit energy and qubit-to-environment tunnel coupling energies are tunable by many orders of magnitude in gate-defined quantum dots (*183*), scaling up will still require a high level of device uniformity and fabrication yield. Current efforts toward realizing scalable quantum dot arrays include electron confinement in foundry-fabricated quantum dot devices (*184*) and electron mobility characterization of wafer-scale ^{28}Si (*172*).

One major source of disorder in silicon quantum dots is in the interface between the silicon and the capping layer (Fig. 3E). This interface is engineered through strain, confinement, and electric fields to lift the valley degeneracy, which is crucial for achieving long coherence times (*185*) and ensuring spin-to-charge conversion efficiency (*186*). Atomic-scale steps and defects at this interface can lead to disorder in this valley splitting (*187*). Si-MOS quantum dots can have larger valley splitting than Si/SiGe because of hard confinement from the silicon oxide layer (*188*). However, the oxide interface can also be a source of larger disorder than the epitaxial interface of Si/SiGe quantum wells. Strong inversion asymmetry at the semiconductor/dielectric interface can also lead to spin-orbit interaction, allowing for new control schemes (*189*, *190*). Such schemes would require a high degree of spatial uniformity, particularly in the interface quality.

Arrays of ~10 quantum dots have been demonstrated in both silicon and GaAs as a preliminary step toward larger-scale integration (*191*, *192*). Fields associated with qubit excitations in quantum dots are localized within ~100 nm, which sets a natural length scale for integration. As such, standard CMOS-type 3D wiring, with wiring layers a few micrometers away from qubits, may be more compatible with quantum dot devices than superconducting qubits.

New material platforms

Harnessing the hole spin degree of freedom in Si and Ge is emerging as an attractive route in semiconductor gate-defined quantum dots (*169*, *193*). Relative to electron spins, holes in the valence band have two distinct advantages. First, the vanishing p-type atomic orbital at the nuclei leads to reduced contact hyperfine interaction for a given density of nuclear spins, thus allowing for long spin coherence times; second, their intrinsically large spin-orbit coupling allows for fast, purely electrical spin control. Prior work on spin-orbit controlled qubits has used electrons in InAs (*167*) and InSb (*168*) for fast electric control of spin states. However, the large spin-orbit coupling can couple to charge fluctuations and lead to short coherence time. Hole spins in Ge quantum dots are attracting renewed attention in this context owing to favorable balance between spin-orbit strength and coherence time (*169*). In terms of device fabrication, the small effective mass created by strain and quantum confinement leads to larger level spacings relative to silicon and allows for larger quantum dot sizes and easier fabrication. In addition, almost any metal can be used to make ohmic contact to confined holes in Ge without the need for local doping or implantation with associated high thermal budget. Hole-spin qubits in CMOS silicon (*170*), Ge nanowires (*194*), and Ge/SiGe heterostructures (*195*) have been experimentally demonstrated with single-qubit gate times of ≤10 ns, allowing for a ratio of coherence time to gate time exceeding a few hundred (*196*).

Similar to color-center qubits, allotropes of carbon can be a good host material for quantum dot spin qubits. Early demonstrations in carbon nanotubes have shown initial quantum dot confinement and spin control (*197*). Bandgap-engineered few-layer graphene is also emerging as a promising platform for hosting highly coherent and controllable quantum dot spin qubits (*198*), with the possibility of isotopic purification of nuclear spin–free ^{12}C. Recent experimental work (*199*) has demonstrated single-electron confinement in a double–quantum dot device fabricated on mechanically exfoliated bilayer graphene. However, reliable single- and two-qubit gate operations have not yet been demonstrated, as this requires control of the valley degree of freedom (just as in silicon) and methods for efficient spin-to-charge conversion for readout.

These challenges call for substantial developments in materials science, such as the growth of large-area, high–electronic mobility, few-layer graphene with strain-induced bandgap and valley splitting. Furthermore, as we make progress in gaining control over disorder in 2D atomically thin materials to enable electrically gated quantum dots (*200*), we can envision opportunities that might exploit both the spin and valley degrees of freedom for storing and transmitting quantum information, as recently demonstrated in bilayer graphene devices (*201*).

Color centers

Color centers are optically addressable qubits (Fig. 4A) that are encoded in electron orbital and spin eigenstates associated with single- or few-atom impurities in solid-state host crystals, most commonly diamond. The nitrogen vacancy (NV) center in diamond is the most widely studied system because of its long coherence time of several milliseconds at room temperature (*202*, *203*). The qubit state can be controlled with microwave pulses, yielding single-qubit gate times on the order of 50 ns (*204*) and two-qubit gate times on the order of 1 μs (*205*). At low temperature, the state can be controlled optically with gate times on the same order (*206*). However, the NV center's poor optical properties—low efficiency of emission in the zero-phonon line, susceptibility to local electric fields, and incompatibility with telecommunication fiber optics—have motivated the development of other systems, particularly for the application of long-distance quantum networks. In diamond, recent work has focused on the negative (*207*) and neutral (*208*) silicon vacancy (SiV) centers as well as similar group IV vacancy centers (*209*). Color centers in silicon carbide include the NV center (*210*, *211*), SiV center (*212*), vanadium center (*213*), and divacancy (*214*, *215*). Defects in other material systems such as the T center in Si (*216*) and rare-earth ions in solid state crystals (*217*–*219*) are also being explored. Although the qubits themselves do not require microfabrication, their assembly into functional devices and arrays requires patterning by ion implantation or high-yield growth, as well as fabricating structures in or on top of the host material to allow for local control and addressing. The implantation process introduces lattice damage and unwanted defects that give rise to electric and magnetic field noise, resulting in short spin coherence times and spectral diffusion of the optical transition (*220*, *221*). Both the rate and collection efficiency of photon emission can be improved by the fabrication of photonic structures (*222*–*226*). However, etching diamond (*227*, *228*) is highly susceptible to process contamination (*229*), making high-yield, scalable fabrication difficult.

Material choices

Color centers in wide-bandgap semiconductors such as diamond and silicon carbide can exhibit long coherence times at room temperature because these host materials feature high Debye temperatures and low spin-orbit coupling, which lead to low electron-phonon coupling and long spin lifetimes (*203*). Furthermore, recent advances in ultrahigh-purity diamond synthesis by plasma-enhanced chemical vapor deposition (PECVD) allow for commercially available bulk substrates with heteroatom impurity concentrations below the parts per billion (ppb) level (*230*), ensuring an environment with very low magnetic noise (Fig. 4B).

For example, diamond has been synthesized with PECVD using isotopically enriched precursors to achieve up to 99.999% ^{12}C abundance. In such host materials, NV center qubits with millisecond coherence times have been demonstrated (*231*–*233*). Similarly, recent work in CVD synthesis of SiC has allowed improvement in coherence time of the divacancy qubit in SiC by as much as a factor of 40, with $T_2^* \sim 375$ μs (*234*).

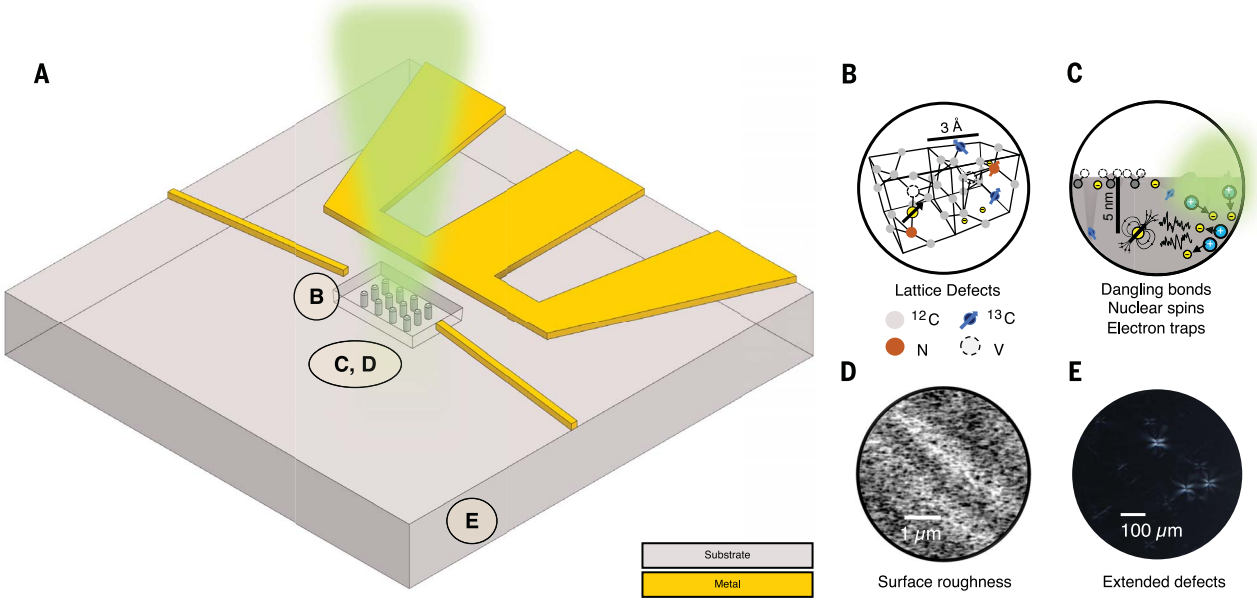

Fig. 4. Nitrogen vacancy (NV) center in diamond. (**A**) Schematic illustration of an NV center in a diamond qubit device. The NV center can be optically initialized, addressed, and read out. Etching nanostructures in the diamond allows for more efficient photon collection. Metal layers form coplanar waveguides for delivering microwave control pulses and electrodes for DC Stark tuning. (**B**) Atomic structure of an NV center and its local environment. Individual nuclear spins can be used as additional qubits. However, heteroatoms, paramagnetic defects, charged defects, and extended defects can contribute to spin decoherence. (**C**) Cartoon depiction of uncontrolled surface states that act as spin and charge traps, resulting in a rapid decrease in NV coherence with proximity to the surface. Optical excitation can ionize the NV center and the environment, causing charge instability of the NV center and the population of traps far from equilibrium. (**D**) Atomic force microscopy image of a diamond surface showing micropits (average surface roughness = 0.35 nm), a surface morphology syndrome that leads to a large density of electron traps. (**E**) Birefringent image of a diamond crystal showing strain associated with extended defects at larger length scales.

Sources of noise and dissipation

Many QIP schemes based on color centers require the qubits to be placed near the surface of the host crystal or in a nanofabricated structure. The spin coherence time of shallow NV centers in diamond within 30 nm of the surface degrades drastically (*229*, *235*). This degradation in coherence is accompanied by worsening charge state stability (*236*, *237*) and broader optical linewidths (*221*, *238*), indicating that the surface hosts excess electric and magnetic noise relative to the bulk. Diamond surfaces are particularly difficult to control because diamond is inert and hard, which makes etching and polishing challenging. The surface can host electronic defects that arise from uncontrolled surface chemistry and adsorbed contaminants (*239*), which lead to both magnetic noise and spectral diffusion. Recent work has established that rough surface morphology, dangling bonds, and disorder in surface termination can result in electronic traps that are apparent in x-ray spectroscopy (*229*). By correlating such measurements with qubit measurements, it was established that these traps give rise to a broadband magnetic noise spectrum (Fig. 4C). Local traps at the surface can also induce electron tunneling and cause rapid ionization of the NV center even in the absence of optical illumination (*236*, *237*).

Several surface terminations have been explored to mitigate these problems, including oxygen (*229*), nitrogen (*240*), and fluorine (*241*). In particular, high-quality oxygen termination after polishing and etching to remove subsurface damage extended the coherence time of shallow NV centers over the state of the art by more than one order of magnitude (*229*). Other ideal surface terminations have also been theoretically proposed (*242*, *243*), but controlling the surface chemistry of diamond without inducing surface roughness (Fig. 4D) or subsurface damage remains an ongoing challenge.

Materials limitations to scaling

Although some of the highest-fidelity single-qubit and two-qubit gates have been demonstrated in NV centers (99.9952% and 99.2%, respectively) (*205*), efforts to scale in this platform are relatively immature. Because of their efficient optical interface, color centers are particularly well suited to modular QIP schemes consisting of small quantum registers based on local nuclear spins, with nodes connected by photonic links (*244*–*246*). Color centers can exhibit substantial inhomogeneity and spectral diffusion across a substrate because of strain arising from extended defects (Fig. 4E) and local electric fields from charged defects that couple to the permanent electric dipole of the qubit. In NV centers, strain can lead to static shifts in the spin resonance transition frequency (*247*), which decreases the ensemble T_2^*. Strain also gives rise to static shifts of the optical transition that lead to an inhomogeneous linewidth in CVD diamond of >100 GHz (*248*), and local strain can also affect the energy splittings and selection rules in the excited-state fine structure. Efforts to synthesize low-strain diamond substrates are aimed at reducing this distribution. Separately, the inhomogeneously broadened linewidth caused by dynamic spectral diffusion can be as large as 1 GHz for charges that are fluctuating at ppb levels (*221*). This sensitivity to fluctuating electric fields is especially problematic in microfabricated structures (*238*). Such effects are less pronounced for color centers lacking a permanent electric dipole, such as group IV vacancy centers in diamond (*207*–*209*).

As another example, QIP schemes with arrays of atomic defects are typically based on dipolar or hyperfine interactions between defects (*249*, *250*), which requires exquisite control over both the strength and sign of the interaction. Large arrays will require control over the positioning of such defects at the nanometer or even subnanometer scale. For color centers, this is very challenging; incorporation during the growth process by means of delta doping allows for localization in depth but not lateral positioning (*233*, *251*), and ion implantation entails a large final distribution (straggle) in the positioning. Furthermore, for color centers that incorporate more than one atom or a particular geometric configuration, their probabilistic formation is also a limitation to scaling. Straggle in ion implantation is small enough that precise positioning with respect to photonic devices has been demonstrated with focused ion-beam implantation (*252*), but this approach does not provide a route to precise control over interactions among color centers. One demonstrated method for creating atomically precise arrays of phosphorus donors in silicon involves atom-by-atom manipulation in a scanning tunneling microscope to remove individual bonds that can be functionalized with phosphorus and subsequently overgrown with more silicon (*253*). Recent work with this approach showed precise atomic site control and exchange interaction–based two-qubit operations between electrons bound to phosphoros donors in silicon (*254*). Such methods have not yet been deployed in other material systems. An alternative is to create color centers in small molecules, which would allow for precise control over the position of qubits through synthetic chemical methods. Recent work has demonstrated optically detected magnetic resonance (ODMR) and T_2 of 640 ns for chromium in an organometallic complex (*255*). Integrating such qubits into nuclear spin–free environments and multiqubit assemblies with organic synthesis could create precisely tuned, large arrays of color centers.

New material platforms

Many possible defect-host combinations have not yet been explored. The main requirements for a host material are (i) stable spin-zero nuclear isotopes to provide a low–magnetic noise environment, (ii) high-purity synthesis to ensure low paramagnetic impurity concentrations, and (iii) a sufficient bandgap to host electronic transitions suitable for optical detection. Several color centers have been explored over the past two decades, but their discovery has been for the most part serendipitous.

Purely ab initio prediction of defect properties is difficult because of the mismatch in length scale between atomic defects and the extended lattice structure (*256*). Furthermore, the measured properties of color centers can be complicated by interactions with unintentional defects in the host material, such as through magnetic interaction, charge transfer, or Fermi level pinning. Ongoing experimental efforts in the community to look for new color centers in diamond and silicon carbide primarily use ODMR and single-atom fluorescence imaging techniques (*257*–*259*). This approach is cumbersome because it requires that fluorescence from a single defect is bright and stable enough to be observed by conventional means, and probing spin via fluorescence requires a particular level structure that may not be present or understood. An alternative approach is to perform a systematic search for defect-host combinations by deterministically introducing heteroatoms into high-purity hosts composed of atoms with stable nuclear spin–free isotopes through ion implantation (*208*, *260*), and then performing high-throughput characterization of hosts and defects. This requires a fully integrated materials pipeline including materials growth, implantation and annealing, spin and optical characterization, and theoretical modeling to provide feedback on spectroscopic measurements. One particularly intriguing area of exploration is to find new, nuclear spin–free host materials for rare earths (*218*, *219*) and transition metals (*213*, *261*), which have been recently demonstrated as good optical qubits with many of the same advantages as color centers (*213*, *219*, *262*) but currently suffer fast dephasing from nuclear spins in their environments.

Trapped ions

In ion qubits (Fig. 5A), information is encoded in electronic states within individual atomic ions, trapped within ultrahigh vacuum in systems operating either at room temperature or at temperatures as low as 4 K. Unlike the other qubit platforms discussed here, ions are isolated in vacuum and are not embedded in noisy solid-state environments [quantum processors based on individual neutral atoms (*263*, *264*) share this property]. As a result, materials considerations generally do not affect coherence of

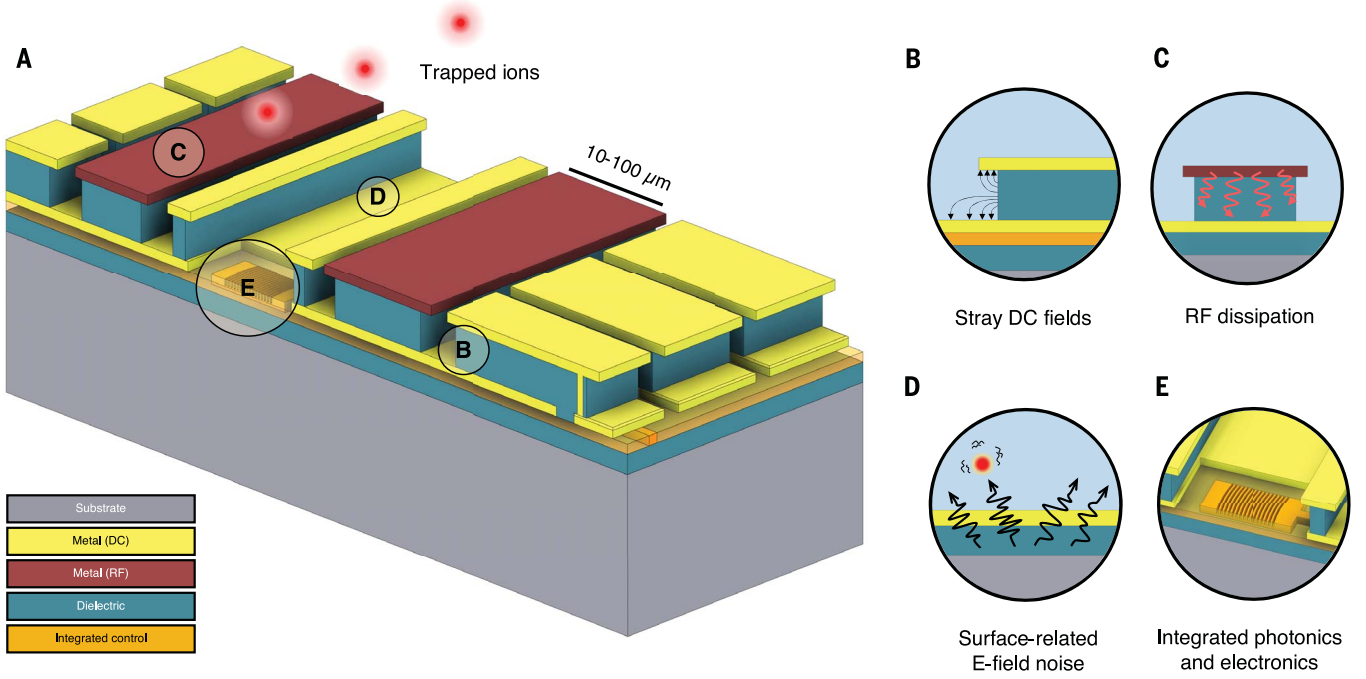

Fig. 5. Ion trap qubit. (**A**) Schematic illustration of elements of a surface-electrode Paul trap chip for ion qubits. Ions are confined by Coulomb forces from RF and DC electric fields resulting from potentials applied to the top electrode layer. Electrodes and potentials are designed to confine ions typically ~30 to 100 μm in vacuum above the surface. Individual ion qubits' coherence is generally not affected by materials considerations. Labeled panels indicate materials issues relating to sources of noise and drift affecting multiqubit operations, as well as components and challenges for scaling. (**B**) Stray DC fields from dielectrics, such as from photoinduced charging by the various laser fields that control ions, can perturb trap potentials. (**C**) RF dissipation in dielectrics can contribute to chip heating and exacerbate E-field noise. (**D**) Surface-related E-field noise can heat the ion motion often involved in multi-ion interactions; hence, they can introduce errors in multiqubit gates. (**E**) Photonics and electronics integrated within ion trap devices (e.g., for delivering light to a large ion array) are likely to play an important role in scaling, but they present various device- and materials-related challenges. [Graphics concept adapted with permission from (*353*)]

single-ion qubits. Materials problems, however, can contribute to error in logical operations between multiple ions and can have an impact on scaling considerations.

State-of-the-art trapped-ion quantum computing systems currently operate with ~20 individually controllable and fully connected qubits (*30*, *265*–*267*) and on the order of 50 to 100 ions in more specialized quantum simulation experiments (*268*). Depending on the choice of ion species and qubit transition, trapped-ion qubits can exhibit $T_2^* \geq 50$ s (*269*) and $T_{2,\mathrm{DD}} \geq 1$ hour (*270*). T_1 in such qubits can be unlimited for any practical purpose, although ions can escape traps, for example, through collisions with background gas particles. Although this loss occurs on time scales of many hours or days in typical experiments, in large ensembles of ions this process motivates the need for loss detection and reloading (*271*).

Because of their long coherence times and relative isolation from noisy environments, trapped ions have demonstrated the highest fidelities for basic quantum operations in any platform. These include single- and two-ion quantum logic gates realized in small-scale systems with 99.9999% (*269*) and 99.9% (*272*, *273*) fidelity, respectively, and single-ion state preparation and readout with >99.9% fidelity (*269*, *274*–*276*). Currently achievable two-qubit gate times are in the range of 0.5 to 100 μs (*272*, *277*, *278*), with single-qubit gates in the range of 10 ns to 5 μs (*269*, *279*). State preparation and readout are implemented with lasers, and logic gates are driven by laser beams precisely aligned to ions (*280*) or by microwaves (*279*).

Materials issues can affect logical operations on ions depending on the physical implementation of the device constituting the ion trap, as well as the control hardware providing electrical and optical signals required for computations. Electric field noise and drift can affect the ion motion, thereby affecting the degree of freedom used to implement logic gates between two or more qubits. To a small degree, ion motion can also affect high-fidelity single-qubit logic gates implemented with lasers, although this is negligible for microwave-driven single-qubit gates. These problems originating from materials become particularly important for ion trap architectures that require closer distances between the ions and surfaces, which are a potential route to larger systems. We summarize these issues below and also refer interested readers to a more specialized review (*281*).

Atoms with two electrons in the valence shell, whose singly ionized state thus has a single valence electron, are commonly used for QIP; these include isotopes of Be, Mg, Ca, Sr, Ba, and Yb, among others [see (*282*) for a discussion of possible qubit encodings within these ions]. Devices for ion qubits are built around the trap structures that confine them at designed locations. In the commonly used radio-frequency (RF) Paul traps, RF and direct-current (DC) voltages applied to trap electrodes typically confine ions within a few tens to hundreds of micrometers from electrode surfaces (*283*). Conventional 3D electrode geometries for Paul traps have been in use since the 1950s, whereas 2D "surface-electrode" or "planar" ion traps, developed during the past two decades, constitute a promising scalable trap architecture (*284*). All electrodes in such traps are fabricated in a metal layer on the surface of a chip, with ions trapped above (Fig. 5A), giving a practical path to complex arrays enabling trapping at multiple regions or trap "zones." Standard photolithography allows the straightforward fabrication of the ~10 to 100 μm–scale electrodes and few-micrometer gaps typical for such devices, thus directly leveraging a mature CMOS (*285*) and microelectromechanical system (MEMS) (*286*) fabrication

infrastructure to enable practical operation of multiple parallel trapping zones in arrays (*287*). However, the resulting trapping potentials are shallower and less symmetric than in 3D traps, prompting the development of traps with complex electrode arrangements in 3D (*288*).

Material choices

A variety of metals can be used for trap electrodes, where low resistance is important in minimizing dissipation from oscillating RF currents that flow upon application of RF trap voltages. Although many designs use simple evaporated or sputtered metal films, thick metal layers (>5 μm) achieved through electroplating are used in some traps; such layers are helpful in minimizing drift caused by any dielectric exposed in gaps between electrodes (stray DC fields; Fig. 5B) (*289*) and in realizing low impedance at the high frequencies essential for microwave-based gates (*290*).

Both the dielectric layers and the substrate supporting the electrodes can be an important source of dissipation. RF loss in these materials heats the trap chip (*284*), resulting in potentially higher electric-field noise (Fig. 5C) and making practical operation of large devices challenging. Substrates are chosen for high thermal conductivity to manage dissipation; common choices include silicon, sapphire, crystal quartz, diamond, alumina, and fused silica, depending on device operating temperature and fabrication requirements. Low-E dielectrics may help in minimizing RF resistive losses, which scale quadratically with capacitance. This issue may be particularly important for planar traps that incorporate RF ground planes (*285*, *287*), in which the bulk of the field is confined to deposited dielectrics as opposed to the substrate.

Sources of noise and dissipation

In ion traps, electrode surfaces generate both electric-field noise and slow drifts (Fig. 5D); neither affects the coherence of individual qubits, but the impact on ion motion can be substantial. Noise components resonant with the typical ~1- to 50-MHz oscillation frequencies of ions in traps can heat ion motion (*291*). Multiqubit gates are often mediated by shared modes of motion and as a result are susceptible to errors arising from this noise. In many traps, this noise does not constitute a dominant gate-error source, but it impedes reducing trap dimensions below a few tens of micrometers and contributes to error in some realizations of multi-ion gates (*276*, *292*).

Measurement of incoherent excitation of ion motion can provide a highly sensitive probe of electric-field noise (below $0.1\,\mu V\,m^{-1}/\sqrt{Hz}$ at ~1-MHz frequencies at the ion location); these measurements indicate that this noise is orders of magnitude higher than expected from Johnson noise (*293*). Although the origins of this noise remain unclear, studies by various groups provide key observations. The noise strongly increases in magnitude near surfaces of trap electrodes (*291*). It can often be suppressed by cooling traps to 4 K (*294*), which suggests that some processes generating noise are thermally activated processes. The magnitude appears to be rather insensitive to the choice of metal used for trap electrodes (*295*); more surprisingly, it appears to be insensitive to whether traps are operated with superconducting electrodes (*296*), which suggests that the noise arises from the surface rather than the bulk. This is also consistent with reductions in heating rates observed after various electrode surface treatments. For example, heating rate reductions by a factor of 100 at room temperature have been reported after in situ argon-ion milling of both gold (*297*) and aluminum-copper trap electrodes (*298*). Ex situ milling as well as plasma cleaning have also been shown to allow reductions (*299*, *300*); marked alterations to frequency and temperature scaling have been reported after milling (*301*). Modest reductions have also been observed after pulsed-laser cleaning (*302*).

Informed by these observations, a number of models have been put forth as to the origin of the noise (*291*). Adsorbed atoms (adatoms) that contaminate electrode surfaces may fluctuate and diffuse. Inhomogeneous electric fields on trap surfaces, known as patch potentials, may also play a role; a specific class consists of localized TLS. RF loss in dielectrics may also contribute, either by heating the trap materials or perhaps through the fluctuations fundamentally associated with this dissipation (*303*). However, the various trends observed in experiments, which include frequency scaling, temperature dependence, and trap-electrode distance (*301*, *304*–*306*), do not conclusively support a single model, and multiple mechanisms likely contribute (*291*).

In addition to ion heating from electric-field noise at megahertz frequencies, slow drifts in electric fields (up to 100 Hz) can shift ion positions on nanometer scales and cause drifts in oscillation frequencies; these quantities can be measured to reconstruct and analyze changes in the local charge environment (*307*). Such drifts have been observed in response to visible and ultraviolet light scattering off trap surfaces (*308*) and have been attributed to photoelectrons deposited on dielectrics (*309*). The need for precise control of ion oscillation frequencies for implementing multi-ion gates motivates the design of traps with minimal exposed dielectric.

Materials limitations to scaling

Trapped ions are compatible with the use of standard multilayer wiring in trap devices as implemented in CMOS processes, because the top metal forming the trap shields the ion from electric fields originating from the wiring and interconnect layers below (Fig. 5E). It therefore appears that with sufficient attention to shielding in design, complex wiring can be implemented by known means without sacrificing coherence. However, delivery of the relevant optical and electronic fields to multiple zones in arrays with low cross-talk and high precision entails substantial challenges for the controlling hardware. Current functional systems use 1D arrays of up to tens of optical beams, focused through bulk optics to micrometer-scale spots inside vacuum chambers to address individual ions within an ensemble (*265*, *310*). Such techniques have enabled some of the largest-scale experiments to date, but the susceptibility of such systems to drifts and vibrations (and resulting noise), along with scaling to thousands of beams or more in a 2D geometry, present major challenges. Photonic devices integrated and co-fabricated with planar ion traps have recently emerged as a promising route to address this problem (*276*, *311*, *312*). Integrated photonics may also facilitate scaling interfaces between ions and photons (*313*, *314*) to enable distributed computing; similar ideas have been implemented in color centers, as described above.

Materials enabling optical routing in waveguides, as well as active modulation and switching, present a particular challenge at the blue and ultraviolet wavelengths corresponding to electronic transitions in many ion species, as the majority of photonics research to date has focused on near-infrared wavelengths relevant to fiber optics and silicon photonics. Recent developments include realization of single-mode waveguides operating with propagation losses of ~8 dB/cm at wavelengths down to 390 nm in single-crystal AlN (*315*) or <3 dB/cm at wavelengths as low as 370 nm in amorphous Al_2O_3 (*316*). It will be important to assess the limits of active and passive nanophotonic material candidates (SiN, Al_2O_3, AlN, $LiNbO_3$, β-BaB_2O_4, and GaN, among others) at these wavelengths, along with their susceptibility to damage by short-wavelength radiation (*317*) and possible material treatments and passivation to protect against such damage.

Exploratory platform: Topological qubits

Finally, we address topological quantum computing (TQC), a long-range vision that relies on a foundational advance made by Kitaev (*318*), who showed how fault-tolerant quantum computation could be carried out using non-Abelian anyons, QPs that are neither fermions nor bosons and that obey non-Abelian statistics. Quantum computation algorithms are carried out by "braiding" these QPs so that they are topologically protected from decoherence by local perturbations such as electron-phonon and hyperfine interactions. Theory has rigorously identified several condensed matter systems in which non-Abelian anyons could be

realized, including certain fractional quantum Hall (FQH) states in high-mobility GaAs/(Ga,Al)As heterostructures (*319*), as well as Majorana zero modes (MZMs) in topological superconductors and superfluids (*320*, *321*) and in quantum spin liquids (*322*).

Theoretical predictions have prompted a surge of experimental activity in pursuit of material platforms for TQC. However, in strong contrast with the other QIP platforms we have discussed, the field still awaits the unambiguous experimental realization of a physical qubit. Possible experimental evidence for non-Abelian anyons was first reported in the $\nu = 5/2$ FQH state (*323*), but this has remained controversial (*324*). Two additional recent experiments have made major advances toward realizing non-Abelian anyons in the FQH regime, reporting fractional statistics (*325*) and anyonic braiding in the $\nu = 1/3$ FQH state (*326*).

The pursuit of non-Abelian MZMs in topological superconductors has involved measurements of a rich variety of materials, including vortices at topological insulator/superconductor heterointerfaces such as $Bi_2Se_3/NbSe_2$ (*327*, *328*), magnetic topological insulator/superconductor devices such as Cr-doped $(Bi,Sb)_2Te_3/Nb$ (*329*), hybrid narrow-bandgap semiconductor/superconductor (S/SC) nanowires [InAs(InSb)/Al(Nb)(NbTiN)] (*330*–*333*), Fe-chalcogenide superconductors (*334*), magnetic atom chains on superconducting surfaces (*335*), and hybrid Au/superconductor nanowires (*336*). Despite many sophisticated experimental efforts and tantalizing observations, definitive evidence for even the existence of MZMs (let alone their non-Abelian character) is still debated (*337*, *338*).

Material choices

The search for MZMs cuts across a broad swath of materials, a complete discussion of which is well beyond our present scope. As an illustrative example of the materials challenges involved in developing a TQC platform, we briefly summarize key issues in a system that has received the most attention to date, hybrid S/SC nanowires. Here, a pair of localized MZMs is predicted at the ends of a narrow-bandgap semiconductor nanowire caused by the combination of Zeeman splitting, spin-orbit coupling, and a proximity-induced hard superconducting gap (*330*). An in-depth discussion of the state of the art in this platform can be found in recent reviews (*332*, *333*).

The most common semiconductor components of this platform are InAs and InSb nanowires (Fig. 6A) (*339*). These are commonly grown by metal-organic vapor-phase epitaxy (MOVPE) (*340*) or MBE (*341*), respectively, using the Au-catalyzed vapor-liquid-solid (VLS) method, wherein a patterned array or a random arrangement of Au nanoparticles seeds vertical nanowire growth. Crystalline disorder within the InAs or InSb nanowire itself (caused by stacking faults or impurities) and disorder within the S/SC interface can lead to trivial subgap states that will decohere any existing topological MZMs. The synthesis of InAs or InSb nanowires of exceptional structural perfection is thus important, although simple metrics such as defect density or electron mobility for minimally acceptable structural and electronic quality have not yet been identified. The current state of the art in VLS synthesis yields reasonably high-quality nanowires with transconductance mobilities ~ 4×10^4 cm^2 V^{-1} s^{-1} in MOVPE-grown InSb nanowires (*340*). A metallic superconductor is then deposited either on an individual nanowire device (*331*) or globally on a nanowire array (*340*).

Superconductors that have been used so far include Al, Nb, NbTiN, and Sn. The transparency of the S/SC interface is crucial because a hard SC gap is required in the proximitized region. A promising approach to improved S/SC interfaces is the synthesis of well-ordered epitaxial crystalline Al shells on InAs nanowires (entirely grown through in situ MBE)

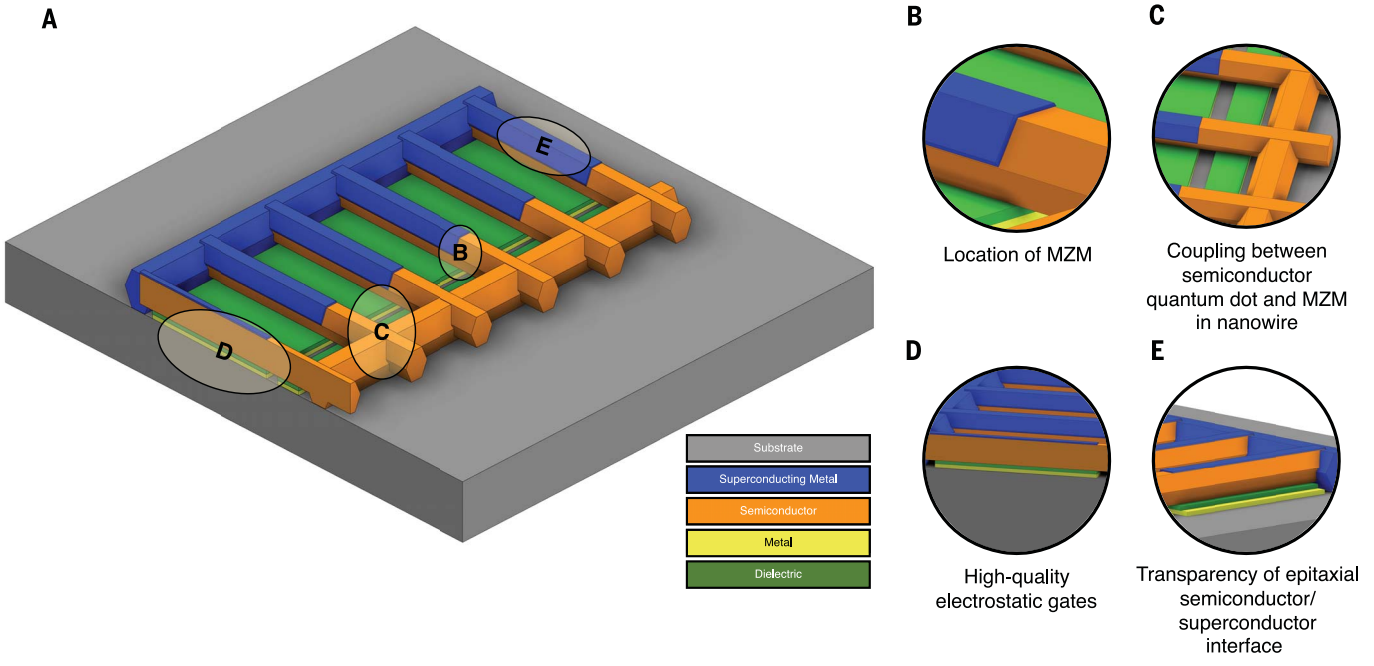

Fig. 6. Potential platforms for a topological qubit. (**A**) Schematic illustration of a proposed scalable topological quantum platform. Localized MZMs are realized at the ends of topological superconductor channels comprising narrow-bandgap semiconductor nanowires (e.g., InAs) proximitized by an epitaxially overgrown superconductor "shell" (e.g., Al). The elementary building block shown here is a one-sided "hexon" (*339*). The states of the MZMs are measured by selectively coupling to electrostatically defined quantum dots. (**B** to **E**) Progress has been made toward the synthesis of deterministic assemblies of hybrid semiconductor/superconductor nanowires (*342*–*344*). The key materials challenges in implementing such schemes include precise location of the MZMs (B), well-controlled coupling between the MZM and the readout quantum dot (C), well-characterized and quiet electrostatic gates (D), and transparent epitaxial semiconductor/superconductor interfaces that result in a hard proximity gap (E). The structural and electronic quality of the nanowires themselves is also a challenge because disorder leads to subgap states that can mimic signatures of MZMs.

(341) and on InSb nanowires (grown through two-step MOVPE/MBE with shadow masks) (342). Tunneling measurements show that both approaches markedly reduce the density of subgap states. Recently, selective-area epitaxial growth of in-plane semiconductor nanowires with solid source MBE (343), gas-source MBE (344), and MOVPE (345) has been reported. Although the quality of nanowires produced by selective-area epitaxy is still limited by defects such as misfit dislocations and stacking faults originating at the interface between the strained epitaxial layer and substrate (343, 344), these defects can be controlled in some cases, such as in plane MOVPE-grown InSb nanowires on InP (343). The key advantage of this approach is that by prepatterning the selective area mask, an entire network of interconnected nanowires can be grown. As a proof-of-concept example, complex networks of InAs and InSb nanowires (e.g., combs, honeycombs, loops) have been grown on InP (111)B substrates using prepatterned SiO_x masks, and phase-coherent quantum transport (Aharanov-Bohm oscillations) has been measured in these systems (343, 345).

Outstanding challenges

The central challenge in any TQC platform is to prove the existence of the qubit itself, the MZM in the case of hybrid S/SC nanowires. There are two aspects to this challenge: the observation of a state at zero energy with the requisite features of a MZM, and proving that this state obeys non-Abelian statistics through braiding operations. The former is probably achievable in the near-term future, whereas the latter remains a daunting challenge. In the hybrid S/SC nanowire case, initial attempts to observe MZMs relied on demonstrating a zero-bias conductance peak when tunneling into a putative MZM state located at the end of a proximitized narrow-bandgap semiconductor nanowire in the presence of a magnetic field parallel to the nanowire axis (330). The MZM state is formed only when the magnetic field exceeds a critical value such that the Zeeman energy $E_Z > \sqrt{\Delta^2 + \mu^2}$, where Δ and μ are the proximitized SC gap and chemical potential, respectively. This is predicted to produce a zero-bias conductance peak with a quantized value of exactly $2e^2/h$. Experiments carried out on hybrid S/SC nanowires have indeed shown signatures of zero-bias conductance peaks (331), and, in some cases, a nearly quantized conductance has been reported (332). However, the identification of such features with MZMs remains controversial (333, 346). In particular, structural disorder in the nanowire leads to trivial zero-energy subgap states (Andreev bound states) that are difficult to distinguish from genuine MZMs. Such zero-energy trivial subgap states can even occur without considering disorder, as a result of the inherent band structure and the inhomogeneous electrostatic potential in S/SC nanowires (337).

Materials limitations to scaling

Once the key problem of realizing a MZM is definitively resolved, detailed schemes have been proposed for scalable TQC platforms wherein S/SC nanowires are assembled for manipulating (braiding) and reading out MZMs. This stage of TQC will be faced with many of the interconnected materials science and physics issues that currently challenge other qubit platforms. An illustrative example of the challenges involved in building a scalable platform is shown in Fig. 6A (339). This scheme relies on the Coulomb blockade of an entire "hexon" of topological superconductor nanowires to create a single topological qubit. The hexon encoding protects the enclosed MZMs from "QP poisoning" caused by exchange of electrons with the environment. The key materials challenges encompass deterministic hybrid S/SC nanowire assembly, precise localization of MZMs (Fig. 6B), readout of MZMs by coupled quantum dots (Fig. 6C), well-controlled electrostatic gates (Fig. 6D), and transparent epitaxial S/SC interfaces that result in a hard gap (Fig. 6E).

Outlook: Materials research challenges and opportunities for QIP

All the quantum computing platforms discussed above have shown tremendous advances in recent years, and this rate of progress will be sustained if new contributors, in particular materials scientists, join the effort. For example, generic materials issues that constrain quantum device performance include heterogeneity of bulk materials, buried interfaces, and poorly characterized surfaces. This situation is reminiscent of the kinds of problems that have been solved for CMOS and other areas of the semiconductor industry, and there are undoubtedly opportunities for translating their solutions to the specific manifestations of these problems in QIP. We now conclude with an outlook on the opportunities for collaborative efforts between quantum scientists and materials scientists.

We identify three principal materials research frontiers of interest in this context. First, as we detailed earlier, understanding the microscopic mechanisms for noise, loss, and decoherence is crucial and would be accelerated by developing high-throughput methods for correlating qubit measurement with direct materials spectroscopy and characterization. Such a program will require teams of researchers working in concert with a large suite of characterization techniques. Second, relatively few material platforms for solid-state QIP have been explored thus far, and the discovery of a new platform is often serendipitous. It is thus important to develop materials discovery pipelines that exploit directed, rational material searches in concert with high-throughput characterization approaches aimed at rapid screening for properties relevant to QIP. Third, there are several materials issues that do not affect single-qubit operations but appear as limitations in trying to scale to larger systems.

High-throughput methods for characterizing qubits

Correlating qubit performance with materials and processing characteristics and eventually transitioning to unambiguously identifying the sources of decoherence is an exciting challenge. For QIP platforms, this process is complicated by device operation requiring millikelvin temperatures or ultrahigh-vacuum conditions. In addition, a complete picture of the qubit and its environment also requires precision at the micro–electron volt level and at subnanometer length scales. A variety of techniques with a range of modalities are thus needed, including those sensitive to atomic-level details in buried engineered lattices, chemically specific local spectroscopy probes of amorphous contaminants, and local characterization of poorly defined surface interactions. These are truly challenging regimes for theoretical approaches and experimental measurements alike, presenting a grand near-term challenge of inventing new materials analysis and quantum measurement techniques to study QIP systems.

Materials spectroscopy methods can be used to identify sources of decoherence in order to provide feedback on materials processing without iterating through the entire device fabrication and qubit characterization process. One recent example of success is the improvement of color-center qubits. Correlating qubit properties and photoelectron spectroscopy allowed for the identification of surface defects that lead to noise, which was used to devise new surface processing that yields shallow NV centers with spin coherence extended by more than an order of magnitude (229). The establishment of proxy diamond surface properties—surface morphology and bond angle orientation—will also enable rapid screening for future surface terminations and processing procedures to further improve NV centers.

Rapid device measurements are also critical for speeding up this feedback loop. Traditional approaches include building probe stations for higher-throughput measurements (121, 122, 347) and cluster tools with in situ processing (297, 298, 300, 302). Fast-turnaround cryogenic apparatuses are crucial for this effort. However, one drawback to building cluster tools with in situ probes is that it has not yet been established which measurement techniques will yield the most relevant information for qubit performance. For example, how would one set

up a high-throughput feedback cycle between a materials science group and a quantum measurement group for improving synthesis or processing protocols when a key parameter can only be accessed at 10 mK? Instead, one might imagine broad exploration of material parameters through a multimodal materials analysis approach that uses both rapid characterization methods to establish proxies and slower, more detailed characterization methods to identify microscopic origins of material properties. Once a particular set of methods and syndromes is established, cluster tools with integrated processing and analysis can contribute to more directed progress. Alternatively, developing device proxies to complement material proxies can greatly speed up this feedback loop. For example, direct measurements of dielectric loss-limited resonators can be made more rapidly than full superconducting qubit measurements (*60*, *348*).

A common theme we have identified is that all the QIP platforms discussed are plagued by electric and magnetic field noise arising from surfaces and interfaces. Establishing rapid materials analysis and device measurement feedback loops will allow for the systematic exploration of new fabrication schemes, growth and deposition methods, cleaning procedures, and surface processing to identify and address the sources of this noise. For example, adventitious carbon- and silicon-containing polymers are ubiquitous contaminants without careful surface preparation in vacuum (*229*), and it is unknown what impact these contaminants have on qubit properties and associated hardware. Furthermore, the exploration of alternative material systems may elucidate the role of oxides and interface layers in noise and dissipation, which will lead to new design principles for future material platforms.

Developing new materials for QIP platforms

Surprisingly, despite several decades of intense effort largely in the physics community to develop platforms for QIP, vanishingly few material platforms have been deployed in quantum processors. For superconducting qubits, only a handful of superconductors have been fabricated into qubits, leaving open a wide frontier of systematically exploring new bulk and thin-film materials, new heterostructures, and different crystalline phases of those materials. Another intriguing area of exploration involves replacing the Josephson junction with epitaxial heterostructures or single layers of 2D van der Waals materials (*349*). Rapid exploration of many material systems over the next few years appears to be highly feasible, although it would require a reorientation of the field from the current approach of focusing on device design to mitigate noise and loss.

Similarly, for color centers, very few defect-host combinations have been characterized thus far. The recent successes of new defects in diamond (*207*, *208*) and silicon carbide (*214*–*216*) show that there is room for a rational, systematic search for new systems. However, such a search would rely on the availability of ultrahigh-purity host materials, which will in turn require synthesis and characterization methods that can measure impurity and defect concentrations with high sensitivity and high dynamic range. This presents a new regime for solid-state chemists and material scientists, in which many materials are purified and processed to be as pristine as silicon, a material system that benefited from an enormous commercial impetus to perfect large-scale, single-crystal synthesis. In the short term, a substantial materials growth effort to explore the limits of material purity in a few promising systems would allow for the development of intermediate-scale quantum platforms. In the long term, such materials synthesis techniques would need to be scalable in order to support industrial deployment, and there are some major practical roadblocks that will need to be addressed, such as the availability of isotopically purified material.

For ion qubits, recent observations indicate possible material dependence of electric-field noise levels after surface treatment (*301*); systematic evaluation of surface treatments applied to traps of different material composition may help to shed light on underlying mechanisms and may eventually identify lower-noise platforms. Evaluating E-field noise at very low levels across large numbers of samples is a challenge that is feasible to tackle with existing methods but would require sustained, collaborative effort.

Finally, there are enticing opportunities for materials scientists seeking to join the hunt for a topological qubit, both by perfecting existing materials and by identifying new candidates. For example, with the use of diffusion-induced superconductors, a hard superconducting gap was recently achieved in high–hole mobility Ge-Si nanowires (*350*). For pursuing completely new materials in the search for MZMs, some broad rules combined with theoretical predictions provide guidance, including looking for materials with strong spin-orbit coupling, inverted bands, and superconductivity. Some of these properties may be found in surprising places, as exemplified by the discovery of coexisting superconductivity and topological Dirac bands in Fe(Se,Te) (*334*).

Scaling to large systems

Across several of the platforms we have discussed here, the current state-of-the-art devices and architectures are designed to avoid noise and dissipation. However, such choices now limit scaling up to larger systems. For example, transmon superconducting qubits are designed to avoid sensitivity to charge noise at the cost of reducing anharmonicity, and qubits are operated at fixed frequency to avoid flux noise, which makes two-qubit gates much slower. Furthermore, reducing surface participation in superconducting qubits enables longer coherence times at the cost of a large device footprint that gives rise to cross-talk among qubits.

Similarly, quantum dots are operated at the point of the charge stability diagram where the qubit energy is first-order insensitive to charge fluctuation (*351*), requiring exhaustive calibration of a large number of tuning parameters. In addition, the vanishing electric dipole moment in this regime often limits capacitance-mediated or exchange-based two-qubit gate speeds (*352*).

Ion traps are typically operated with ions at a minimum of ~30 μm from surfaces. Further reducing this distance would allow for higher-density arrays, but poorly understood surface-related electric field noise remains an obstacle to operating at smaller scales. If the underlying sources of noise could be addressed and mitigated, this would open up new possibilities for device designs and system architectures.

For topological qubits, once the qubit is unambiguously established, scalable architectures such as the hexon approach shown in Fig. 6A will require exceptional consistency in the fabrication of assembled nanostructures with well-controlled semiconductor/superconductor heterointerfaces.

Beyond these issues at the level of materials and devices, there will be major challenges at the systems integration and architecture levels to address. Using co-design concepts to tackle these challenges at all layers of the stack will be particularly important going forward. A key component of the co-design approach is the ability to define abstractions of material properties and their impacts on device performance, so that systems architects and algorithms developers can use them to design new quantum processors.

Concluding remarks

We hope to have communicated the emerging opportunities for materials scientists to participate in the grand challenge of developing QIP platforms. Apart from the technical issues that we have detailed, a meaningful transition from quantum information science to quantum information technologies will also require substantial investments to support broad community participation in tackling quantum questions, ranging from materials performance to quantum algorithms. Quantum computing began as a fundamentally interdisciplinary effort linking computer science, information science, and quantum physics; the time is now ripe for expanding the field by including new collaborations and partnerships with materials science.

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ACKNOWLEDGMENTS

We thank J. Park for technical support for producing figures; C. Murray, M. Carroll, A. Fuhrer, B. Cava, A. Houck, J. Thompson, and J. Chiaverini for critical reading of the manuscript and useful feedback; and the Kavli Foundation for support and encouragement for the discussions that led to this manuscript. **Funding:** Supported by NSF (RAISE DMR-1839199 and DMR-1752047), the Army Research Laboratory's Center for Distributed Quantum Information (W911NF-15-2-0060), the Horizon 2020 Framework Programme (820445, Quantum Internet Alliance), the Austrian Science Fund (F 7109), Samsung Science and Technology Foundation under project SSTF-BA1502-03, a National Research Foundation of Korea grant funded by the Korean government (MSIT) (2018R1A2A3075438, 2019M3E4A1080144, 2019M3E4A1080145, 2019R1A5A1027055), and the Creative Pioneering Researchers Program through Seoul National University. Also supported by the Institute for Quantum Matter under DOE EFRC grant DE-SC0019331, QNEXT DOE National Quantum Information Science Research Centers, and the Penn State Two-Dimensional Crystal Consortium–Materials Innovation Platform (2DCC-MIP) under NSF grant DMR-1539916 (N.S.); the Program Management Unit for Human Resources Institutional Development, Research and Innovation (grant B05F630108) (S.S.); and an ETH postdoctoral fellowship (K.K.M.). **Competing interests:** The authors declare no competing interests.

10.1126/science.abb2823

Materials challenges and opportunities for quantum computing hardware

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Science **372** (6539), eabb2823.
DOI: 10.1126/science.abb2823

Combatting noise on the platform

The potential of quantum computers to solve problems that are intractable for classical computers has driven advances in hardware fabrication. In practice, the main challenge in realizing quantum computers is that general, many-particle quantum states are highly sensitive to noise, which inevitably causes errors in quantum algorithms. Some noise sources are inherent to the current materials platforms. de Leon *et al.* review some of the materials challenges for five platforms for quantum computers and propose directions for their solution.

Science, this issue p. eabb2823