Deconvolution of Hot Carrier and Cold Carrier Injection in ZnO TFTs

P.Bolshakov, R.A. Rodriguez-Davila, M. Quevedo-Lopez, and C.D. Young
Materials Science and Engineering Dept., University of Texas at Dallas, 800 W. Campbell Rd., Richardson, TX, USA
Email: chadwin.young@utdallas.edu

***Abstract*—Positive bias instability stress (PBI) and hot carrier injection stress (HCI) was done on ZnO thin-film transistors (TFTs) with 100ºC Al_2O_3. The threshold voltage (V_T), transconductance (g_m), and subthreshold slope (SS) were monitored. HCI stress with two intermittent sense measurements where the first I_{DS}-V_{GS} is measured at the drain contact and the second is measured at the source contact to separate the contribution of the hot carrier and cold carrier injection on the V_T shift. PBI stress was done to determine the viability of the carrier injection separation using only HCI.**

Keywords - ZnO, TFTs, Al_2O_3, V_T, PBI, HCI

I. Introduction

Large area/flexible electronics may rely on oxide-based semiconductors that are desirable because of their compatibility with low-temperature fabrication required for large-area/flex-compatible technologies. ZnO is an oxide-based candidate to be used as an active layer in thin-film transistors (TFT) circuitry due to inexpensive processing and noteworthy electrical performance [1-3] and possible uses in flexible circuits [1]. For flex compatibility, deposition of high-k gate dielectrics at these low temperatures will be required as well. With all the low-temperature processing, thin-film transistor reliability must be evaluated due to threshold voltage (V_t) instability experienced by TFTs with high-k dielectrics [4-6]. In this work, TFTs are constant voltage stressed while monitoring critical parameters to assess the reliability of ZnO-based TFTs.

II. Device and Stress Procedure Description

Zinc-oxide TFTs are fabricated using traditional photolithography to pattern staggered-bottom-gate and top-contacts, as previously reported (**Fig. 1**) [7] with the final device in **Fig. 2**. The devices are fabricated on a glass substrate with patterned 135 nm of indium tin oxide (ITO) to serve as the gate electrode. Then, a 15 nm Al_2O_3 gate dielectric is deposited by atomic layer deposition (ALD) at 100ºC followed by 45 nm of zinc oxide as the semiconductor channel deposited by pulsed laser deposition (PLD). Stress testing was performed by applying stress voltages of either 5.5 V or 6.0 V, with intermittent I_D-V_G sense measurements.

III. Data/Results and Discussion

Low-temperature high-k dielectrics are essential for compatibility with large-area/flex electronics. A deconvolution of the contribution of hot carrier (HC) injection and cold carrier (CC) injection to the ΔV_T using only HCI stress measurements could allow for a reduction in measurements time and devices under test. To demonstrate consistent trends across devices, multiple TFTs were measured for each sense scheme at two different voltages. All devices had dimension of W/L = 160/20 μm, as shown in the plan-view picture of a device in **Fig. 2**. The **Fig. 3.** and **Fig. 5** illustrate the evolution of I_D-V_G degradation for devices stressed at 5.5 V and 6.0 V, respectively, with four different sense schemes. The first scheme in **Fig. 3a** is the conventional PBI stress measurement. The HCI stress in **Fig. 3b** and **Fig. 3c** is on the same TFT where **(b)** is the 1st sense measurement at the drain contact and **(c)** is the 2nd sense measurement at the source contact. Presumably the 2nd sense does not see the HC injection unlike the 1st sense measurement. The HCI in **Fig. 3d** is HCI with only a single sense measurement at the source contact. The same exact setup is done for **Fig. 5** at stress voltage of 6.0 V. For both stress voltage, the HCI at drain contact (**Fig. 3b** and **Fig. 5b**) appears to cause an increase in OFF current, suggesting degradation near the drain contact. One can observe V_T shifts with little to no degradation in either g_m or SS in all schemes. It should also be noted that the Δg_m in **Fig. 4** for stress at 5.5 V shows negligible degradation but the Δg_m in **Fig. 6** for stress at 6.0 V shows degradation at longer stress times. This suggests that near interface trap generation requires larger voltage stress and longer stress times to emerge. Extraction of the ΔV_T across all four sets of TFTs in **Fig. 4** and **Fig. 6** yields a more comprehensive understanding of the behavior of the V_T with stress time. At stress voltage of 5.5 V and 6.0 V, HCI with sense at drain contact demonstrates the larger relative ΔV_T. Presumably due to the contribution of both HC and CC injection. The other 3 sense schemes all show close agreement with each other in the ΔV_T. This is expected as the ΔV_T trends for the PBI and the two HCI sense at the source contact can be attributed to CC injection. The agreement between PBI and HCI at source also allows for separation of the HC injection and CC injection in terms of their contribution to ΔV_T. This can be done by subtracting the ΔV_T of HCI at the source contact from the ΔV_T of HCI at the drain contact as shown in **Fig. 7**. For both stress voltages, the red represents the HC + CC from HCI at drain contact while the blue and green, which are in close agreement, represent the CC from HCI at source contact and PBI, respectively. Furthermore, **Fig. 8** compares the ΔV_T after 1000 sec stress for both stress voltages. For stress of 5.5 V (red), the HC injection (Drain – Source) contribution is ~25% but for 6.0 V stress (blue), the HC injection contribution is ~15%. This is attributed to a larger increase in the contribution of CC injection compared to HC injection at the higher stress voltage. This suggests that with increasing voltage stress during HCI measurements, the component of CC injection is increasing at a higher rate than the component of HC injection. This can be explained by the larger gate area compared to the drain contact area resulting in a greater contribution from the field generated at the gate versus the field generated at the drain contact as shown in **Fig. 9**. Future work would involve smaller channel dimensions to determine their impact of HC and CC injection deconvolution using HCI.

IV. Conclusions

To determine the viability of using only HCI to separate the contribution of hot carrier injection and cold carrier injection in ZnO TFTs, multiple HCI sense schemes and PBI measurements are done. The results show that HCI with two intermittent sense measurements at the drain contact and the source contact can be used to attribute the percentage of contribution of hot carrier injection and cold carrier injection to the threshold voltage shift. Furthermore, the larger increase in cold carrier injection contribution compared to hot carrier injection contribution at higher voltage stress suggests that the contribution of each changes at different rates.

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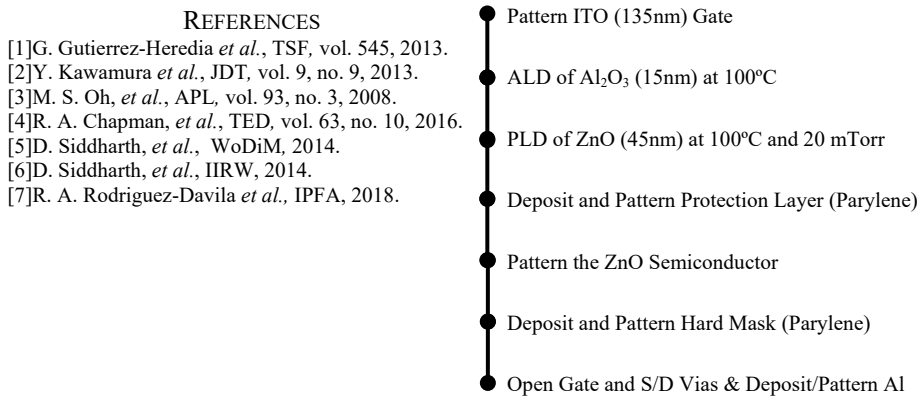

Fig. 1. Process flow for ZnO TFTs with both Al_2O_3 and ZnO deposited at 100ºC.

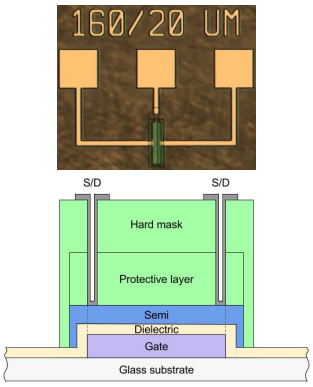

Fig. 2. Plan-view and cross-section schematic of the ZnO TFT structure with a channel width of 160 µm and a channel length of 20 µm.

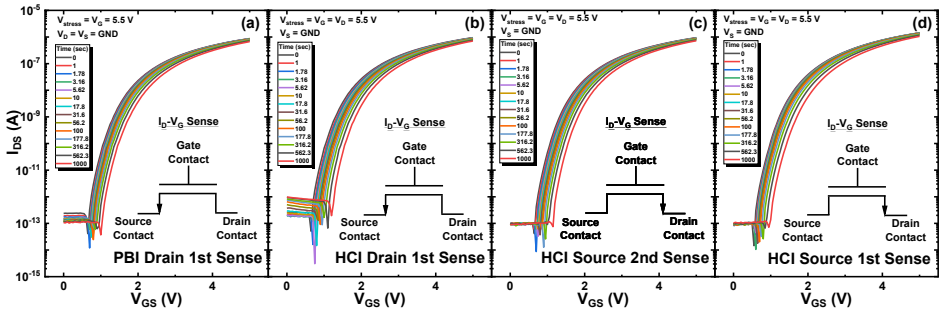

Fig. 3. Example I_{DS}-V_{GS} of TFTs with 100ºC Al_2O_3 stressed at 5.5 V. (a) I_{Ds}-V_{GS} for positive bias instability (PBI) stress with intermittent sense measurements during gate only stress. Hot carrier injection (HCI) stress with two intermittent sense measurements with the (b) 1st sense measurement at the drain contact where the stress voltage was applied followed by the (c) 2nd sense measurement at the source contact where no stress was applied. (d) HCI stress with the sense measurement done at the source contact where no stress was applied. For HCI with sense at drain contact (b), the degradation appears to increase the OFF current.

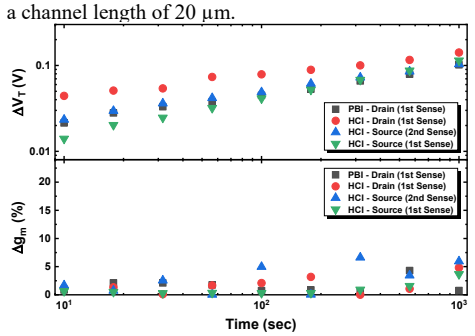

Fig. 4. The change in threshold voltage (V_T) and change in transconductance (g_m) for all four types of measurements at stress voltage of 5.5 V. The small change in Δg_m for all sense schemes suggests no interface state generation is contributing to the ΔV_T.

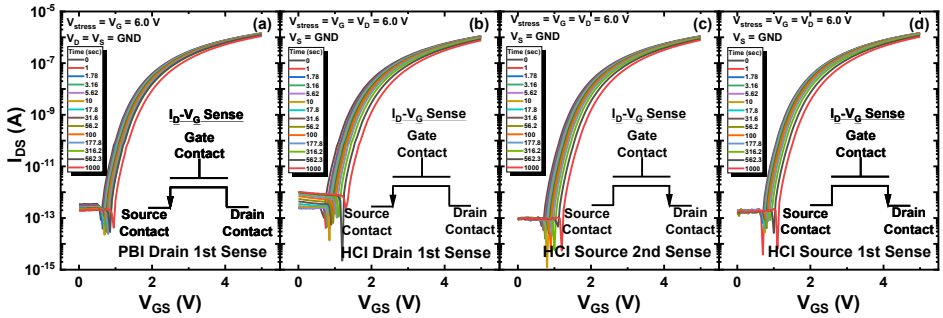

Fig. 5. Example I_{DS}-V_{GS} of TFTs with 100ºC Al_2O_3 stressed at 6.0 V. (a) I_{Ds}-V_{GS} for positive bias instability (PBI) stress with intermittent sense measurements during gate only stress. Hot carrier injection (HCI) stress with two intermittent sense measurements with the (b) 1st sense measurement at the drain contact where the stress voltage was applied followed by the (c) 2nd sense measurement at the source contact where no stress was applied. (d) HCI stress with the sense measurement done at the source contact where no stress was applied. For HCI with sense at drain contact (b), the degradation appears to increase the OFF current.

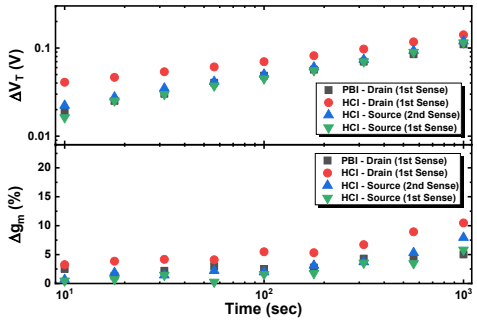

Fig. 6. The change in threshold voltage (V_T) and change in transconductance (g_m) for all four types of measurements at stress voltage of 6.0 V. The Δg_m appears to trend exponentially at higher stress voltage indicating interface state generation.

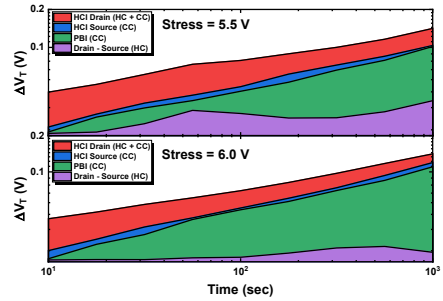

Fig. 7. Comparison of ΔV_T for the PBI (green) and HCI sense at drain (red) and HCI sense at source (blue). There is a close agreement between the PBI and HCI with sense at source suggesting cold carrier (CC) injection can be separated from hot carrier (HC) injection only using HCI measurements.

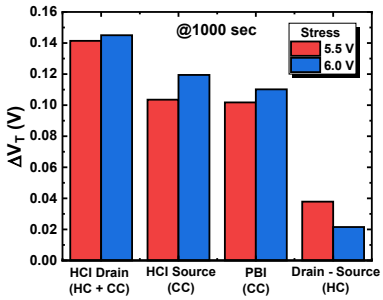

Fig. 8. Comparison of ΔV_T at a fixed time between the TFTs with stress at 5.5 V and 6.0 V. At a stress voltage of 5.5 V about 25% of the ΔV_T is attributed to HC injection while at 6.0 V about 15% of the ΔV_T is attributed to HC injection. This suggests that at higher stress voltages the contribution of HC injection to ΔV_T may become negligible compared to CC injection.

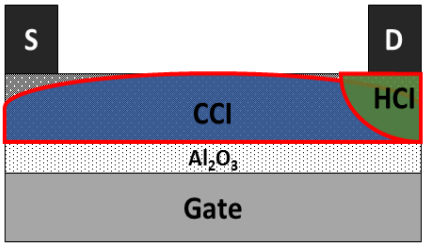

Fig. 9. Graphic demonstrating the fields generated from stress at the gate and stress at the drain. There is an overlap of the vertical field where CCI occurs and the lateral field where the HCI occurs. The relatively long channel length suggests the source side of the device would mostly be dominated by the vertical field and CCI.