Enhanced Threshold Voltage Stability in ZnO Thin-Film-Transistors by Excess of Oxygen in Atomic Layer Deposited Al_2O_3

R. A. Rodriguez-Davila, R. A. Chapman, M. Catalano, M. Quevedo-Lopez, and C.D. Young

The University of Texas at Dallas, 800 W Campbell Rd, Richardson, TX 75080, USA
E-mail address of the corresponding author: chadwin.young@utdallas.edu

***Abstract* — The prolonged bias stress of ZnO TFTs transistors with Al_2O_3 deposited at 100, 175, and 250°C is presented. Fully patterned bottom gated and top contacted devices serve as the test structures. The reliability study shows increasing threshold voltage shifting of 10.5, 18.6, and 27.2 % with deposition temperature with no significant change in the density of interface states for all the samples. Nevertheless, there is a dependence of the oxide trap states with stress time. The analysis of the transconductance as a function of the threshold voltage shifting indicates that oxide traps states near the interface are the dominant instability mechanism for significant stress times. The Al_2O_3 deposited at a temperature of 100 °C contains a higher concentration of oxygen compared to the other samples. This present oxygen excess could be filling oxygen vacancies present in the Al_2O_3, thereby resulting in a smaller ΔV_{TH}.**

***Index Terms*-- Thin Film Transistors (TFTs), zinc oxide, high-k, Photolithography, Reliability**

I. Introduction

High performance and stable transistors fabricated at low temperatures can enable the development of new electronic devices such as flexible and wearable electronics. Oxide-based semiconductors, such as ZnO and IGZO, have been widely used as an active channel in thin-film transistors (TFTs) due to its compatibility with low-temperature processing and exceptional electrical performance,[1-3] as well as its potential uses in flexible circuits. However, these devices suffer from threshold voltage instability, which negatively impacts the development of commercial devices. As a way to enhance stability, studies of gate dielectric engineering using bilayers [4-6] or nanolaminates [7] structures exist. However, these methods can be complicated to replicate because conditions and parameters (like thicknesses) need to be appropriately adjusted and tuned, which makes the implementation problematic. The present research addresses the prolonged bias stress study of zinc oxide TFTs with Al_2O_3 as the gate dielectric deposited under different substrate temperatures. The bias stress occurs in the saturation region emulating the TFT operation in the ON-state ($V_{DS} = V_{GS} > V_{TH}$) for 1000 sec, similar to HCI stress. The bias stress is interrupted periodically to obtain the transfer characteristic and quantify the TFT performance evolution as a function of the stress time.

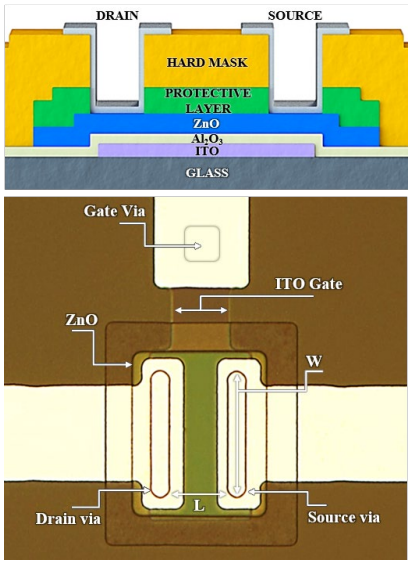

Fig. 1 (a) Cross section and (b) Plan view image of the fabricated TFT with W/L= 40/20 µm.

II. Materials and Methods

Fig. 1 shows a cross-sectional and plan view of the fabricated TFTs. The substrate consists of glass with ITO, serving as the gate electrode. The gate dielectric is Al_2O_3 (15 nm) deposited by ALD at 100, 175, and 250°C (three fabricated samples). Water vapor is the oxygen source, and trimethylaluminum is the Al precursor. Next, a 45 nm thick ZnO is deposited by pulsed laser deposition (PLD) at 100 ºC. No post-deposition anneal is done on the samples. A layer of 250 nm of polyp-xylylene-C (Parylene-C) is deposited by chemical vapor deposition at room temperature to protect and passivate the top surface of the oxide semiconductor from the subsequent photolithography steps. After patterning the first Parylene layer and semiconductor, a second layer of 250 nm of Parylene-C is deposited as a hard mask to protect the sides and fully encapsulate the semiconductor. This second Parylene layer is patterned to extend 20 µm from the edges of

the semiconductor. Source-Drain (S-D) vias are defined using oxygen-based reactive ion etching. Finally, 200 nm of Al is deposited and patterned to define S-D contacts. The designed channel lengths (L) were 10, 20, 40, 60, 80 µm, and the channel widths (W) were 40, 80, 160 µm. *The gate dielectric deposition temperature (DT) is the only variable in the fabrication process.* A similar fabrication process was reported before.[8-10]

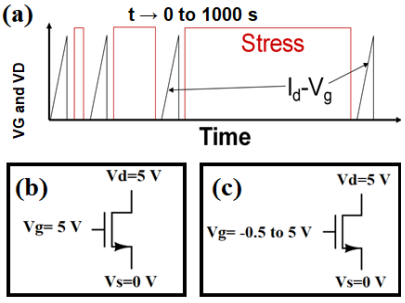

Fig. 2. (a) Bias stress vs. time, (b) Stress bias, and (c) Sense bias.

Reliability studies were performed at room temperature. The stress bias was applied to the gate (V_{GS}) and drain (V_{DS}) simultaneously from 1 to 1000 seconds with interspersed I_{DS}-V_{GS} sense measurements. These sense measurements were collected in the saturation regime with V_{DS} = 5 V. **Fig. 2** shows an illustration of the employed stress methodology. Chemical analysis was performed using energy dispersive spectroscopy line scans in transmission electron microscopy.

Transmission electron microscopy images were taken using a JEOL ARM200F with stem *Cs* corrector operated at 200 kV. Chemical analysis was performed using energy dispersive spectroscopy line scans were performed with an X-MaxN 180TLE detector (Oxford Instruments). The spatial resolution of the line scan is 0.27 nm/pixel, and the collection time is 0.4 s/pixel.

III. Electrical Performance of Devices

Representative transfer characteristics collected during stress time for the different Al_2O_3 DT are shown in **Fig. 3**. Electron trapping is evident with a positive parallel shifting of the transfer characteristic as a function of time for all samples. Following the simplest analytic model for field effect transistors,[11] the drain current in saturation can be expressed using equation (1); where C_{OX} is the gate dielectric capacitance per unit area, and μ_{SAT} is the saturation mobility. By extrapolating $I_{DS}^{0.5}$ as a function of V_{GS} under the condition of $V_{DS} > V_{GS} - V_{TH\text{-}SAT}$, the $V_{TH\text{-}SAT}$ is obtained from the fitted-line intercept with the x-axis and the saturation mobility (μ_{SAT}) from the slope. From the maximum slope obtained from the derivative of the transfer curve in the logarithmic scale, the Subthreshold swing (SS) is extracted (Equation 2).

$$I_{DS} = \frac{\mu_{SAT} C_{OX} W}{2L} (V_{GS} - V_{TH-SAT})^2 \quad (1)$$

$$SS = \frac{dV_{GS}}{d(\log I_{DS})}\Big|_{MAX} \quad (2)$$

The oxide capacitance, C_{OX}, is obtained from MIM capacitors that are onto the same fabricated sample. The change in $V_{TH\text{-}SAT}$ ($\delta V_{TH\text{-}SAT}$) is the difference between V_{TH} extracted at each stress time step and the initial value (t = 0 s), divided by the initial value. Similar calculations are done for δSS and $\delta\mu_{SAT}$. The evolution of the percentage changes, as a function of the stress time, is illustrated in **Fig. 4**. At the end of the stress, $\delta V_{TH\text{-}SAT}$ is about 12, 18, and 24 %, with increasing Al_2O_3 DT. The increase in V_{TH} can decrease the saturation mobility, as shown in **Fig. 4**. δSS shows independence of stress time for all of the samples.

Typically, $\Delta V_{TH\text{-}SAT}$ could be due to oxide states or interface states. The total oxide charge, Q_{OT}, can be determined using:

$$Q_{OT} = -C_{OX} \Delta V_{FB} \quad (3)$$

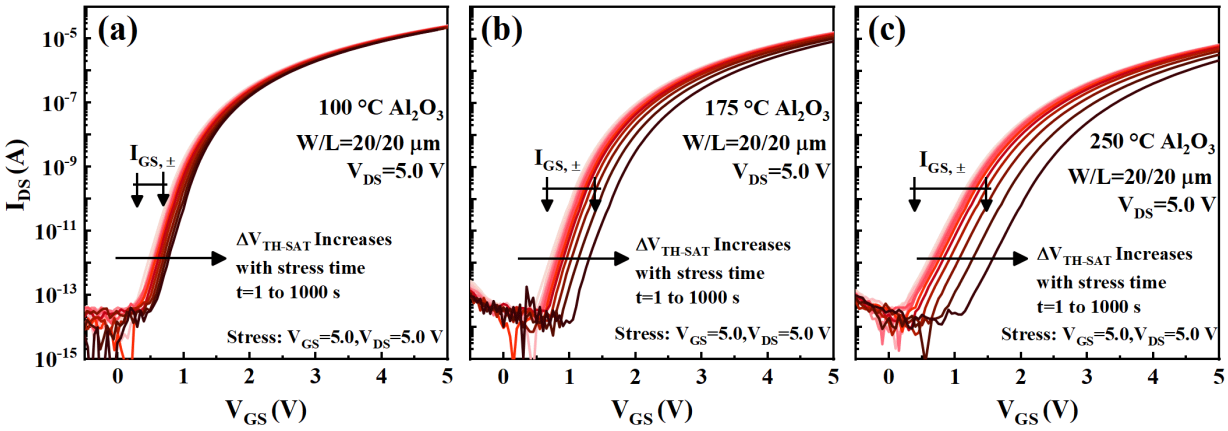

Fig. 3. Typical transfer characteristic for the sense interval and different Al_2O_3 deposition temperatures: (a) 100; (b) 175; and (c) 250 °C. Parallel and positive ΔV_{TH} is observed for all samples.

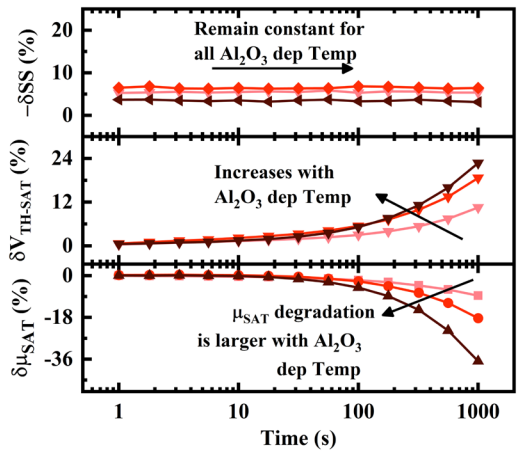

Fig. 4. Evolution of the change in saturation mobility, $V_{TH,}$ and subthreshold swing with time.

Where ΔV_{FB} represents the flat-band voltage shift due to charge trapping. Since the TFTs work in the accumulation mode, V_{FB} determines the voltage at which the channel starts accumulating; therefore, V_{ON} is the gate voltage corresponding to the flat band in the channel layer, which corresponds to the onset where I_{DS} values start increasing exponentially. Then, ΔV_{ON} could replace ΔV_{FB} in equation (4), and the change in dielectric trap density (ΔN_{OT}) due to the initial stress produced by the first and second cycle can be calculated using:

$$\Delta N_{OT} = -\frac{1}{q} C_{OX} \Delta V_{ON} \qquad (4)$$

The change in the interface trap density, ΔD_{IT}, can be related to the shift of SS after the stress using:

$$\Delta D_{IT} = \frac{C_{OX}}{\ln(10) qkT} \Delta SS \qquad (5)$$

The calculation of the ΔSS and ΔV_{ON} allows the estimation of the change in interface states and oxide traps states. The evolution of ΔD_{IT} and ΔN_{OT} as a function of Al_2O_3 DT is in **Fig. 5**. The independence of ΔD_{IT} with time suggests that δV_{TH} is independent of interface states. This change occurs due to the time-zero-instability, as reported previously.[9] ΔN_{OT} shows a near exponential increasing dependence with time, suggesting that the electron trapping occurs inside the dielectric, possibly in a border trap region in close proximity to the interface. However, since ΔN_{OT} includes the entire trap states inside the dielectric, it is difficult to know the exact origin of the traps at this time.

Fig. 5(c) shows the transconductance degradation as a function of the δV_{TH}. This evolution can be separated into three different regions for most of the samples. Region 1 is similar for all of the three samples, suggesting a correlated degradation mechanism. This is the initial filing of the pre-existing interface traps. In region 2, δg_m demonstrates an independence of the $\delta V_{TH,}$ which indicates that trapping now takes place in these existing oxide traps a short distance away from the interface. For 175 and 250 °C Al_2O_3 samples with reduced excess oxygen during ALD, a third region exists. This region can be due to trapping induced by the prolonged bias stress inside the dielectric and near the interface that can

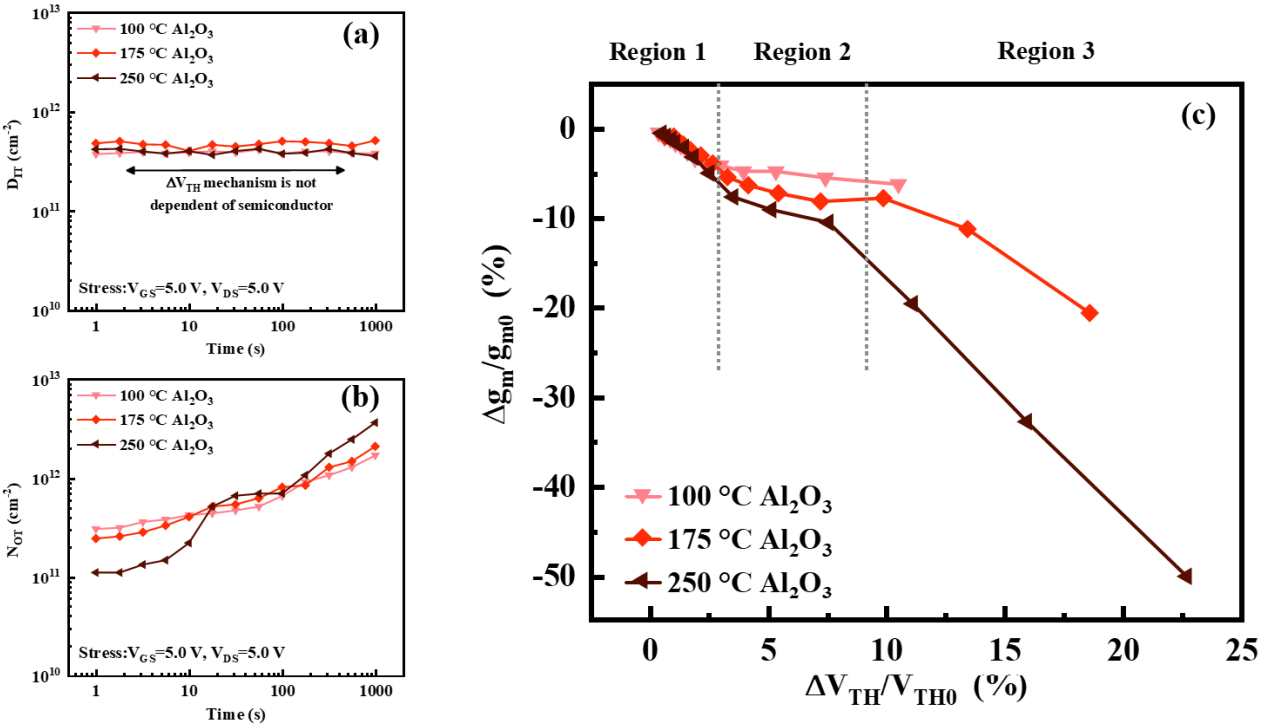

Fig. 5. Change in the density of interface states with stress time. (b) Change in the density of total oxide trap states with stress time. (c) Degradation of transconductance with V_{TH} shifting.

now have an influence on δg_m, since the density has increased.

IV. Induced Defect Formation Study

For this study, two devices from each kind are used: (1) Fresh device with no-stress; and (2) Device with gate and drain bias stress. The cross-sectional TEM samples (lamellas) are prepared using a focus ion beam (FEI Nova 200 nano lab dual-beam focus ion beam and scanning electron microscope) and the in-situ lift-off technique.[12] This technique utilizes the dual-beam FIB/SEM visualization and precision milling capabilities at the specified region of interest. A conductive film consisting of 100 nm of gold is deposited by electron beam evaporation on the TFT sample surface to prevent charging during FIB processing, a. Subsequently, the transference of the sample to the FIB/SEM tool takes place. A SiO_2 layer is deposited on the region of interest to protect the sample surface from subsequent damage. A thick layer of ion beam assisted Pt is deposited to provide mechanical stability during the milling and thinning process and provide better image contrast during TEM analysis. Ga+ ion beam is used to mill trenches until the lamella is about 1 µm thick. Next, it is directly attached to a tungsten needle which is operated using a high precision in-situ micromanipulator (Omniprobe) and then attached to the supported TEM grid using FIB-deposited platinum. Once attached to the grid, the lamella was further thinned down until electron transparency (<100 nm). A final polishing using a low ion beam current is performed on lamella sides to remove contaminants from the process.

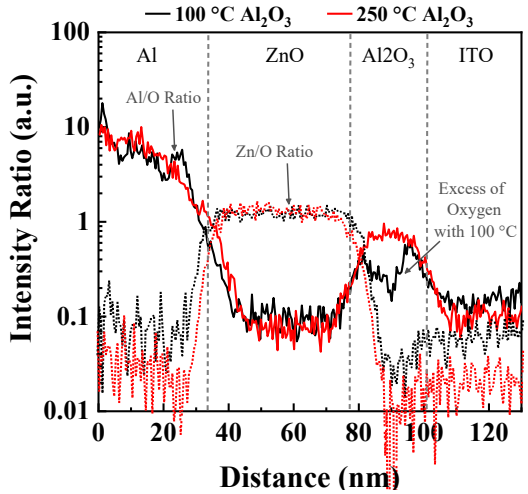

Fig. 6. Representative EDS line scan for 100 and 250 °C Al_2O_3 using transmission electron microscopy (TEM).

EDS lines scan using TEM is executed to understand the initial distribution of Al, Zn, and O across the TFT structure. **Fig. 6** shows the lines scan for Al/O and Zn/O ratios for 100 °C and 250 °C samples. As shown, an excess of oxygen exists in the 100 °C sample. Reports of oxygen excess in low-temperature ALD Al_2O_3 exist.[13] Nauman et al. reported[14] that oxygen diffusion from the gate (ITO) and residual -OH groups incorporated during the ALD deposition of Al_2O_3 are responsible for the excess of oxygen. Furthermore, Jeon et al. studied the growth of Al_2O_3 by ALD using isopropyl alcohol as the oxygen source instead of H_2O to minimize the excess oxygen. Nevertheless, they obtain a smaller concentration of oxygen, but it is still above the stoichiometric Al_2O_3 value. Cameron et al.[15] reported O/Al values changing between 2.5 and 3.6, while Shi et al.[13] reported values of 5 for O/Al. Therefore, the increase in the oxygen concentration in Al_2O_3 might be due to the non-reactive residual of oxygen precursor. This excess of oxygen can reduce the number of initially available oxygen vacancy trap states and also help reduce their influence during the prolonged bias stress, resulting in an overall smaller ΔV_{TH}. Figure 10 illustrates the proposed instability mechanisms for the 100 and 250 °C samples for the regions in **Fig. 7**.

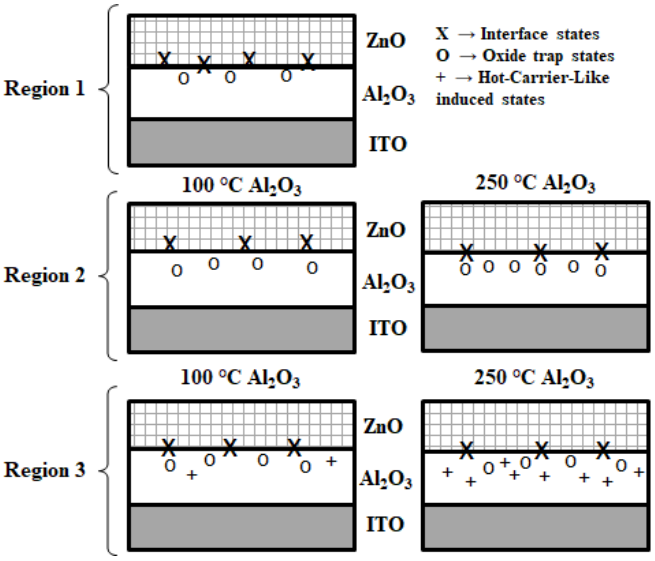

Fig. 7. Proposed ΔV_{TH} instability mechanism due to prolonged bias stress.

V. Conclusions

The reliability of nanocrystalline ZnO TFTs with different Al_2O_3 deposition temperature was presented. Reliability studies exhibit transfer curves shifting towards positive direction monotonically by incrementing the positive gate bias stress time. The SS does not show a detectable change, while δg_m and ΔN_{OT} demonstrate quantifiable change. The plausible mechanism is near-interface electron trapping inside Al_2O_3. The smaller ΔV_{TH} obtained in the 100 °C Al_2O_3 sample can be due to excess oxygen, reducing some oxygen vacancies during atomic layer deposition.

Acknowledgment

This work was supported in part by The National Science Foundation CAREER Award (ECCS-11139986), AFOSR

project FA9550-18-1-0019', CONACYT and RD Research Technology USA, LLC.

REFERENCES

[1] G. Gutierrez-Heredia *et al.*, "Fully patterned and low temperature transparent ZnO-based inverters," *Thin Solid Films,* vol. 545, pp. 458-461, 2013/10/31/ 2013.

[2] Y. Kawamura, M. Horita, Y. Ishikawa, and Y. Uraoka, "Effects of Gate Insulator on Thin-Film Transistors With ZnO Channel Layer Deposited by Plasma-Assisted Atomic Layer Deposition," *Journal of Display Technology,* vol. 9, no. 9, pp. 694-698, 2013.

[3] M. S. Oh, W. Choi, K. Lee, D. K. Hwang, and S. Im, "Flexible high gain complementary inverter using n-ZnO and p-pentacene channels on polyethersulfone substrate," *Applied Physics Letters,* vol. 93, no. 3, p. 033510, 2008/07/21 2008.

[4] F. H. Alshammari, P. K. Nayak, Z. Wang, and H. N. Alshareef, "Enhanced ZnO Thin-Film Transistor Performance Using Bilayer Gate Dielectrics," *ACS Applied Materials & Interfaces,* vol. 8, no. 35, pp. 22751-22755, 2016/09/07 2016.

[5] J.-W. Jo, K.-H. Kim, J. Kim, S. G. Ban, Y.-H. Kim, and S. K. Park, "High-Mobility and Hysteresis-Free Flexible Oxide Thin-Film Transistors and Circuits by Using Bilayer Sol–Gel Gate Dielectrics," *ACS Applied Materials & Interfaces,* vol. 10, no. 3, pp. 2679-2687, 2018/01/24 2018.

[6] C. Lin *et al.*, "Top-Gate Staggered a-IGZO TFTs Adopting the Bilayer Gate Insulator for Driving AMOLED," *IEEE Transactions on Electron Devices,* vol. 59, no. 6, pp. 1701-1708, 2012.

[7] T. Waggoner, J. Triska, K. Hoshino, J. F. Wager, and J. F. C. Jr., "Zirconium oxide-aluminum oxide nanolaminate gate dielectrics for amorphous oxide semiconductor thin-film transistors," *Journal of Vacuum Science & Technology B,* vol. 29, no. 4, p. 04D115, 2011.

[8] R. A. Rodriguez-Davila, I. Mejia, R. A. Chapman, C. D. Young, and M. Quevedo-Lopez, "Performance and Reliability Comparison of ZnO and IGZO Thin-Film Transistors and Inverters Fabricated at a Maximum Process Temperature of 115 °C," *IEEE Transactions on Electron Devices,* vol. 66, no. 9, pp. 3861-3866, 2019.

[9] R. A. Rodriguez-Davila, R. A. Chapman, P. Bolshakov, C. D. Young, and M. Quevedo-Lopez, "Impact of Al2O3 deposition temperature on the performance and initial stability of nanocrystalline ZnO thin-film transistors," *Microelectronic Engineering,* vol. 217, p. 111114, 2019/09/15/ 2019.

[10] R. A. Chapman *et al.*, "Quantum Confinement and Interface States in ZnO Nanocrystalline Thin-Film Transistors," *IEEE Transactions on Electron Devices,* vol. 65, no. 5, pp. 1787-1795, 2018.

[11] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John Wiley & Sons, Inc., 2006.

[12] D. B. Williams and C. B. Carter, *Transmission Electron Microscopy: A Textbook for Materials Science* (no. v. 2). Springer US, 2009.

[13] S. Shi, S. Qian, X. Hou, J. Mu, J. He, and X. Chou, "Structural and Optical Properties of Amorphous Al2O3 Thin Film Deposited by Atomic Layer Deposition %J Advances in Condensed Matter Physics," vol. 2018, p. 10, 2018, Art. no. 7598978.

[14] V. Naumann, M. Otto, R. B. Wehrspohn, M. Werner, and C. Hagendorf, "Interface and Material Characterization of Thin ALD-Al2O3 Layers on Crystalline Silicon," *Energy Procedia,* vol. 27, pp. 312-318, 2012/01/01/ 2012.

[15] T. O. Kääriäinen and D. C. Cameron, "Plasma-Assisted Atomic Layer Deposition of Al2O3 at Room Temperature," vol. 6, no. S1, pp. S237-S241, 2009.