6.3 A 0.9V Dual-Channel Filtering-by-Aliasing Receiver Front-End Achieving +35dBm IIP_3 and <–81dBm LO Leakage Supporting Intra- and Inter-Band Carrier Aggregation

Shi Bu, Sudhakar Pamarti

University of California, Los Angeles, CA

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Programmable receivers have drawn a lot of attention in recent years, especially those exploiting periodically time-varying (PTV) circuits. *N*-path filters and mixer-first receivers [1–3] achieve sharp filtering and good linearity but can suffer from high LO leakage (>–70dBm), which is not compliant with the FCC requirements [4]. In addition, they do not support multi-carrier operation very well [5].

The filtering-by-aliasing (FA) receiver front-end in [6] uses a resistor DAC to realize a PTV resistor, $R(t)$, followed by a passive mixer and an integrate-and-dump circuit to achieve sharp analog FIR filtering and moderate linearity (Fig. 6.3.1). However, the PTV resistor presents a time-varying impedance at the RF node, V_{RF}. While low S_{11} can be achieved in an average sense [6], it is difficult to guarantee desired filter response in the presence of complex source impedances, e.g., from parasitics. More importantly, if FA were applied in multi-carrier systems, it causes undesirable inter-channel corruption. Furthermore, achievable filter attenuation and linearity are limited by parasitics and switch resistance nonlinearities of the resistor DAC and the mixer.

This work presents a slice-based FA receiver architecture to address these issues without sacrificing the sharp filtering offered by FA. As shown in Fig. 6.3.1, the k^{th} slice is made of a resistor, $R_{unit}/2^{k-1}$, a transconductance (G_m) cell, $2^{k-1}G_{m,unit}$, and selection switches. The switches in the slice steer the current into a common integrating capacitor, C, when B_{k-1}=1 (i.e., slice is ON) or into the G_m cell's output in unity-gain configuration when B_{k-1}=0 (i.e., slice is OFF). Binary-weighted slices effectively make up a resistor DAC that can realize a PTV resistor, $R_{eff}(t)$, by selecting the *CtrlCode* appropriately to achieve desired sharp FA filtering. The passive mixer in the feedback enables filtering at ω_{LO}. Meanwhile, note that, whether ON/OFF, the k^{th} slice presents the same input resistance since its G_m cell is always in negative feedback. Therefore, the input resistance of the entire circuit is time-invariant and can be readily matched to R_s and not just in an average sense as in [6]. More importantly, FA operation is now tolerant of any complex impedances at V_{RF}. In effect, while the overall operation is PTV, the circuit can be treated and analyzed on a slice-by-slice basis in a time-invariant sense.

The proposed architecture offers several crucial benefits (Fig. 6.3.2). Firstly, the time-invariant input impedance enables multi-carrier FA operation free of interference between channels. This is because no time-dependent impedance interaction occurs, and the current to be integrated in each channel is not affected by others' operations. Secondly, all switches are placed in feedback, so switch non-idealities have negligible effect on filter shape and linearity. This is because the current from the k^{th} slice to the integrating capacitor is independent of the feedback network's impedance (recall Fig. 6.3.1). Furthermore, G_m-induced nonlinearity can also be easily made small by using a larger G_m to form a better virtual ground. This offers a scalable way of enhancing linearity. Thirdly, most of any LO leakage charge will go to the virtual ground rather than through the large resistors of the slices and onward to the antenna, thereby lowering LO leakage power significantly. The proposed architecture increases the noise figure (NF) slightly since the OFF slices act as an equivalent shunt resistor at V_{RF}. This can be mitigated to a certain extent as described later. Switch parasitics may also degrade filter response at much higher LO frequencies.

A dual-channel RF front-end was implemented, whose block diagram is shown in Fig. 6.3.3. Each channel is realized by a 4-path passive mixer and a 13b binary-weighted slice-based DAC; 13b ensures the DAC resolution does not limit filter shape. The DACs switch at $f_{clk}/2$ and the effective PTV resistor variations, $R_{eff1}(t)$ and $R_{eff2}(t)$, with a period of T_s, are sketched. The sampling and reset clocks are derived synchronously from the same f_{clk} signal. While not required, $R_{eff2}(t)$ is deliberately chosen to be an equal but shifted version of $R_{eff1}(t)$. This bestows the same filter shape on both channels; the shift guarantees that $R_{eff1}(t)$ and $R_{eff2}(t)$ are never simultaneously small, allowing the MSB slice to be shared thereby saving power and area, and reducing the NF penalty from the OFF-slice shunt resistance. The integrating capacitor is realized in ping-pong fashion to allow one capacitor to be integrating signal current while the other is being read and then reset. The 4-path passive mixers are integrated with the ping-pong capacitor banks. They are driven by two sets of 25% duty-cycled clock signals at f_{LO1} and f_{LO2}, respectively, to mix the RF current to baseband for integration. Note that f_{LO1} and f_{LO2} can be any value within the RF range.

The IC was fabricated in TSMC 28nm CMOS technology. The G_m cells are implemented as inverters and $G_{m,unit}R_{unit}$ is designed to be about 15, as an optimal trade-off between G_m linearity, R_{unit} noise, and power. All switches are implemented using transmission gates with equally sized NMOS and PMOS transistors, with LO switches designed to have an ON-resistance of 4Ω. The DACs are DC calibrated at start-up to compensate for mismatches; simulations suggest PVT variability has minimal impact on filter performance. MOM capacitors serve as the integrating capacitors, tunable from 10 to 80pF. The entire chip uses a single supply voltage of 0.9V, and the DC bias of the chain is about 0.45V set by G_m cells' biasing at reset and their buffer configuration. An on-chip generated 0.45V V_B is used to provide common mode for the capacitors during sampling. For 10MHz bandwidth (BW) filters centered at f_{LO1}=500MHz and f_{LO2}=740MHz, a current of 60mA is drawn by the entire chip at f_{clk}=2GHz. The system was verified to work up to f_{clk}=4GHz. In addition to the default high-performance (HP) operation mode, a low-noise (LN) mode can be enabled by disabling the shorting switches, $\overline{B_{k-1}}$. This decreases the net OFF-slice shunt resistance thereby reducing the NF by about 3dB at the cost of slightly degraded filtering and linearity. The HP or LN modes can be chosen for strong- and weak-blocker scenarios, respectively [7], using blocker-level detection, e.g., with an integrated blocker detector [8] or a spectrum scanner [9].

The sampled outputs are buffered externally for measurement. Fig 6.3.4 shows the measured concurrent filter responses with 10MHz BW at f_{LO1}=500MHz and f_{LO2} = 740MHz in HP mode. All measurements were performed with both channels ON and with f_{LO1} and f_{LO2} spaced by 240MHz. The transition BW is 32MHz with a stopband rejection (A_{stop}) of 53dB. The out-of-band (OOB) and in-band (IB) IIP_3 are 35dBm and 13.4dBm, and the blocker 1dB compression point (B_{1dB}) is 12dBm with a supply of mere 0.9V, since all nonlinearities are suppressed by the feedback loop. The filtering and linearity performance are similar for the two channels and do not vary appreciably across different LO frequencies.

Figure 6.3.5 shows the measured S_{11} and LO leakage power. A wideband S_{11} better than –14dB for the entire range of operation (0.1 to 1GHz) is achieved in HP mode and it is smaller than –10dB up to 2.3GHz. In contrast, the S_{11} is more poorly controlled and only <–8.5dB in LN mode. The worst-case LO leakage, measured over two chips, is less than –81dBm in HP mode, much smaller than the FCC requirements [4]. Even in LN mode, it is still below –69dBm. The rejection of signals in the other channel is roughly the same as A_{stop}.

Figure 6.3.6 compares this work with recent single- and multi-carrier designs. This work maintains the sharp filtering of single-carrier FA [6] even in a dual-carrier configuration. Compared to other multi-carrier works, the NF is slightly higher, while it achieves at least 19dBm better IIP_3 with only 0.9V supply. The achieved performance is comparable to or even better than the single-carrier ones with higher supplies. Figure 6.3.7 shows the die photo of the fabricated IC. The active area is 1.3mm^2.

Acknowledgement:
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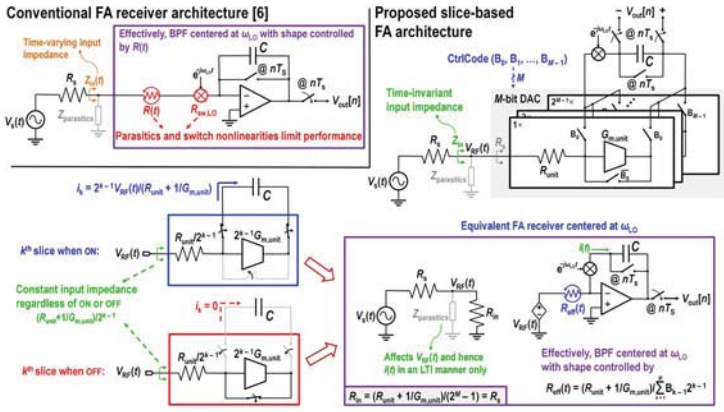

Figure 6.3.1: Conventional FA receiver (top-left), slice-based FA receiver architecture (top-right), operation of one slice (bottom-left), and the overall receiver model (bottom-right).

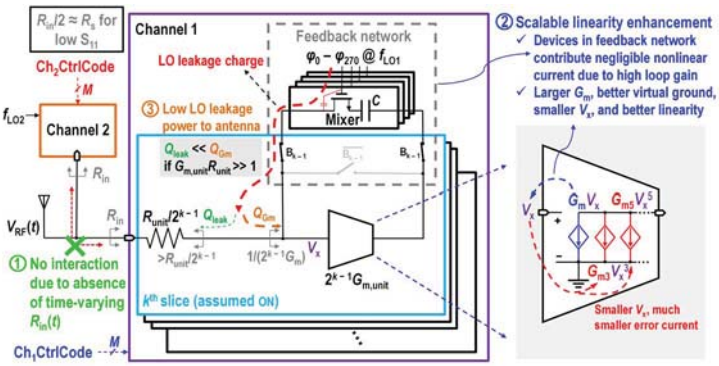

Figure 6.3.2: Illustration, using one ON slice, of 1) elimination of channel interaction; 2) scalable linearity enhancement; 3) and LO leakage suppression.

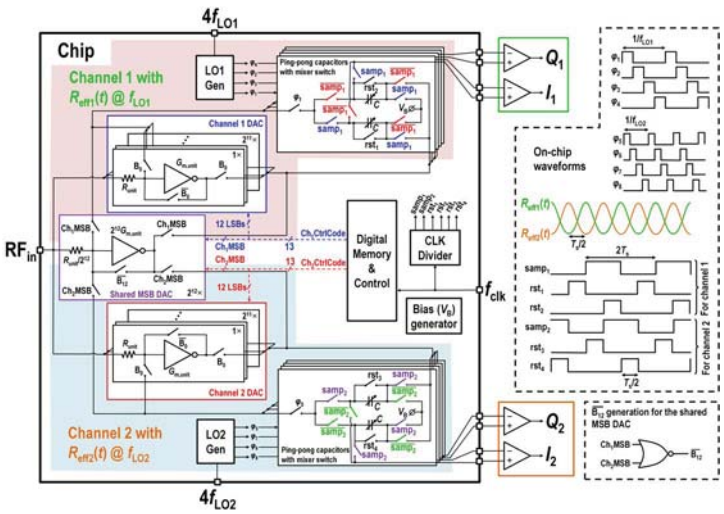

Figure 6.3.3: Block diagram of the implemented two-channel receiver front-end IC using the slice-based FA architecture.

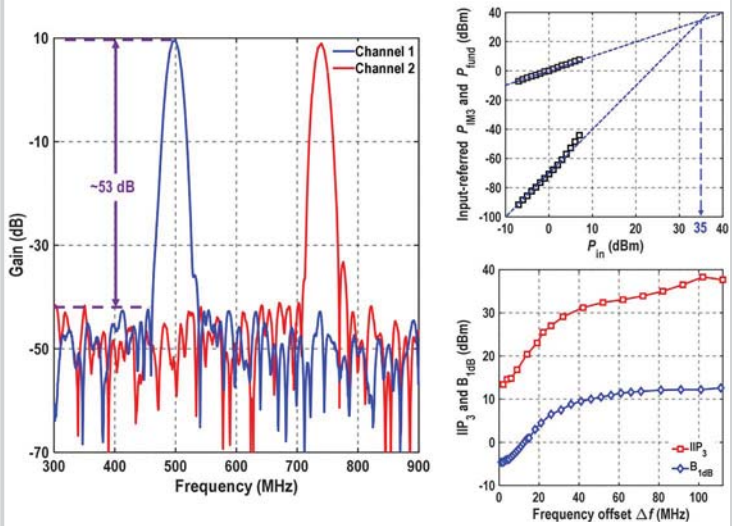

Figure 6.3.4: Measured concurrent-receiving filter shapes (left), input-referred P_{IM3} versus P_{in} at offset frequency Δf = 82MHz (top-right), and IIP_3 and B_{1dB} at different Δf (bottom-right) in high-performance (HP) mode.

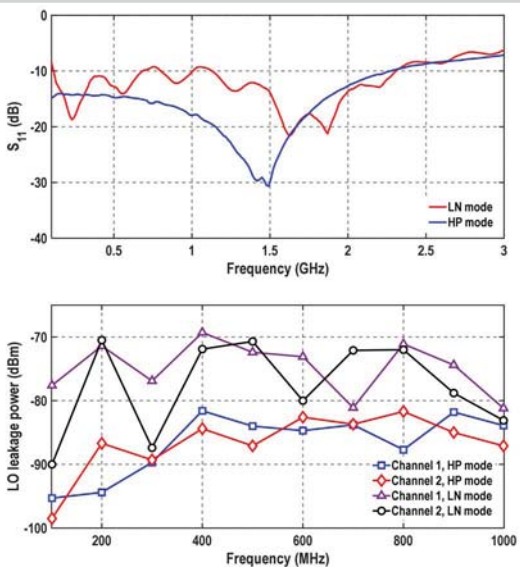

Figure 6.3.5: Measured S_{11} (top) and LO leakage power at different LO frequencies (bottom) in both high-performance (HP) and low-noise (LN) modes.

	Single-channel receivers/filters				Carrier aggregation receivers			This work	
	[6] ISSCC'17	[1] ISSCC'17	[2] ISSCC'18	[3] JSSC'20	[10] ISSCC'15	[11] JSSC'18	[5] JSSC'20*	LN mode	HP mode
Architecture	TI-FA	N-path	N-path	N-path	Current-domain signal process.	Code-domain N-path	Multi-branch mod.-mixer-clock	Slice-based FA	
CMOS technology	65 nm	28 nm	65 nm	28 nm	65 nm	65 nm	65 nm	28 nm	
RF freq. (GHz)	0.1–1	0.1–2	0.8–1.1	0.2–2	0.5–3	0.5–1.4	0.3–1.3	0.1–1	
RF input	Differential	Differential	Differential	Single-ended	Differential	Differential	Differential	Single-ended	
BW (MHz)	2.5–40	13	30–50	18	1–30	2	10–66	5–20	
No. of channels	1				3	2	2	2	
Carrier spacing	N/A				<100	<700	200–600	30–900§	
A_{max} (transition BW)	>58 (2.5× BW)	>47° dB (6× BW)	>17 (0.5× BW)	>27° (1.7× BW)	>30 (3× BW)	>28* (10× BW)	>60* (12× BW)	>44 (3.2× BW)	>53 (3.2× BW)
S_{11} (dB)	<–9	<–8*	<–7*	<–10*	<–10*	<–11*	<–6*	<–8.5	<–14
IB IIP_3 (dBm)	+8.2	+5*	+25	+1.5*	–28	–26	–6.9	+11.5	+13.4
OOB IIP_3 (dBm)	+24 (Δf/BW = 6)	+44 (Δf/BW = 12.3)	+24 (Δf/BW = 1)	+33 (Δf/BW = 4.4)	–4.8 (Δf/BW = 4)	–15 (Δf/BW = 10)	+16 (Δf/BW = 12)	+25 (Δf/BW = 8)	+35 (Δf/BW = 8)
OOB IIP_2 (dBm)	+64	+90	+61	N/A	N/A	N/A	N/A	+71 (Δf/BW = 8)	+82 (Δf/BW = 8)
OOB B_{1dB} (dBm)	+12 (Δf/BW = 6)	+13 (Δf/BW = 12.3)	+9 (Δf/BW = 1)	+12 (Δf/BW = 4.4)	–1	–11.8	+4	+12.6 (Δf/BW = 8)	+12.1 (Δf/BW = 8)
LO leakage (dBm)	N/A	N/A	–45	N/A	N/A	N/A	N/A	<–69	<–81
Sideband rej. (dB)	N/A				N/A	35	>48	>43	>49
Supply voltage (V)	1.2/1	1.2/1	1	1.2	1.2/2.5	N/A	1.2	0.9	
Power (mW)	75–99	34–96	80–97	146.6–179	84/channel	18/channel	19.6/channel	16–27.5 /channel	21–31 /channel
NF (dB)	7 @ 0.5 GHz	8.1 @ 1.3 GHz	7.6° @ 0.87 GHz	4.3–7.6	4.8	3.4–4.9	12.8	7.9 @ 0.5 GHz	10.8 @ 0.5 GHz
Gain (dB)	23	16	–4.2	13	50	38.5	53.2	12	10
Area (mm^2)	2.3	0.8	1.9	0.48	7.8†	0.31	1.8	1.3	

*Estimated from reported data. °High-linearity mode only. †Including on-chip frequency synthesizer.
§For achieving a rejection of the other carrier by more than 40dB. Otherwise the spacing can be arbitrarily small till the two channels become adjacent.

Figure 6.3.6: Performance summary and comparison to state-of-the-art single-channel tunable receivers/filters and multi-channel receivers.

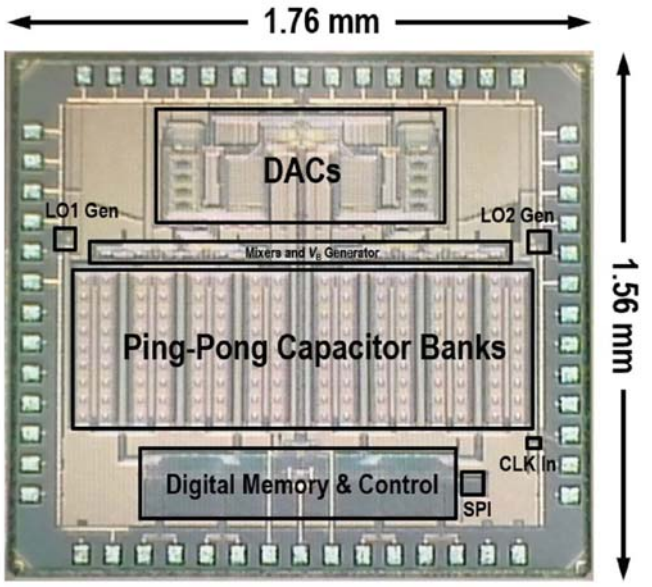

Figure 6.3.7: Die micrograph.

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