Passivation of III-V surfaces with crystalline oxidation

P. Laukkanen[1*], M. P. J. Punkkinen[1], M. Kuzmin[1,2], K. Kokko[1], J. Lång[3], and R. M. Wallace[4*]

[1] *Department of Physics and Astronomy, University of Turku, FI-20014 Turku, Finland*

[2] *Ioffe Physical-Technical Institute, Russian Academy of Sciences, St. Petersburg 194021, Russian Federation*

[3] *Comptek Solutions Inc. Voimakatu 14, FI-20520 Turku, Finland*

[4] *Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, Texas 75080, USA*

ABSTRACT

The control of interfacial physicochemical properties associated with device materials to minimize the impact of point defects on device performance has been a dominant theme in the semiconductor industry. The control of the density of such defects for silicon has been well established for metal oxide-semiconductor field-effect device applications through deliberate reactions with chemically congruent species, such as hydrogen. In contrast, the control of interfacial defects for technologically important III-V device materials is still an active area of research. Performance criteria for the III-V devices are demanding in terms of energy efficiency, material consumption, sensitivity, and speed. The surface reactions of III-V crystals, including the oxidation, are typically known to result in performance limitation for devices, causing significant degradation due to high defect-level densities at the surfaces/interfaces, in contrast to high quality bulk crystal regions. Here, we discuss the approach of utilizing atomically thin, ordered oxide interfacial layers of III-V compound semiconductors, since they provide a unique opportunity for metal-oxide semiconductor applications, compared to the more common approach to avoid the surface oxidation. The long-range ordered oxide interfaces have been obtained by

oxidizing cleaned III-V surfaces intentionally in ultrahigh vacuum conditions. This can be combined with different passivation methods to decrease interfacial defect density in III-V devices. We present the current understanding of the physical and chemical properties of the crystalline oxidized III-V materials, based on both experimental and computational models. The results are compared to those obtained by the current state-of-the-art passivation methods.

I. INTRODUCTION

After the demonstration of stimulated electroluminescence of AlGaAs/GaAs heterostructure diodes[1,2] as well as the field-effect transistor operation using modulation doped AlGaAs/GaAs heterostructures[3,4] in the 1970s, the photonics components and high electron-mobility transistors (HEMTs) have become established III-V compound-semiconductor device technologies which are currently used in many applications of photonics and wireless communication. For example, the III-V based light emitting diodes (LED), laser diodes, and detectors are key parts of the lighting and optical-fiber communication systems, and are finding further applications in medical technology (e.g. laser diodes) and the automotive industry via the light-detection and ranging (LIDAR) technology. While HEMTs were already commercialized in the mid 80s via low noise amplifiers, the use of HEMTs has increased substantially during the last decade because of significant development of monolithic microwave integrated circuits (MMIC) for wireless communication. Table I exemplifies selected milestones for III-V technology. It is common for such III-V devices that their performance criteria are demanding. The surfaces of III-V crystals which easily react with environment form one weak, limiting part for such device technologies.

Oxidation of the III-V surfaces serves as an example of problematic reactions. During the last 50 years, this surface phenomenon has been most often linked to research and development of the metal-oxide-semiconductor field-effect transistors (MOSFET) with a III-V surface channel. Indeed,

several excellent books and reviews have been published about that subject (e.g. Refs. 5-10). Although the III-V MOSFET has not yet been commercialized, an extensive body of the research results has provided a strong basis to fundamentally understand and control the surface-related degradation in many currently used III-V devices as well. For example, the obtained knowledge is essential to improve the efficiency and sensitivity of scaled LED and sensor components, as well as the reduction of the degradation of mirrors for laser diodes [e.g. Refs. 11-16]. There is also an intriguing relationship between the MOSFET and HEMT studies historically because the invention of HEMT, encapsulating the electron channel with high-quality epitaxial III-V heterointerfaces, thereby mimized the oxidation-induced surface/interface defect problem of the III-V MOSFET and thus suppressed the urgency for studies of this subject in the 1980s as low power applications were not a commercial priority at the time. However, the results obtained from the III-V oxidation studies have now become very relevant to further develop the HEMT gate structure for needs in wireless communication technology where power consumption is important.[17-19]

Research on the oxidation of silicon surfaces in the late 1950's and the early 1960's in combination with the invention of planar process technology eventually led to manufacturing of high-quality, amorphous SiO_2/Si interfaces for devices such as the microprocessor MOSFET.[20] This success led to intensive investigations to produce device-quality amorphous oxidized surfaces for III-V´s in the 1970s and 80s.[6] Those studies however revealed that the amorphous III-V oxidation is different from the well-established SiO_2/Si system, as described in previous reviews.[7-10,21-23] The difference between the oxidation of Si and III-V materials is discussed also in this review (Sections II and III). Since realizing that the intentional amorphous oxidation of III-V surfaces results in many defects, which are difficult to remove or passivate, the long-standing approach has included avoiding or minimizing any oxidation of III-V crystals in the research and development of III-V devices. This is indeed a very challenging target because it is very difficult to avoid the interaction of III-V crystalline (wafer) surfaces with oxygen and

the resulting oxygen incorporation into many III-V materials in practice. The oxidation is an energetically driven process for most III-V materials, and as such it is very difficult to avoid spurious exposure of the surfaces to an oxygen-containing environment during a multistep process of the device manufacturing (Section II). Such uncontrolled oxidation causes degradation in current III-V technology performance, and therefore it is relevant to understand the III-V oxide properties and to develop the passivation methods for decreasing the oxidation-induced defects and degradation in the devices.

Indeed, various passivation methods have been studied and developed for III-V surfaces to decrease interfacial defect densities during the last 50 years (Section VI). One potential solution to decrease the defect density is the epitaxial growth of insulator films on III-V´s because the interfacial bond structure resulting from an epitaxial interface naturally contains less point defects than the corresponding disordered interface typically associated with oxidation. Here, the well-established HEMT channel technology with a highly epitaxial III-V heterostructure interface provides a strict reference. However it is not straightforward, in practice, to manufacture such highly crystalline insulator/III-V stacks that have a minimal lattice mismatch between an insulator film and a III-V surface to avoid the strain-induced problems with increasing an insulator-film thickness. Furthermore, the heteroepitaxial insulator/III-V system should have the proper physical and chemical properties: e.g. large enough energy barrier for carriers and chemical stability in harsh conditions of further device processing.

Leveraging prior studies with amorphous oxide insulating layers on GaAs produced by molecular-beam-epitaxy (MBE) compatible methods (e.g. "GGO" $(Ga_2O_3)_{1-x}(Gd_2O_3)_x$), the demonstration of the epitaxial growth of cubic Gd_2O_3 was a significant step forward in oxide-epitaxy on GaAs and stimulated many further investigations in this field.[24-28] Among these were fundamental studies of the oxidation of atomically clean, reconstructed GaAs under ultrahigh vacuum (UHV) conditions as well as device demonstrations.[29-32] These investigations also revealed a significant potential of exploiting UHV technology in the development of insulator/III-V device interfaces, which has been also supported

by the results obtained via combining MBE and atomic-layer deposition in elegant way.[33,34] The investigations reviewed here emphasize the use of UHV technology and the importance of atomic scale control of III-V surfaces afforded by the UHV enviroment. It is noted that the commercial III-V growth technology incorporates MBE among the growth techniques exploiting UHV technology, and thus has been rendered as a manufacturable technology with useful yield. Moreover, an alternative method for growing epitaxial insulator/III-V interfaces using the now common atomic-layer-deposition (ALD) technique used in high volume semiconductor manufacturing where much higher pressures and precursor-surface reactions are employed during growth, has been recently reported.[35,36]

Although the III-V community has learned to avoid any oxidation of the surfaces, largely through exploiting epitaxial III-V insulating layers, the opposite approach - intentional oxidation of III-V materials - has been investigated with surprisingly promising results.[37-45] The resulting surface oxides have an amorphous or disordered nature, as expected, but also a clear indication of local interfacial crystallization has been measured for the thermal oxidation of InAs in non-UHV conditions.[45] Furthermore, in studies of the initial (or monolayer) oxidation of reconstructed III-V surfaces such as GaN, InAs and InGaAs, an ordered oxide structures were reported by several groups.[46-50] Taken together, these results suggested that proper III-V oxidation is not necessarily harmful to the device performance, as Robach et al.[37] concluded already in 1986: "Our results show, in contrast to what is generally assumed in the literature, that some specific native oxides are able to exhibit good electrical properties".

Currently, a significant body of the results shows that the monolayer oxidation of III-V surfaces offers a potential pathway, perhaps in conjunction with other passivation methods, to decrease the density of defect levels and to enhance the performance of III-V devices.[46-68] Our purpose here then is to review these results and report on the progress of the research with an eye toward device applications. Initially in Section II, we describe why spurious oxidation can be readily harmful to the performance of III-V electronics and photonics devices; why it has been avoided for several decades.

Concomitantly, we compare the III-V oxidation to the important reference case of SiO_2/Si. Then in Section III, we review basic experimental procedures to fabricate the crystalline oxidized III-V surfaces, including the first crucial step: cleaning and crystallization of III-V surfaces. Section IV summarizes the common characterization methods for the III-V interface research. The chemical and physical properties of the crystalline oxidized interfaces are described in Section V. Finally, in Section VI, we discuss the prospects to include the monolayer crystalline oxides for the passivation procedures in current III-V device technology, and make a comparison to the current state-of-the-art passivation methods.

II. EFFECTS OF OXIDATION ON DEVICE INTERFACES

Oxidation of most semiconductor crystals is an exothermic reaction. For example, the Gibbs formation energies ΔG for GaAs[69,70] (-67.8 kJ/mol), Ga_2O_3 (-999.7 kJ/mol), and $GaAsO_4$ (-891.6 kJ/mol) provide an idea how much the energy decreases when oxygen atoms are incorporated into the crystal, and oxygen bonds readily form with the semiconductor elements. One assumes that the ability to prepare an atomically clean and crystalline semiconductor surface is established (which is not trivial, as described later in Section III). The resultant surface reactivity presents a challenging situation to avoid spurious oxidation of a semiconductor surface during the subsequent step(s) of device processing, such as the growth of an insulator or metal film on the top of the cleaned semiconductor surface.[63] This is because even a short exposure to oxygen (or water) can cause the reaction and incorporation of oxygen atoms into a semiconductor. The challenge can be exemplified by the basic vacuum-technology result[71] from the kinetic theory of gasses that a solid surface becomes covered by one adsorbate layer in about one second when the environment pressure for a solid is as low as 1×10^{-6} mbar, which is already a suitable vacuum (clean environment relative to atmospheric exposure) for many practical thin film deposition systems to grow a metal or insulator thin film. In other words, the cleaned semiconductor surface can

become spuriously oxidized due to the residual gas pressure conditions, including the conditions through which the cleaned semiconductor sample is transferred to the film-growth apparatus, such as a process fabrication tool. Moreover, there are also other probable sources for the oxidation; several practical insulator films used in device processing are oxides: e.g. SiO_2, Al_2O_3, HfO_2, and TiO_2. Indeed, the growth conditions for such insulating films are very oxygen rich, and interdiffusion of elements across an oxide-semiconductor interface can readily cause oxygen incorporation into the semiconductor as well. The results presented for a very clean InGaAs surface in Ref. 63 provide an instructive example for this challenge.

Then it might be asked what concentration of oxygen has some significant effect. The density of atoms, and thus bonds, at semiconductor surfaces is typically on the order of 10^{14} to 10^{15} cm^{-2}. It is the chemical reactivity control ("passivation") of such surfaces, that inevitably exhibit dangling bonds (i.e. broken, unsatured bonds), with suitable insulating overlayers and reactants that is essential for useful interfaces in device applications. The Si MOSFET provides the most stringent interface state density requirement: it could be as low as 10^9 defect levels per cm^2eV to reach well-working MOSFET operation, *after* appropriate passivation of the silicon interface.[72-74] Thus a very small density of defects can be harmful, although other semiconductor devices are not as sensitive as the MOSFET to such surface defects. Indeed, many applications contain working III-V device components, as described in Section I. However, the comparison to the MOSFET defect-density requirement, achieved for silicon, together with the knowledge that III-V MOSFETs have been a very challenging goal gives one an idea of how much surface defects cause degradation in the current III-V devices in photonics and MMIC application for instance.

Figure 1 exemplifies such surface-related degradation. The III-V surfaces are normally covered by an insulator or metal film in devices; that is, the critical surface lies at a buried interface. This embedded property has hindered the physical characterization of interface properties (Section IV). A

thickness of the oxidation-modified III-V layer can be several nanometers,[5] depending on the manufacturing conditions for the insulator-semiconductor and metal-semiconductor junctions. For example, a 1-nm thick semiconductor film contains about six layers of atoms, each of which has the atomic density ~10^{14} cm^{-2}.

The reacted III-V layer contains oxidation-induced electron levels (short red lines in Figure 1) around the crucial energy region: the band gap. The oxygen-containing III-V surface can also include defects arising from interaction with carbon, hydrogen, or metal elements. The function of insulator-semiconductor interfaces is normally to enable the control of the current flow in the semiconductor side via the band offsets (barriers) between the semiconductor and insulator conduction or valence band edges, as schematically drawn in Figure 1b. The defect levels cause the recombination of carriers before they are directed to provide useful current flow. The defect levels might also trap carriers and become charged, affecting further the carrier transport properties. The interface defects may also increase a leakage current through the insulator.[75] Last but not least concerning III-V MOSFET, the Fermi-energy at the semiconductor surface might become locked (pinned) at some specific energy level in the band gap such that an external field is unable to modulate the band bending and therefore the Fermi level position over the gap.[6-9] In addition to the presented defect levels in the semiconductor side, so-called border trap states[76] (not shown in Figure 1) often appear in the insulator layers near the semiconductor surface.[77,78] Extreme care on surface preparation and passivation must be performed to enable clear distinctions between interfacial and border trap states.[23]

The Schottky and Ohmic metal-semiconductor interfaces also include oxidation-induced defects because it is hard to avoid an oxygen contact of a semiconductor surface during the metallization process, including the sample cleaning and transfer to a metal-deposition unit. It is of course worth noting that the metal-semiconductor interfaces are also challenging because of metal-semiconductor interactions.[79,80] On the other hand, a thin oxide layer between a metal film and semiconductor crystal,

acting as a tunneling barrier, has been proposed to solve the problem of metal-induced gap states through passivation.[79-82] Nevertheless, the oxidation-induced defect levels can again cause losses of carriers around the metal-semiconductor interfaces that connect the device to outside world. Figure 1c exemplifies how the electrons might recombine at an Ohmic-type junction of a photodiode before light-absorption induced carriers are collected into an external circuit. Furthermore, these defect levels can cause an increase in the reverse-biased leakage or dark current because the thermal excitation of electrons from the valence to conduction band increases via the gap levels.

A further interesting question is what kind of atomic-scale structural change(s), as compared to the bulk crystal, causes the electronic defect levels in the band gap. This is a very challenging defect-physics issue to experimentally measure, but the detailed theoretical studies have examined this question. The most established model at the moment is that the origins of the gap levels are (i) dangling bonds (i.e. unsaturated broken bonds) of group-III and -V atoms,[83] and (ii) group-V dimer bonds with antibonding levels.[84] In contrast, the oxidized phase of group-III or group-V element itself does not appear to cause defect levels directly in the area of the semiconductor band gap, but can result in a concentration dependent, oxygen-induced structural disorder which can result in gap states.[8,83-85] Another open question about the oxidized phases of group-III or group-V element is their band gap size; whether the oxidized phases still cause the electron levels just above the semiconductor conduction-band edge or just below the semiconductor valence-band edge. It is also emphasized that the impact of border traps in the insulator itself have been (typically) excluded in such analysis. The formation of different oxidized phases can lead to grain boundaries with enriched point-defect densities, which further can cause leakage paths.[5,7,86] Furthermore it is possible that the oxidation of a semiconductor surface continues (e.g. during process annealing), and the thickness of the oxidized layer increases. Then crystal quality of the oxidized layer can degrade rapidly. This is due to several reasons: There are usually many different metastable oxide phases which can form due to the process energetics and kinetics.[87-90] Most of oxidized phases

have also a clearly different crystal structure as compared to the III-V crystal structure, leading to a significant strain and its relaxation.[90] Therefore, it is not surprising that the resulting oxidized semiconductor surfaces are normally amorphous in structure.

Such amorphicity holds true also for the most famous oxidized semiconductor system: SiO_2/Si. SiO_2 films remain amorphous in most applications, including films that are grown at high temperatures even around 1000 ºC. Interestingly, an ultrathin interface layer (0.5 nm) between the Si crystal and amorphous SiO_2 film has been reported to have a well-ordered, crystalline tridymite structure of SiO_2 after a specific high-temperature oxidation treatment of Si[91] or with lattice mismatch-induced strain.[92] There are also other observations which support that monolayer crystallization of SiO_2 occurs under suitable conditions.[91-96] The presence of such an ordered oxide monolayer might be one key difference between the SiO_2/Si device interface and conventional III-V interfaces. A well-ordered interface layer naturally includes less point defects than the corresponding disordered layer as a majority of the interfacial dangling bonds is satisfied assuming a reasonable bond length is available. Furthermore, when one considers the manufacturing process of high-quality insulator/Si interfaces with low defect densities, the process steps often include a high-temperature rapid annealing step near the temperatures where SiO_2 decomposes. This provides another significant difference between the Si and III-V oxides. Namely, SiO_2 can be removed from a Si surface by vacuum heating (around 800 ºC) but a similar removal of III-V surface oxides by vacuum heating is very difficult because most III-V crystals start to decompose due to III-V bond scission/desorption before their oxides do.[97-99]

Finally, as noted previously, the method to passivate a major part of the remaining Si dangling bonds chemically by careful hydrogen incorporation into the interface, decreases the interface gap-level density to the 10^{10} $cm^{-2}eV^{-1}$ or lower range, allowing the proper MOSFET operation.[72-74,100] For the III-V interfaces, a similar hydrogen-passivation recipe resulting in similar interface state densities has not yet been found,[101-106] but the sulfur treatments have provided promising results (e.g. Refs. 107-

112). The hydrogen and sulfur passivation are described later in Section VI. Furthermore, crystalline oxidized III-V surfaces reviewed in this work might provide a step toward the interface control, analogous to the crystalline (tridymite) SiO_2/Si interface layer. Moreover, very promising results have been found from ab initio calculations: an energetically favored crystalline Ga_2O_3-type thin interface layer between GaAs and HfO_2 can provide a defect-level free gap.[85,113,114] This means that by finding proper parameters for the growth of HfO_2/GaAs gate dielectric structure, one should be able to decrease the interface defect density significantly through an ordered oxide monolayer. Indeed the previous experiments support that a favorable interface can be formed with amorphous (and polycrystalline) Ga_2O_3 film deposition on GaAs.[115-118] Of course, bonding is a major difference in the oxides of Si and III-V′s: namely the covalent-type bonding structure of Si in SiO_2 vs. ionic-type higher coordination bonding of the III elements in their oxides. It is important to note that the group V oxides resemble covalent type SiO_2-type using electronegativity arguments.[119]

III. PREPARATION OF MONOLAYER CRYSTALLINE OXIDIZED SURFACES

The first crucial step is the cleaning of III-V surfaces from spurious oxides and carbon contaminants. This issue has been indeed investigated intensively because, as described in Section I, avoiding the formation of the surface oxides has been the long-standing target in conventional III-V technology. A comprehensive review the cleaning procedures is beyond the scope of this work, and so we focus initially on wet chemical treatment(s) as this is one of the most used procedures in device fabrication technology, and because it can be readily included in various steps of the industrial process of III-V device components. In contrast, an ion sputter-cleaning approach, which is a common surface-science method to remove surface contaminants, clearly introduces surface disorder. Furthermore, in some specific cases, covering a III-V surface with a protective As or Sb “capping” film in the epitaxial growth system (e.g. using MBE) can be also utilized, which provides a well-ordered crystalline starting

surface after removing the As or Sb cap by the thermal desorption in ultrahigh vacuum (UHV) conditions. However, III-V components become often exposed to an oxygen-containing environment in several different processing steps associated with device fabrication, and the wet etching is a simple and quick method to be integrated with the multistep manufacturing procedures.

It is noted that one common problem among most cleaning procedures (except for the As or Sb capping technique) persists for III-V surfaces: a III-V surface does not exhibit long-range ordering after removing native oxide and carbon contaminants by wet chemistry for instance. In contrast, after removing the contaminants, the III-V surfaces are disordered and resemble an amorphous layer with many point defects, lying on the top bulk crystal planes. Figure 2 exemplifies this problem using the InP(100) surface that has been cleaned by a HCl+IPA -based etching recipe, similar to that used previously for GaAs(100).[120,121] Figure 2a shows a low-energy electron diffraction (LEED) pattern from the InP(100) surface just after the HCl+IPA cleaning in N_2 background without any direct air exposure. Indeed most of amorphous surface oxides have been removed in the etching because (1×1) LEED pattern appears, consistent with the GaAs(100) results.[120,121] However, as scanning tunneling microscopy (STM) images reveal (Figure 2), there is no detectable long range order for this surface. This is a good example where the appearance of LEED spots, typically an indication of long-range order of the near-surface region, does not necessarily provide proof of a crystalline topmost surface. In other words, (1×1) diffraction spots arise in this case from the bulk planes beneath a topmost amorphous layer. Although LEED is surely a surface sensitive characterization method, LEED is not sensitive to local defects, and thus it is often instructive to inspect the associated surface using STM as well. It is worth noting that before cleaning of a III-V surface, no LEED spot is seen because an amorphous oxidized layer is too thick at the surface to get elastic electrons out from the bulk plane. GaN-based crystals are an exception

here: (1×1) LEED can be observed from GaN surfaces without any cleaning as this surface resists extensive oxidation.[55,122]

Figure 2 exemplifies also how the vacuum heating around 350 ºC improves crystal quality of the etched InP(100) surface, and leads to the formation of a structural reconstruction. The InP(100)(2×4) reconstruction can be observed in both LEED and STM in (Figure 2). Note that InP(100) does not exhibit (4×2) at all, in contrast to GaAs(100) and InAs(100). Because the reconstructions are a clear fingerprint of the clean and long-range ordered surface for most III-V crystals, Figure 3 summarizes some common III-V reconstructions: III-As(100)(2×4),[123-133] GaAs(100)(6×6),[124,134] III-V(100)(4×2),[135-138] InP(100)(2×4),[139-141] GaSb(100)(4×3),[142-145] and InSb(111)B(3×3),[146-148] which are also relevant to the oxidized III-V surfaces considered in Section V.

When a clean and ordered III-V surface is obtained under ultrahigh vacuum (UHV) conditions, it is possible to reoxidize the surface again, but now in a controlled way. The parameter space for controlling the oxidation includes: the III-V oxidation process temperature, oxygen pressure and duration (exposure), and the starting as well as ending of the oxidation procedure (e.g. whether the oxidized III-V crystal is still post heated or not in vacuum after terminating the oxygen exposure). Depending on the III-V material, the crystal surface temperature has been typically in the range of 350-500 ºC, the oxygen pressure in the range of 5×10^{-7}-5×10^{-5} mbar, and the duration in the range of 10-30 min. The crystal temperature has been typically increased and stabilized before opening an oxygen leak valve for controlled exposures. The parameters are described in more detail for each III-V surface in Section V and Table II. It is also instructive to provide some comparison to the controlled oxidation of the Si surface.[91,93,149,150] The crystal nature of the SiO_2 interface layer has been obtained in particular by means of the high temperature oxidation around 900 ºC in atmospheric pressures. However, as noted previously, the III-V crystals start to decompose at such high temperatures, depending on the crystal

environment during the heating.[97-99] The wide-bandgap GaN and AlGaN are again an exception to such thermal decomposition because they tolerate similar temperatures to those used for silicon due to the relatively large bond scission energies of the nitrides. The high-quality silicon oxidation occurs near the temperatures at which SiO_2 starts to decompose, as well as significant oxygen diffusion through the SiO_x and into the underlying Si. In contrast to atmospheric oxidation pressures for Si, the formation of III-V crystalline oxides (Section V) has been observed by lowering the oxidation pressure (flux) using ultrahigh-vacuum technology. This pressure difference appears to result in reaction kinetics that compensate the requirement of the lower oxidation temperatures for III-V´s.[151] Moreover, there is an interesting consistency between the findings of crystalline tridymite SiO_2 interface[91] and III-V crystalline oxidation. Namely, and as Ourmazd *et al.* explained,[91] the key for their observation of crystalline SiO_2 formation was the preparation of a very smooth and highly crystalline starting Si surface by means of a sophisticated silicon molecular-beam-epitaxy (MBE) technique. The resulting grain size of the SiO_x crystals is determined by the spacing between atomic-scale steps on the clean surface before the oxidation.[91] Although MBE has not been always available in the III-V crystalline oxidation studies, a special focus by the research community has been put on the preparation of well-defined starting surfaces for the subsequent oxidation studies.[24-34,46-67]

Figure 4 presents a schematic approach to prepare crystalline oxidized III-V surfaces. The cleaning of crystal surfaces can be done in several ways to remove the surface oxides and contaminants. The optimized environment of a vacuum chamber allows one to enhance the crystalline nature of the cleaned surface, which is otherwise a very challenging task because a semiconductor surface strongly reacts with environment. In UHV surface-science apparatus, the heating of the surface is the established method to make semiconductor surfaces well ordered. Table II summarizes key surface-preparation parameters under such conditions.

After the subsequent controlled oxidation, the crystal can be transferred to a next processing step such as the growth of an overlying insulator film. Foe example, the crystalline oxidation of InAs were initiated using small samples (about 6 mm × 12 mm pieces of a wafer),[50] but later the approach was also transferred on a wafer-scale.[54] These oxidized wafers were successfully transferred via air to an atomic layer deposition (ALD) reactor for subsequent (high-k) dielectric deposition, but the use of clustered-chamber vacuum technology also allows designing a less reactive environment for the sample transfer and deposition, in principle.[152] This is a relevant issue because it has been found that properties of the crystalline oxidized InAs change during air exposure,[53] as discussed more in Section V.

IV. INTERFACE MEASUREMENTS METHODS

Characterization of the buried interfaces is challenging in general because a critical interface layer typically lies below the topmost film and is narrow as well as disordered. Thus, it is often necessary to combine the benefits of several complementary experimental and computational methods to get good understanding of the interface properties and effects. The widely used measurements for the interface characterization include the x-ray photoelectron spectroscopy (XPS), capacitance-voltage (C-V) analysis of MOS capacitors, high resolution transmission electron microscopy (TEM), and photoluminescence (PL). Each of these techniques has their own strengths and weaknesses, which we attempt to summarize in this section. Furthermore, in the characterization of the monolayer crystalline oxidized III-V surfaces in Section V, the traditional surface-science methods: LEED, reflection high energy electron diffraction (RHEED) as well as STM and scanning-tunneling spectroscopy (STS), reviewed elsewhere,[153-155] can be used to probe initial stages of the interface formation and semiconductor oxidation. As noted previously, the benefit of STM/STS is that the method allows to probe

the local atomic and electronic structures around defects at surfaces, while electron diffraction methods enable long range order studies.

Here it is also useful to consider the interface dimensions such as one point defect per unit (interface) area which can cause the uniform defect densities 1×10^{10} cm^{-2} and 1×10^{12} cm^{-2} for instance. Namely, such a low density as one point defect per the 100 nm × 100 nm interface area can already cause a midgap level density of 1×10^{10} $eV^{-1}cm^{-2}$, while one point defect per 10 nm × 10 nm can lead to the defect-level density of 1×10^{12} $eV^{-1}cm^{-2}$. The comparison to the semiconductor host-atom density of $\sim10^{14}$ cm^{-2} sets a rather stringent requirement for a sensitivity of any physical interface characterization method. Indeed, the sensitivity of electrical characterization due to carrier scattering is often employed for such evaluations in combination with process variations. This approach also has limits though as some interpretation ambiguity can manifest itself from the device model, experimental design, and characterization method.[156]

After the research of Siegbahn et al.,[157,158] XPS (also known at the time as Electron Spectroscopy for Chemical Analysis – ESCA) has become one of the most used techniques in materials science and technology.[153,155,159,160] One clear strength of XPS is in its elemental sensitivity which enables the determination of material chemical composition in non-destructive manner down to perhaps 0.5-1 atomic % ($\sim10^{12}$ to 10^{13} atoms/cm^2) for most elements, and is better for heavy than light elements.[161]

However, such XPS result reflects the chemical composition of a near-surface region rather than the bulk composition because a mean free path (λ) for the elastic photoelectrons (without any energy losses) inside a solid is rather short: typically 0.5 nm – 3 nm depending on the photoelectron kinetic energy. This results in an “information depth" of $\sim3\lambda$.[153,159,162] Although the electron mean free path is a universal property among solids, some material-dependent variation has been also found for the mean free path generally due to the material density. For example, the path can be larger for oxides than the

corresponding pure element.[163,164] Even if the XPS probing depth is low, it provides an opportunity to obtain a signal from the buried interface region through a thin, outermost film. Furthermore, the use of hard x-ray photoelectron spectroscopy (HAXPES) with high-resolution, tunable energy synchrotron sources has been utilized more and more to investigate deep interfaces beneath an insulator or metal film thicker than 10 nm.[162,165] Such synchrotron XPS (also called Photoemission Spectroscopy – PES) enables one to probe practical type interfaces because in many applications a crucial interface lies deep below a cap. However, when trying to connect the core-level results to the defect-level densities, it is useful to remember that the low atomic concentrations ($<1\times10^{11}$ cm^{-2}) are very challenging to measure by XPS or HAXPES, and require an extremely good signal/noise ratio. Another limitation is the associated analytical spot size, which can range from microns to millimeters depending on the configuration.

The widely used benefit of XPS is its capability to provide information about the atomic bonding structure with neighboring atoms at interfaces via the core-level shift analyses. The valence-electron distribution around the studied atoms is sensitive to the bonding environment of the atoms. Furthermore, the binding energies of core-level electrons depend on the valence-electron distribution (so-called on-site charge) in a simplified initial-state picture: higher electron density around the atom smaller core-level binding energy. However, there are also two other physical factors which can change the core-level binding energy: namely changes in the Coulombic electrostatic potential induced by other atoms (e.g. nearest and second-nearest neighboring atoms) in the material and changes in the final-state screening effect of remaining electrons (i.e. relaxation response of other electrons to the created core hole).[166-168] These different contributions can even cancel each other, complicating the analysis of the measured core-level shift. Thus, it is very instructive to compare the measured and calculated core-level shifts (simulated with both the ground-state structures and the final relaxed structures with the core hole) to understand possible atomic structures behind the measured shifts.[167,168-172]

Concerning the oxidation of semiconductors, it is widely accepted that the core-level binding energy of Si and group-V atoms increases systematically with increasing the number of direct oxygen bonds (e.g. Refs. 168-172), but for group-III elements the situation might be much more complex,[172] as discussed below in Section V. Figure 5a exemplifies the oxidation-induced InGaAs core-level shifts measured by HAXPES from SiN_x/InGaAs, which can be seen as a shoulder or tail of the III-V substrate bulk peak that is commonly used as the reference energy (i.e. 0 eV) for shifts. It can be seen that the oxidation-induced shifts for Ga and In are not so large, around 1 eV or smaller, as compared to the oxidation-induced shifts of As which can extend up to 5 eV. The emission components with only small shifts (e.g. for Ga and In) typically overlap with each other, hindering a detailed determination of the substrate peak position. Tuning the surface sensitivity of XPS spectra by changing the photoelectron-emission angle or kinetic energy is helpful to solve the bulk peak position carefully, for understanding the interface-related spectral features in detail. Still, it is important to note that different atomic structures at the interfaces can cause similar core-level shifts, and surely, complementary characterizations need to be combined toward good understanding of the atomic structures of interfaces. Even the detailed atomic structure of the SiO_2/Si interface causing the commonly observed Si core-level shifts: i.e. Si^{+1} - Si^{+3} oxidation-state like components in addition to Si^{+4} of SiO_2 appears to remain an open issue.[168-170,173-176]

High resolution transmission electron microscopy (HR-TEM) has provided indispensable information about atomic structures of various materials, particularly when coupled with various imaging and spectroscopic techniques.[177-183] The preparation of the specimen has been revolutionized by the use of focused ion-beam techniques. However, work on III-V materials can require considerable care, and even require the traditional methods of polishing. TEM is often utilized to image insulator/III-V interfaces on the atomic scale (e.g. Refs. 45,181-183). One example is shown in Figure 5b, including large-scale and zoomed-in atomic-scale TEM images for the ZrO_2/InAs interface with thermal oxidation.[45] Such images of atomic columns through the speciemen thickness give important information

for example about a degree of interface crystallization, size of possible crystalline domains, and unit-cell dimensions. Indeed, Figure 5b reveals at least local crystallization of a thermally oxidized InAs layer,[45] which interestingly resembles the crystalline tridymite SiO_2/Si case.[91] Also, possible post-annealing induced structural changes inside an insulator film (e.g. formation of crystalline grains) can be observed by TEM. The atomic resolution images provide nanoscale information on the material, and it is worthy to recall what defect densities might be relevant in this case: one defect per 10 nm × 10 nm area corresponsing to 1×10^{12} defects/cm^2. In regard to the oxidation studies of III-V interfaces, the imaging of individual oxygen atoms is not straightforward with any microscopy technique due to the associated atomic electron density (e.g. low Z).

Photoluminescence (PL) is a very common measurement in the research and development of III-V optoelectronics materials, where the direct band gap enables an efficient enough light emission. Traditionally PL has been used to study the electronic structures of III-V bulk crystals and heterostructures around the energy band gap. However, the potential of PL for the interface characterization has been also realized for some time.[184-190] The basic argument for the surface or interface sensitivity of PL arises from a long diffusion length of the photogenerated carriers (i.e. electrons in the conduction band and holes in the valence band), which can be hundreds of nanometers depending on the majority and minority carrier lifetimes. Therefore, although the major absorption of the excitation photons occurs in the bulk crystal area, the photogenerated carriers can reach the defect-rich interfaces via the long carrier diffusion lengths. That is; the interfaces cause non-radiative recombination of the carriers via defect levels and decrease the PL intensity. The qualitative comparison of defect-level densities is the common result of the PL characterization of different interfaces. Figure 5c presents an example for the PL characterization for Ga_2O_3/GaAs interfaces together with the high-quality heteroepitaxial interface.[187] It is seen that the PL intensity from Ga_2O_3/GaAs is almost the same as for

the very strict reference of epitaxial AlGaAs/GaAs. The room-temperature PL measurement is relatively quick and of course non-destructive. One challenge arises from possible overlapping band-bending effects on the PL intensity comparsion;[188,189] for example, the upward band bending toward the interface repels the conduction-band electrons that have typically longer diffusion lengths than holes. This decreases the non-radiative recombination via interface defects, and a harmful effect of the interface defect levels on PL intensities. The fixed charges inside an insulator film or/and slow border traps[191] can form a static charge and internal electric field in relation to the time scale of PL intensity measurement. It is also useful to realize that the reflection of excitation light might vary between different samples with different refractive indexes, affecting the PL intensity.

Last, but not least, capacitance-voltage (C-V) characterization of metal-oxide-semiconductor capacitors (MOSCAP) is popular. C-V characterization serves as a well-known electrical probe of the insulator-semiconductor interfaces, as compared to XPS, TEM, or PL. Thus the C-V characterization has been widely utilized in the research and development of III-V passivation (e.g. Refs. 192-202). Indeed, the performance of MOSCAPs is very sensitive to the properties of an insulator/semiconductor interface. The quantitative analysis of C-V data to determine the defect-level density is described in detail in many previous works (e.g. Refs. 9,192,194), and here we only qualitatively present specific features of C-V curves related to the interface defects. In Ref. 194 the challenges and guidelines for the analysis of III-V MOSCAP have been described in instructive way. As Engel-Herbert et al.[194] write, the C-V analysis concepts have been largely developed for silicon MOSCAP, but many properties of III-V are naturally different from silicon ones. For example, the carrier lifetime in III-V's can be several orders shorter than in Si because of the direct band gap.

Figure 5d shows the C-V curve examples measured from Al_2O_3/n-InGaAs MOSCAP with and without the forming-gas-anneal (FGA) hydrogen passivation.[202] A measurement frequency for the difference curves increases to downward. The observed dispersion of accumulation capacitance as a

function of the frequency at the positive voltage side has been found to arise from border traps for carefully fabricated capacitors,[23,203] which however lie very close to interface (distance less than 1 nm).[196-199] Furthermore, the frequency dispersion of the depletion region (around 0 V), appearing as a hump of the capacitance increase, can be attributed due to the interface defects. It can be seen that FGA decreases the density of these defects (Figure 5d). The capacitance increase in the hump area resembles the early inversion increase, but in the true inversion operation (i.e. proper Fermi-level movement over the band gap without a significant pinning) the capacitance should increase and saturate clearly in the inversion region at the negative voltage side (for n-type semiconductors). Another qualitative comparison of C-V curves can be done for the curves measured at high enough frequency to avoid any response of the fast interface states. In such conditions, the slope of the depletion region capacitance is still affected by the interface levels because the DC voltage is changed so slowly. Thus, the reduced slope (or more stretched out capacitance step) in the depletion region, measured with high frequencies, corresponds to a higher density of defect levels. Recent modeling and C-V characterization work (using an Al_2O_3/InGaAs capacitor structure) has also demonstrated the role of inelastic tunneling as a means to distinguish interface state and border trap contributions to the C-V (and conductance-voltage) response.[204] Similar studies using a crystalline oxide interface would be of interest.

V. CHEMICAL AND PHYSICAL PROPERTIES OF CRYSTALLINE OXIDIZED SURFACES

A. In-V surfaces

a. InAs surfaces

The monolayer crystalline oxidation of InAs(100) surfaces has been investigated extensively.[50,52-54,56,58,62,66] Before those studies, long-range ordered In_2O molecule structures have been deposited and investigated on InAs(100), providing an interesting counterpart system for comparison.[48,49] The response of InAs(100) surfaces is that their lattice cell changes upon exposure to the crystalline

oxidation process. This leads to oxidation-induced surface-reconstruction periodicities that are distinct from those for the clean InAs(100) surface which exhibits the c(4×4), (2×4), and (4×2) reconstructions after the cleaning with a decreasing As/In ratio at the surface (Section III). The oxidation has been so far been found to induce c(4×2) and (3×1) reconstructions at InAs(100). Thus, LEED or RHEED can be quickly used to monitor and conclude the incorporation of oxygen, due to clear changes in LEED and RHEED patterns. This is indeed a benefit because typical laboratory XPS is not sufficiently sensitive to small changes in the incorporated oxygen amount ($<10^{13}$ cm^{-2}). On the other hand, a small XPS oxygen signal (i.e. O1s) can easily appear on a cleaned surface before the controlled oxidation due to for instance incomplete cleaning or degassing surfaces present in vacuum tools. However, with careful attention to the analytical spot size and geometry, monochromatic XPS provides a crucial piece of the evidence for the crystalline oxidation because the O1s peak should increase in intensity with the oxygen incorporation and because chemical bonding environment of group-III and -V elements changes, causing detectable changes in their core-level spectra.

The c(4×2)-O and (3×1)-O layers are two different crystalline oxidized surfaces of InAs(100), of which (3×1)-O includes more oxygen (about two times) than c(4×2)-O according to the O1s XPS measurements.[50,58,59] The clean InAs(100) surface has been reported to be obtained by either the Ar-ion sputtering+vacuum heating[50,58,59] or by the As-decapping technique.[53,54,56,62] In Figure 6, LEED shows the (4×2) reconstruction for the sputter-cleaned InAs(100) after the vacuum heating around 400 ºC. Figure 7 shows the corresponding STM image, which reveals a smooth two-dimensional step-terrace structure for a well-cleaned InAs(100). It is noted that the As-decapping method allows also the preparation of a more As-rich (2×4) starting surface, as compared to the (4×2) surface (Figure 3).[54]

Figures 6 and 7 also show LEED patterns and associated STM images for the oxidized InAs(100) surface.[50,66] The two-dimensional step-terrace structure remains in large-scale STM images

for the c(4×2)-O and (3×1)-O surfaces after the controlled oxidations. This indicates the crystalline nature for these surfaces and is consistent with the clear LEED patterns. This is further supported by the comparison to LEED and STM from an amorphous surface oxides of InAs(100) in Figures 6 and 7. The c(4×2)-O surface is obtained when the oxidation temperature has been higher than that used for the (3×1)-O reconstruction, or when the oxidation time (i.e. oxidation dose) has been smaller than that used for the (3×1)-O. It is essential to note here that these observations have been done with the same experimental setup,[50,58,59] because the comparison of the temperatures, in particular, between different experimental surface analysis systems is generally a complicated issue and can require extensive cross-calibrations. Furthermore, the oxidation temperature, pressure, and time affect each other in the establishment of the "window" of reproducible parameters required to obtain (3×1)-O and c(4×2)-O reconstruction signatures.

Table II presents details for the surface cleaning and oxidation, and the parameter ranges where both the (3×1)-O and c(4×2)-O surfaces have been observed can be summarized as follows: 300-400 °C for the oxidation temperature, 1-10×10^{-6} mbar for oxygen pressure, and 5-30 min for the oxidation duration. The (3×1)-O surface has been found to contain a double the amount of oxygen atoms, as compared to the c(4×2)-O surface.[50,58,59] This difference might also be seen in the STM image (Figure 7e) where both the c(4×2)-O and (3×1)-O phases coexist. Namely, the c(4×2)-O areas look more flat (or two dimensional) than the (3×1)-O areas do; the (3×1)-O areas are more corrugated on atomic scale, which can be understood as follows. Because the (3×1)-O layer can be expected to be a thicker oxide than the c(4×2)-O layer, the structural strain is expected to increase for the (3×1)-O layer. These crystalline oxides on the top of InAs resemble a thin heteroepitaxial system where the strain might be relieved through the formation of a corrugated (3×1)-O structure.

In Figure 7e, an additional structural feature is detected, distinct from the (3×1)-O and c(4×2)-O areas. Namely, local white rows (marked with AsO_x) appear in particular on the (3×1)-O areas.

That phase has been associated with As oxides because XPS of (3×1)-O shows a clear As_2O_3-type high-oxidation state feature in the As3d core-level spectra,[53,54,58,62] as exemplified in Figure 8. Furthermore, this As_2O_3-type emission arises from the topmost surface according the synchrotron-radiation XPS (Figure 8),[58] and it also disappears immediately after starting the atomic layer deposition.[53,62] These results indicate that the As_2O_3-type bonding structure (i.e. As^{3+} atoms) does not belong to the basic unit cell of (3×1)-O but rather lies on the top of it. It has been suggested that the local As_2O_3-type rows form when oxygen atoms become incorporated into InAs, removing some of the As host atoms which then diffuse toward the surface and form there bonds with oxygen.[66] That is, the In-O bonding is energetically more favored than As-O in InAs.

Indeed several oxidation-induced changes (i.e. core-level shifts) have been found in the In core-level spectra for both the (3×1)-O surface[53,54,58,62] and c(4×2)-O surface.[59] Moreover, in the O1s spectrum of (3×1)-O, it has been observed both the In-O and As-O emission components,[58] while the O1s spectrum of c(4×2)-O has less components and energy variation.[59] Surprisingly, the In core-level spectra of both the (3×1)-O and c(4×2)-O surfaces have the oxidation-induced components (shifts) at smaller binding-energy side, as compared to the InAs bulk binding energy.[58,59] In early studies, these shifts were associated, at least in part, with In dangling bonds,[57-59] but subsequent studies of the buried interfaces of Al_2O_3/InAs[66] and HfO_2/InP[172] have revealed that the oxidation can cause negative shifts in particular for indium. The As oxides resemble more the Si oxidation case, where the Si core-level binding energy systematically increases with increasing the number of oxygen bonds up the +4 oxidation state, but a great care should be put on the analysis of the group-III shifts induced by oxidation.[172] An interesting and surprising result, which the calculated core-level shifts reveal, is that the In core-level shift does not directly depend on the amount of oxygen bonds or nearest oxygen neighbors, in contrast to the common reference system of the silicon oxidation. However, this result is consistent with the

comparison of the In core-level shifts between the InAs(100)(3×1)-O and InAs(100)c(4×2)-O surfaces; namely, the most positive In shift for (3×1)-O is about 0.5 eV while the most positive In shift for c(4×2)-O, having lower oxygen amount, is about 1 eV.[58,59]

Initial atomic models[50] were proposed on the c(4×2)-O and (3×1)-O surfaces on the basis of the ab initio calculations and STM-image comparison, as presented in Figure 9. Subsequent PES measurements have however shown that these surfaces include more oxygen than the initial models predict. By comparing the spectral results of (3×1)-O to the corresponding oxidized structures of InSb (see below), it can be concluded that the (3×1)-O surface includes more than two monolayers (MLs) of oxygen (1 ML means the atomic density of InAs plane).[57-59] The higher amount of incorporated oxygen atoms is reasonable for several reasons. First, it has been found that the (3×1)-O surface is relatively more stable in air exposure than the clean InAs because some (3×1) LEED spots appear even after the air exposure.[50] Also, a (3×1) RHEED pattern can be observed after air exposure of the InAs(100)(3×1)-O, as shown in Figure 7f. Furthermore, even if (3×1) LEED has been found to disappear just after starting the atomic-layer deposition (ALD) of Al_2O_3 or HfO_2 insulator film,[53,62] an improvement has been found in the electrical properties of the interfaces,[54,62] as described below. This suggests again that the (3×1)-O layer is persistent and thick enough to provide a suitable barrier to harsh ALD growth conditions of the overlayer.

Valence-band photoelectron spectra of the c(4×2)-O and (3×1)-O surfaces show that the gap area below the Fermi level is free of the electron levels within the resolution of the photoelectron spectroscopy.[50] For comparison, the spectrum from an air-exposed InAs(100) showed a clear electron emission from the levels around the gap area up to the Fermi-level (i.e. metallic type surface)[50] and is consistent with the harmful effect of the normal (disordered) III-V oxides reported many times. In contrast, the valence spectra of c(4×2)-O and (3×1)-O indicate that the band gap increases for these

surfaces, as compared to InAs. Therefore, the above results predict that the crystalline oxidized InAs surfaces improve electrical properties of the InAs materials.

It is interesting to compare the crystalline oxidized InAs results to the similar system where In_2O molecules are deposited on the well-defined InAs(100)(4×2) surface.[48] Figure 10 presents STM images for this In_2O/InAs system which becomes ordered after post annealing at 380 ºC. A row structure with the distance of 13 Å or 8.5 Å can be seen in the STM images, indicating the 3× or 2× periodicities in STM images.[48] This is consistent with the periodicities of c(4×2)-O and (3×1)-O discussed previously. The row structure of In_2O/InAs (Figure 10) resembles more the structure of (3×1)-O than c(4×2)-O according to STM images (Figures 7 and 9). However, as also discussed previously, the oxidized (3×1)-O surface can contain 2 ML or more oxygen. On the other hand, the STS measurements and calculated electronic structures[48] indicate that the band gap free of defect levels is possible using the In_2O deposition, which also agrees with the valence-band photoemission of the c(4×2)-O and (3×1)-O surfaces.[50]

The electrical test of the crystalline oxide approach was reported in 2013 by a large international consortium for the crystalline oxidized III-V surfaces using the InAs(100)(3×1)-O surface.[54,205] Their HfO_2/InAs capacitor measurements revealed a significant decrease (about 40 times) in the defect-level density (2.2×10^{11} cm^{-2} eV^{-1})[54] and also a very promising mobility values for ZrO_2/n-InAs MOSFET[205] due to incorporating the (3×1)-O layer into the gate interface. The reference sample was a traditional HCl-based treated InAs(100) surface before the ALD-HfO_2 growth. Alternative studies by this group also explored ALD pre-treatments of the InAs surface in combination with Al_2O_3 and HfO_2 ALD, where extracted D_{it} values were ~30× higher, and no detection of an ordered interface was reported.[206] The capacitance-voltage curves of the HfO_2/InAs capacitors[54] are presented in Figure 11, and similar C-V curves have been found also for the ZrO_2/(3×1)-O/InAs interfaces.[205] The latter interface

revealed also high performance mobility of 6000-7000 cm^2/Vs for surface channel NMOSFET.[205] These results indeed provided good motivation for investigating the controlled oxidation of III-V´s, and were later supported by other findings for the (3×1)-O.[62,66] At the same time, the work presented in Ref. 54 provided also the first wafer-scale test for the controlled oxidation using the reflection high-energy electron diffraction (RHEED) to monitor the crystalline oxidation in elegant way in situ by means of clear changes in the diffraction pattern. It is worth noting that the crystalline oxidized InAs(100)(3×1)-O wafer was exposed to the air prior to the ALD growth,[54] which is a rather tough test of the surface oxide stability, and further supporting the above conclusion that the (3×1)-O layer includes more than two monolayers of incorporated oxygen.

In further studies, it was also observed that a leakage current through the ALD-Al_2O_3/InAs(100) structure decreased when the crystalline c(4×2)-O or (3×1)-O layers were incorporated at the interface.[66] This result is consistent with the decrease in interface defect density.[75] In the leakage current comparison,[66] the crystalline oxidation decreased the leakage current by factor of 10 approximately (at -2 V), when compared to the reference sample which was cleaned by a similar Ar-ion sputtering+vacuum heating before ALD-Al_2O_3. When the reference sample contained a native oxide plus ALD-Al_2O_3, then the crystalline oxidation decreased the leakage current by factor of about 5 (at – 2V). The most-likely reason for this difference between the sputtered and native-oxide samples is that the Ar-ion sputtering, used in surface preparation, degrades the crystal structure of InAs into some depth toward the bulk, and the subsequent heating in vacuum cannot fully recover the crystal quality, as compared to the bulk in the native oxide sample.

b. InSb surfaces

Clean InSb(100) surface reconstructions are similar to InAs(100) when the Sb amount decreases on the surface; namely both InSb(100) and InAs(100) exhibit the In-induced (4×2) structure (Figure 3) which is also called c(8×2) because a shift of the ×4 rows in turn along the row direction causes sometimes c(8×2) LEED. However, the atomic structure is basically same for c(8×2) and (4×2), including the same ×4 rows. InSb(100) has a similar (3×1)-O crystalline oxidized structure to that for InAs. The photoelectron data indicates that (3×1)-O is largely same for InSb and InAs.[58] However the oxidation results in a (1×2)-O reconstruction on InSb(100), instead of c(4×2)-O as found for InAs. Therefore we focus here on (1×2)-O, also because it has been studied more.[57] Subsequently, we also describe a specific III-V(111) example in this review: crystalline oxidized InSb(111) which is more challenging because its surface lattice does not change obviously due to oxidation, in contrast to the (1×2)-O and (3×1)-O periodicities which do not appear on the clean InSb(100).

Figure 12 summarizes how the oxidation parameters for the crystalline InSb(100)(1×2)-O depend on the crystal temperature, oxygen pressure and duration. The atomic models were studied by means of ab initio calculations as a function of the oxygen amount. It is clear that many different models can be constructed, and as more oxygen was incorporated, the stability of the structure formed is enhanced because oxidation decreases the total energy. Figure 13 presents such models which explain reasonably the scanning tunneling microscopy/spectroscopy and photoelectron results measurements of the InSb(100)(1×2)-O structure to date.. The models presented in Figure 13 as a function of oxygen amount in the range of 0.5-2.0 monolayers exemplify an interesting change of the conductivity when the oxygen amount changes. Namely, the 0.5 ML model is metallic while with the 1.0 – 2.0 ML oxidation, the band structure becomes more insulating. The band structure examples are shown in Figure 14. The metallic nature of the 0.5 ML model (Figures 13a and 14a) arises from the dimer-atoms 2 and 3. Interestingly, the In dangling bonds become filled (saturated) when the oxygen amount is increased,

which is in contrast to the common prediction that the group-III dangling-bond levels remain empty and lie in the conduction band.[57] The variation in the conductivity observed with oxygen amount supports the goal to control the oxidation state of III-V surfaces on atomic scale at the device interfaces.

Crystalline oxidized InSb(111) provides an interesting, different example in comparison to the common III-V(100) faces considered in this review. The results obtained for the oxidized InSb(111)B(3×3)[65] provide also a relevant information for technology where usually several different crystal plane orientations are exposed to oxygen-containing environment during the device component processing. On the basis of the oxidation results of InSb(100), it can be hypothesized that the crystalline oxidation is possible for the other crystal planes too. However, as the results of Ref. 65 show, there are some important differences, as compared to the III-V(100) oxidation. First of all, the oxidation of InSb(111)B does not produce a new surface lattice cell or periodicity, in addition to the (3×3) and (2×2) reconstructions formed at the clean surface (Figure 15) as a function of Sb/In surface ratio. That makes the studies of InSb(111) oxidation challenging because a simple and quick monitoring of the oxidation by LEED (or RHEED) is apparently not possible in this case. It is worth noting that even the combination of LEED and XPS does not provide conclusive evidence for the crystalline oxidation phase here because the possibility that the oxidation-induced changes in XPS arise from local defects between the (2×2) or (3×3) areas still remains. However, compelling evidence for the crystalline oxidation of InSb(111)B is gained by combining atomic resolution STM images and STS curves with LEED and XPS.[65]

When the clean InSb(111)B(3×3) surface was oxidized to result in a crystalline layer, its surface lattice remained (3×3) or changed to (2×2) depending on the oxidation temperature. The (3×3) lattice remained when the temperature was higher, around 400 ºC, while the cell transformed to (2×2) due to the oxidation when the temperature was lower than 400 ºC, around 350 ºC. This result is consistent with the knowledge that the (2×2) structure is usually seen in Sb-rich surface conditions, which

furthermore can remain if the temperature is low enough. The result suggests that some Sb atoms are forced out to the surface because of oxygen incorporation into InSb, consistent with the initial stages of oxidation of InSb(100) in Figure 13a. The STM image in Figure 15 reveals that epitaxial-type islands are formed at the oxidized InSb(111)B(2×2)-O surface. Also XPS data (Figure 15) clearly shows the oxidation. To recapitulate, the results for InSb(111)-B suggest that the crystalline oxidation is a general property among the different crystal planes, which is relevant to the practical processing of III-V devices and future nanodevices.

c. InP surfaces

The crystalline-oxidized InP surface has received less attention than the other crystalline oxidized III-V surfaces. The InP(100)(2×3)-O surface has been found at relatively high temperatures 450-550 ^{o}C when the oxygen pressure is 5-10×10^{-7} mbar. STM, LEED, and XPS results are summarized in Figure 16 for InP(100)(2×3)-O. It is interesting that that the calculated core-level shifts for the HfO_2/InP(100) interface with a semicoherent structure (i.e. O10 model)[172] agree well with the shifts estimated by means of XPS measurements for InP(100)(2×3)-O (Figure 16). Thus this structure provides a good starting point for developing the atomic model InP(100)(2×3)-O.

In regard to establishing the structure, it is relevant that the semicoherent (O10 model) interface models for HfO_2/InP(100) causes a significant positive (i.e. high binding energy) shift for P atoms between +3 eV and +5 eV.[172] Therefore, the suggested surface nature of the corresponding high-binding energy shift of As atoms on the InAs(100)(3×1)-O comes into question; viz. whether this As shift still arises from the deeper, inherent unit-cell structure of the (3×1)-O layer. On the other hand, the P-O bonding is energetically more favored than As-O or Sb-O bond formation.[9,69,70] Furthermore P_2O_5

is more stable than In_2O_3 while As_2O_5 or As_2O_3 is less stable than In_2O_3. These details remain to be studied further at this time.

B. Ga-V surfaces

a. GaAs surfaces

The crystalline oxidation parameters, similar to those found for the InAs and InSb systems, have not been reported on the pure GaAs surfaces so far. However, the growth or deposition of Ga_2O molecules on GaAs(100) has led to an ordered structure.[29,31] Figures 17(a) and 17(b) show the initial bonding sites for Ga_2O on GaAs(100)(2×4). The MBE method combined with the As capping was used to prepare the well-defined As-terminated GaAs(100)(2×4) surface for Ga_2O depositions. RHEED showed a clear 2× periodicity for the Ga_2O covered surface.[29] Furthermore, the STS curves in Figures 17(c) and 17(d) suggest an unpinned surface free of the gap levels. Moreover, the recent computational results[113,114] indicate that an ordered Ga_2O_3 type interface layer has the potential to form. This prediction is consistent with the experiments showing interfacial crystallization at MBE-grown Ga_2O_3/GaAs,[182] in addition to the Ga_2O_3/Gd_2O_3/GaAs system.[24-28,115-118] Incorporating Gd atoms into the interface is expected to make the epitaxial film growth easier because Gd atom is much larger than Ga, providing better lattice match between the oxide and GaAs. Consistently, the results from the GaAs oxidation experiments have shown that even small amount of another group-III element of indium, which is also larger atom than Ga, at the GaAs(100) surface induces the long-range ordering of intentionally oxidized surfaces, as presented below. That is also consistent with the previous calculations showing a difference in structural and electronic properties between GaAs and InGaAs, and a benefit for including indium.[207]

Initial crystalline oxidation tests in Ref. 48 were performed on GaAs(100) using tin (Sn) and indium adsorption and desorption experiments. Oxidation was studied through examination of the

reaction of tin (Sn) on removing surface oxides from GaAs in a catalytic manner, and also oxidation of Sn-covered GaAs surfaces.[208,209] Similar catalytic effects for indium on removing GaAs oxides were studied, and weak ×3 streaks were observed when In-terminated GaAs(100)(4×2)-In surface was oxidized. This led to the oxidation induced (4×3)-InO structure which showed the same sharp 4× spots as for the starting GaAs(100)(4×2)-In combined with ×3 streaks (Figure 18), in contrast to ×2 streaks (e.g. Figure 6b).

Figure 18 shows STM images for the GaAs(100)(4×3)-InO, which reveals the formation of additional building blocks between the initial 4× rows. The initial atomic model for (4×3)-InO is in good agreement with the topmost structure (Figure 18) according to the comparison of the simulated and measured STM images. Further studies has reported also oxidation-induced c(4×2)-InO and (1×1)-InO surface reconstructions on GaAs(100).[64] The In-containing GaAs(100) surfaces are challenging because, in addition to the large oxidation parameters space, the amount of indium can vary signifcantly for GaAs(100)(4×2)-In reconstructions.[210] The results indicate that (1×1)-InO has less indium than the two other reconstructions.[64] Initially, the (1×1) LEED pattern suggests just an amorphous topmost surface, as discussed in Section III, but STM images for this surface show a long-range ordering, as presented in Figure 19. Also the (1×1) LEED pattern is exceptionally sharp for this surface, supporting the ordering for the surface. Thus, further studies of GaAs(100)(1×1)-InO with the lowest indium amount might provide crucial information to find proper crystalline oxidation parameters for pure GaAs(100). Related to that, it would also be useful to investigate further how the ratio of As/Ga amounts on the GaAs surface affects the oxidation result. Namely, the above described result that Ga_2O-induced 2× periodicity was observed particularly on the As-terminated GaAs(100)(2×4) starting surface, in contrast to Ga-terminated GaAs(100)(4×2)[29,31] indicates a role of controlling the As/Ga surface ratio (Figure 3).

The crystalline oxidation of the In-terminated GaAs(100)(4×2) surfaces have been often performed with lower oxygen pressures, 1-10×10^{-7} mbar, as compared to the above InAs and InSb systems. Also the oxidation temperatures have been higher for GaAs(100)(4×2)-In; in the range of 400-550 ºC. As mentioned already, the oxidation of GaAs(100)(4×2)-In is challenging also because the final result depends on the amount ratio of As/group-III at the starting surface. If indium is deposited on the As-terminated (or As rich) GaAs substrate, an ultrathin InAs layer with the (4×2) reconstruction is most likely formed. However, this InAs can readily re-evaporated from the substrate at the elevated oxidation temperatures.

The third structure on GaAs(100), namely c(4×2)-InO is probably linked to the InAs-type topmost structure because its formation is sensitive to finding a correct combination of the experimental parameters. And also because the pure InAs(100) has the oxidized c(4×2)-O phase. Properties of the GaAs(100)c(4×2)-InO surface have been summarized in Figure 20. First, this oxidized structure has been incorporated into the Al_2O_3/GaAs interface, where atomic layer deposition (ALD) was used to grow Al_2O_3 in situ without breaking vacuum conditions. The photoluminescence (PL) intensity comparison in Figure 20 indicates that the interface defect density decreases due to c(4×2)-InO because the PL intensity increases; that is non-radiative recombination decreases at the interface. The PL-intensity method is based on long diffusion lengths (even hundreds of nanometers) of carriers in high-quality III-V crystals, which means that the photoexcited carriers in the bulk can diffuse and reach the surface and interface regions. Therefore, the surface region of III-V crystals affects the PL intensity. However, when analyzing PL-intensity results one needs to realize also other possible factors behind PL intensity changes, such as the band bending at III-V interfaces and changes in the light reflection (Section IV). If the bands bend upward at the interface, electrons experience a repelling internal electric field while holes feel an opposite effect. Such field-effect passivation can also increase the PL intensity.[187,188]

Figure 20 presents also XPS results from the Al_2O_3/GaAs interfaces to understand if the interfaces have a different chemical structure, which can be linked to the PL improvement. Indeed XPS reveals a difference: the Al_2O_3/GaAs interface without c(4×2)-InO has higher oxidation state for part of Ga atoms (i.e. GaO_y component). This emission component is missing or is smaller when the c(4×2)-InO structure was used. The GaO_y component with a shift of around +1 eV has been often associated with Ga_2O_3 type (Ga^{3+}) structure.[211,212] On the other hand, the Ga_2O_3 type interface structure has been found to be useful, as discussed above.[113-118,182] The recent ab initio calculations of core-level shifts[172] can provide an explanation for the observed shifts: similar to the negative core-level (i.e. smaller binding energy) shifts for In_2O_3 phase, our calculations indicate similar negative shift also for the Ga core level in Ga_2O_3 as compared to GaAs. Thus, the atomic structure behind the +1 eV shift of GaO_y might be different from the previous Ga_2O_3 identification. Nevertheless, it can be seen in Figure 20 that at both interfaces, the bonding environment of Ga atoms is affected by the oxidation. Furthermore, the Ga3d spectra (Figure 20) show that the c(4×2)-InO interface layer decreases the oxidation-induced changes in the Ga bonding structure, which might be expected. One scenario for the defect level formation is following: Without the c(4×2)-InO layer, Ga atoms will have more direct oxygen bonding leading to Ga_2O_3 -type formation. Although the formed Ga_2O_3 phase itself does not probably cause the electron levels in the GaAs band-gap area, the Ga_2O_3 formation can lead to the presence of harmful dangling bonds,[83-85] for example, in the surrounding GaAs crystal because of broken bonds and the lattice mismatch between GaAs and Ga_2O_3.[87-90] Such concepts makes it reasonable to enable detecting oxidation-induced XPS features (e.g. tiny shoulders or tails) although the defect-level density can be on the order of 1×10^{13} $cm^{-2}eV^{-1}$ or slightly lower (Section IV).

b. InGaAs surfaces

Although the crystalline oxidation of In-terminated GaAs(100) surfaces was reported in 2011, the crystalline oxidation for a ternary InGaAs alloy was demonstrated only in 2017.[63] Indeed, a rather different combination of the oxidation parameters was found to produce the crystalline $In_{0.53}Ga_{0.47}As(100)(3\times1)$-O surface (Figure 21). Namely, higher oxygen pressure (5×10^{-5} mbar) and shorter oxidation time (5 min) at 350 °C were used as compared to the InAs oxidation. In addition, it was also introduced an interesting complementary vacuum procedure for controlling the oxidized surfaces: atomic hydrogen exposure which produced another crystalline oxidized surface, $In_{0.53}Ga_{0.47}As(100)(3\times2)$-O.[63] This was obtained by exposing an amorphous pre-oxidized surface afterward to atomic hydrogen at 350 °C with 1×10^{-6} mbar. These periodicities are consistent with the earlier results for the In_2O deposition on $In_{0.53}Ga_{0.47}As$.[47,48] Namely, the ordered In_2O structure, similar to In_2O/InAs with 2× or 3× periodicity, has been reported also on $In_{0.53}Ga_{0.47}As(100)(4\times2)$.[47,48] However, similar detailed studies of other stable $In_xGa_{1-x}As$ alloys remain to be reported.

It was also found that the formation of Ga^{3+} oxidation-state type structures (Figure 21) should be avoided in mapping the crystalline oxidation parameters for InGaAs.[63] This is a crucial instruction and consistent with the above GaAs-InO measurements. The Ga^{3+} XPS component resembles the above GaO_y emission. As discussed already, this component most likely originates from an alternative bonding environment than Ga_2O_3. The comparison to the calculated InP core-level shifts suggests that Ga^{3+} (i.e. GaO_y) can arise from $Ga(AsO_3)_3$ type structure but then clear positive shifts can be expected for As.[172] At any rate, the Ga^{3+} type XPS feature has been clearly shown to be harmful,[59,63,211] but future studies are needed to pinpoint its atomic structure, which would be helpful to engineer the oxidation parameters for GaAs crystal inrterfaces.

Using the electrical measurements of $HfO_2/In_{0.53}Ga_{0.47}As(100)$ capacitors, it was furthermore reported that the (3×1)-O and (3×2)-O layers are helpful to decrease the density of interface

defects and also the density of border trap (Figure 21). In these experiments, the reference or control sample included high-quality crystalline $In_{0.53}Ga_{0.47}As(100)(4\times2)$ surface obtained by the elegant decapping technique. Thus these results are very promising and consistent with the above electrical results for InAs and GaAs-InO materials.

c. GaSb surfaces

Pure GaSb resembles GaAs because no crystalline oxidized structure has been so far found for them by means of the oxidation of the pure GaAs and GaSb surfaces. Furthermore, small amount of indium deposited on GaSb before the oxidation changes the resulting oxides.[60] Indium deposition combined with vacuum annealing near 400 ºC provides a (4×2)-In reconstruction for GaSb(100) too. A difference is that the clean GaSb(100) surface does not exhibit a (4×2) reconstruction (while GaAs does). In contrast, clean GaSb(100) shows different types of (4×3) reconstructions with decreasing the Sb/Ga ratio (Figure 3). However, the GaSb(100)(4×2)-In surfaces can be formed as shown in Figure 22. This STM image presents also the oxidized GaSb(100)(1×3)-InO areas. The comparison between the (4×2)-In and (1×3)-O areas reveals how the structural corrugation is increased on (1×3)-O. A similar effect was above observed also for the InAs(100)(3×1)-O, supporting that a relief in the structural strain can contribute to the phase stabilization.

STS curves in Figure 22 suggest that the InO_x structure does not cause the gap levels. In contrast the oxidation of pure GaSb(100) leads to increasing of the gap emission.[60] Figure 23 shows defective clusters formed on GaSb due the oxidation, and corresponding changes in the Ga and Sb core-level spectra measured by synchrotron PES (MAX-lab, Lund).[213] It can be seen how the Ga^{3+} type emission with about +1.0 eV shift as well as the Sb-Sb-Sb type emission with +0.8 eV shift start to form due the oxidation. That is consistent with the above GaAs and GaInAs results where the Ga^{3+} shift was

identified as the harmful step. On the other hand, metallic features seen in STS for the oxidized GaSb clusters can readily arise from extra Sb which is enriched toward the surface. The oxidation temperature is low enough that Sb atoms hardly evaporate from the surface.

C. AlGaN surfaces

One of the earliest finding for the monolayer crystalline oxidation of III-V's was reported on GaN in 2006.[46] Figure 24 summarizes characterization of the oxidized GaN(0001) surface. In general, GaN and $Al_xGa_{1-x}N$ crystals are clearly different from the other III-V´s. First, the nitrides have usually the wurtzite crystal structure with a polarity along the [0001] direction due to the ionic nature of Ga-N bond. Second, these crystals tolerate much higher heating temperatures than other III-V´s due to the interatomic bond stength. The $Al_xGa_{1-x}N$ crystals can be readily heated around 1000 ºC without crystal decomposition. Strong Ga-N bonding makes the nitrides also chemically stable, which is reflected by the observations that a (1×1) LEED pattern can be seen from the nitride surfaces without any cleaning.[55,122] This is an unusual property (Figure 25) compared to most III-V materials.

The GaN surface was oxidized at 550 ºC in an O_2 partial pressure of 1.5×10^{-5} Torr (Figure 24).[46] A specific starting surface on GaN(0001) was used: namely GaN(0001)(1×1)-Ga where a bilayer of Ga was deposited before the oxidation. Again, the MBE method was used to prepare a well-defined starting surface (see Section III). The oxidation in molecular O_2 background changed the surface structure to so-called GaN(0001)(3√3×3√3)-O-R30º (Figure 24).[46] A similar periodicity has been observed also on a clean GaN.[46] According to the experimental and computational results reported, Dong et al. suggested atomic models for the crystalline oxidized GaN in Figure 24d. They concluded that a saturation amount of the incorporated oxygen is about 2 ML in their conditions. This result is also consistent with the above finding that the In-V(100)(3×1)-O can contain 2 ML of oxygen or more (Section VA) because

it can be expected the saturation oxygen amount is even higher for InAs as compared to GaN (GaN is chemically more stable). Furthermore, these oxidation results[46] for GaN suggest that it is useful to increase the amount of Ga on GaAs to find the crystalline oxidized phases on GaAs (Section VBa).

The strong bonding associated with the nitrides presents a challenge to oxidize $Al_xGa_{1-x}N$ crystals. Thus a modified procedure was found for the crystalline oxidation of $Al_{0.25}Ga_{0.75}N$ using the plasma of oxygen containing also nitrogen.[55] The N_2 : O_2 flow ratio was 45 sccm : 0.5 sccm, and the AlGaN temperature was 550 ^oC during 10 min plasma treatment.[55] The temperature during the plasma treatment was found to affect the resulting surface structure: lowering the temperature to 300 ^oC caused an amorphous AlGaN surface, as can be seen in Figure 25. The atomic model for the crystalline oxidized AlGaN surface is shown in Figure 26, which follows that proposed for GaN.[214] It has the same bulk-plane lattice at the surface in consistent with the hexagonal (1×1) LEED. Furthermore, electrical characterization of Al_2O_3/AlGaN diodes (Figure 26) reveals that the crystalline oxidation decreases the density of interface defects. The capacitance-voltage curves in Figure 26 look different from the common C-V curves because they have two different capacitance steps. The first step of C around -10 V or -6 V is due to a 2D electron-gas at the epitaxial AlGaN/GaN interface, which has indeed higher crystal quality than the Al_2O_3/AlGaN interface. Indeed, the slope of the C step is higher around -10 V or -6 V (Section IV). The second capacitance step arises from the Al_2O_3/AlGaN interface.[215]

VI. CURRENT PASSIVATION METHODS AND DEVICE APPLICATIONS

The passivation of III-V surfaces has been investigated and developed intensively for several decades because decreasing the surface-related defect levels is relevant to develop the current and future III-V devices. This field is exceptionally broad since it has been traditionally divided in two main sectors, electronics and photonics, which have been rather separated disciplines. Furthermore, the

passivated III-V surfaces can be categorized into those at insulator/III-V and metal/III-V interfaces. Indeed excellent books have been written about the III-V oxidation and passivation together with the related device issues (e.g. Refs. 6 and 9), and it is obvious that a very comprehensive review for this complex field is beyond the scope of this review. However, we have attempted to provide a step toward the useful comparison of various III-V passivation methods by summarizing a large arsenal of the passivation instruments. Surely each method has own strengths and weaknesses and requires further perusal of the associated literature. Furthermore, it can be readily expected that combining the benefits of different passivation methods is the key to improve the performance of current III-V devices further, and also to enable the development of future III-V applications. Because of a diverse variety of III-V device components including for example HEMT, laser diode, LED, detector and solar cell, the most proper or efficient passivation method is not likely the same for all device types but rather varies among the target devices. The monolayer crystalline oxidation process reviewed here might be one tool to exploit for the III-V passivation puzzle. In this Section, we first introduce a few examples of the currently used III-V devices where the surfaces cause the performance degradation. After that, we go through different passivation methods studied and developed for III-V crystals. Finally, it is discussed how the crystalline oxidation method might be incorporated into the passivation technology as one processing step.

A. Examples of surface challenges in the currently used III-V devices

As mentioned in the introduction, the use of HEMT components has increased significantly because of various applications of monolithic microwave integrated circuit (MMIC) in wireless communication. Indeed, the annual market of MMICs is recently projected to be several billions of US dollars.[216] The III-V HEMT is one of the main components used to build up MMICs. Typically a MMIC circuit chip contains less than ten HEMT components processed on semi-insulating GaAs wafer. Also InP wafers are used more and more because they allow the epitaxial growth of structures with the high

indium-composition InGaAs channels, providing superior speed and operation frequencies which approach the InAs ones. Furthermore, use of GaN HEMTs is expected to increase sunstantially in future, particularly in the area of power transistors.[217-221] The gate properties of GaN-based HEMTs continue to be investigated and developed in order to realize the full potential of these devices in many applications. The gate stability and normally-off mode (i.e. enhancement HEMT) are crucial targets toward this GaN technology.[217-224] Here the results presented in Section V for the crystalline AlGaN oxidation are very relevant because GaN HEMTs contain typically an AlGaN/GaN junction at the gate area. One main strategy to produce the enhancement-mode GaN HEMT has been the recess gate combined with a thin insulator (e.g. Al_2O_3 or SiO_2 or SiN_x) between AlGaN and a gate metal.[217-224]

Figure 27a shows the HEMT structures with an insulator film at the gate. The current HEMT industry employs largely the GaAs-based heterostructures, grown either in pseudomorphic or metamorphic manner, and containing a high-electron mobility InGaAs channel. The epitaxial film structure above the channel often includes a heteroepitaxial InGaP or AlGaAs or InAlAs film capped still by n-type GaAs which provides Ohmic-type drain and source contacts. Then the gate area is etched to remove n-GaAs and part of InGaP or AlGaAs or InAlAs, to enhance the Schottky-gate control of channel. Another way is to process the gate area first on the as-grown epitaxial structure, and after that, to use a re-growth approach for preparing the highly n-doped drain and source areas. Commercial GaAs-based HEMTs also suffer different degradation mechanisms during the operation, which largely arises from the three different contact areas, and are originating from metal-semiconductor interactions.[218] Indeed it has been investigated the incorporation of a thin insulator film between the gate metal and semiconductor because the gate insulator/III-V interface has a significant effect on the device performance.[17-19,225-232] The insulator barrier at the gate junction can be expected to suppress the intermixing of metal and III-V elements, and to decrease the leakage current through the gate. The role of the surface passivation increases further, when the recess etching is used to remove a part of III-V

material before the gate metallization, because the gate metal becomes a very close to the epitaxial carrier channel. As discussed in Section III, the semiconductor surfaces are very far from the ideal surface after any etching procedure, containing disorder and contaminants. Thus, one question is how to treat and passivate III-V surface in the gate area before the metal deposition. A less studied option is still to use a thin insulator film at the drain and source contact areas too forming the passivated contacts, but for the silicon solar cells a similar approach has been considered and tested.[80-82,233]

Figure 27b exemplifies another current application of III-V crystals: infrared (IR) photodiodes or detectors, which cannot be made of silicon because Si is largely transparent for the technologically crucial infrared wavelengths such as 1550 nm. The use of infrared photodiodes increases continuously due to various applications such optical fiber communication and sensor circuits. The sensors also typically incorporate a III-V infrared light emitter, and such sensors are utilized in diverse industrial areas like aerospace, automotive, and security.[234-241] The surface region of III-V crystals have again a significant role in the IR detector operation.[242-246] III-V surfaces cause losses of the photogenerated carriers via non-radiative recombination processes (Figure 1). On the other hand, the thermal excitation of electrons via the gap levels to the conduction band increases the dark, or leakage current. Both surface effects degrade the signal/noise ratio, and therefore, the development of III-V surface passivation is relevant to the IR diode sector too, to decrease losses and malfunctions. Figure 27b is an example of a large planar type IR detector, but also dense arrays of the mesa-type structures are developed, in particular, for imaging applications. In the mesa structures like in nanostructures, various III-V surfaces are exposed after to the dry or wet etching processing step. That is, the passivation of different crystal orientations becomes relevant; not only for the typical (100) face. The mesa type structure is presented in Figure 27c but it is an example for the third application of III-V crystals: microLED of which passivation becomes more and more relevant to the technology.[247-251] Part of the forward-bias current in the LED is lost at the mesa surfaces via non-radiative recombination.

Furthermore, the semiconductor surfaces and interfaces can cause optical losses,[250,251] in addition to the electrical losses.

Surely, there are many more examples for the current III-V applications such as bonded III-V chips on Si wafers,[252] high-efficiency solar cells,[253] and metal-semiconductor FET[254,255] of which further development includes the target to decrease the surface-induced defect levels. Among the various III-V devices, the MOSFET provides the most stringent test for the surface passivation method under research and development to reduce the D_{it} to low 10^{10} $cm^{-2}eV^{-1}$. However, it is important to note that the passivation method, which works well for MOSFET applications, is not necessarily optimized or even applicable for many other III-V devices. In other words, there are the passivation methods and in particular the combinations of them that do not provide the lowest D_{it} but are still very potential to improve the efficiency of some currently used III-V devices.

B. Comparison of different passivation methods

As described in the introduction, many investigations in 1970s and 80s indicated that amorphous III-V oxidation did not provide the high-quality passivation, attained for the well-known SiO_2/Si system.[6-10] The mainstream effort in the III-V passivation work has entailed avoiding the formation of (or removing) III-V oxides. One of the earliest methods toward that target has been the deposition of a thin silicon interface control layer (Si ICL).[8,9,256-259] The method seeks to reproduce the properties associated with the SiO_2/Si interface. Typically, an amorphous or disordered ultrathin (0.5-1 nm) silicon layer is deposited on a III-V surface at low temperatures (less than 400 ^oC) before an insulator film growth. Si can be deposited from solid or gas sources. The post-deposition annealing of the stack of insulator/Si/III-V has been often performed after the growth of insulator film(s). Thus, the Si ICL becomes oxidized at least partly. Indeed the Si ICL approach has provided the interface defect-level densities (D_{it}) that are among the lowest D_{it} values reported in literature,[256,258] $\sim 10^{10}$ $eV^{-1}cm^{-2}$, which are

in fact close to D_{it} of a well-passivated SiO_2/Si system. Table III presents and compares the D_{it} values for different passivation methods. One challenge in the Si ICL method is a possible interaction between III-V and Si because small Si atoms can readily diffuse toward III-V, in particular, at elevated temperatures. On the other hand, such intermixing provides an interesting way to increase the n-type doping concentration at many III-V surfaces (i.e. Si substitution of elements III can causes the shallow donor level), which should be beneficial for the Ohmic n-contacts for instance.

The other passivation method that has been also investigated already for several decades is based on incorporating sulfur at III-V interfaces.[107-112,260-268] The wet chemistry (e.g. dip in $(NH_4)_2S$ solution) has been mostly used for the sulfur incorporation because it is a simple and scalable method, and thus has the potential to be integrated with industrial manufacturing procedures. Because sulfur-containing solutions like $(NH_4)_2S$ are not a strong etchant typically for III-V surface oxides, a complementary wet chemistry such as HCl etching is often combined with the sulfur passivation. The sulfur-based passivation has also led to a low D_{it} ~10^{10} $eV^{-1}cm^{-2}$, as well as to proper MOSFET operation for SiO_2/InP interface.[258] On the other hand, a pure sulfur treatment is not typically durable or stable enough in reactive environments like in air, and the resultant passivation effect vanishes with the time.[263-265] Therefore, the sulfur treatment is often combined with a capping or encapsulation of III-V crystals by a thin film. For example, ALD after the sulfur treatment is the common capping method.[110-112,263-265]

Since the beginning of 2000s, use of the ALD method has continuously increased in semiconductor industry.[269-288] It can be also predicted that ALD will become even more popular in future because it enables the growth of conformal coatings for nanostructures and three-dimensionally structured surfaces at low temperatures (< 400 ^oC). The low temperature processing is needed as different materials are integrated with semiconductor crystals to produce hybrid materials and three-dimensionally stacked heterostructures. So far HfO_2 and Al_2O_3 insulating films are the most common materials grown by ALD. A very interesting property of ALD on III-V's concerning the passivation is the self cleaning

of III-V surfaces during ALD.[271-275] Promising D_{it} values ~10^{11} $eV^{-1}cm^{-2}$ and very low leakage current through the oxide interface: 2×10^{-9} A/cm^2 at ±2V have been obtained by utilizing ALD (Table III). Another very promising result found in ALD-based studies is the growth of epitaxial La_2O_3/GaAs and MgCaO/GaN interfaces by means of ALD.[35,36]

Furthermore, ALD is often combined with the preparation of a specific interface layer before ALD. The interface layer can contain the above-described sulfur treatment and/or Si ICL. Recently also ZnO and ZnS as well as AlN interface layers have been investigated.[277-280] A specific property of Zn is its potential for the p-type doping of many III-V's, which needs to be taken into account when planning the III-V passivation. Moreover, the incorporation of fluorine into InAs surface has been found to decrease D_{it} down to ~10^{10} $eV^{-1}cm^{-2}$ level.[281] Fluorine passivation has been also studied for silicon (e.g. Ref. 282) because strong bonding between Si and F, as compared to Si-H bond, can provide a more stable chemical passivation than hydrogen. However, harmful effects (e.g. decrease in n-type doping efficiency) have been also found because of the fluorine incorporation into III-V.[283-285] Another interesting finding is also that an amorphous InAs oxide, prepared in a UHV chamber, can be used as the interface layer before ALD.[286]

The chemical passivation with hydrogen is often the last step in a well optimized passivation procedure of SiO_2/Si interfaces.[73,74,84,100] Hydrogen incorporation into Si dangling bonds is understood to remove part of the Si dangling-bond induced gap levels far away from the Si band gap area (i.e. deep to the valence and conduction bands) via the Si-H bonding. Such hydrogen passivation is often performed by heating SiO_2/Si interfaces in a "forming gas" environment (e.g. 95%N_2+5%H_2) at around 400-500 ºC. The current understanding is that a proper forming gas annealing (FGA) also decreases D_{it} at III-V interfaces, but there is still room for optimizing the hydrogen passivation of III-V device interfaces.[101-106,289-292] One potential way is a concomitant nitridation of III-V surfaces resulting a III-N nitride passivation together with hydrogen.[287] Benefits of the hydrogen passivation include simplicity

and scalability of the method as well as the low operation temperature, latter of which means that the ready components with the metal contacts can be also treated by FGA. On the other hand, excessive hydrogen incorporation into insulator films can be harmful to device operations.[293]

We then return to the MBE method introduced already in the introduction section. The option for electron-beam deposition and/or thermal deposition of films has been typically integrated with MBE.[24-28,294-299] One of the lowest D_{it}, 5×10^{10} $eV^{-1}cm^{-2}$ was obtained by means of the MBE passivation for Ga_2O_3/GaAs interface.[26] That is consistent also with the PL results showing almost same PL intensity for Ga_2O_3/GaAs and epitaxial AlGaAs/GaAs systems.[187-189] Undoubtedly MBE enables the preparation of the cleanest and most crystalline (or most well-ordered) starting surfaces, which are often reconstructed with a large surface unit cell (Section III and Figure 3). Furthermore, MBE enables a control of the doping level at III-V surfaces. Moreover, RHEED is normally integrated with MBE, allowing in-situ control of the III-V surface modification and insulator growth. MBE has been also used for sulfur passivation in sophisticated way via preparing sulfur-induced III-V(100)(2×1)-S reconstructed passivation layer.[297] It is however admitted that MBE is a relatively complex instrument. The method is particularly suitable for so-called front-end-of-line material growth and passivation, but the use of MBE during the device prosessing and in the back-end-of-line device fabrication stages is not straightforward. It is noted however that the multichamber tools (equipped with capabilities such as sputter deposition, ALD, annealing, etc.) employed for contemporary, wafer-scale semiconductor integrated circuit manufacturing are quite sophisticated, and include the ability to obtain pressures down to ~10^{-9} mbar in some processes. Provided through put could be established, tool innovation for the crystalline oxidation approach remains a real possibility.

The crystalline monolayer oxidation method utilizes the UHV environment similarly to the method of MBE. However, the instrumental requirements for the crystalline oxidation (Figure 4) are not

as high as for MBE. The D_{it} value of 2×10^{11} $eV^{-1}cm^{-2}$ has been reported for the InAs crystalline oxidation,[54] and D_{it} ~10^{12} $eV^{-1}cm^{-2}$ has been found for the crystalline oxidation of InGaAs (Table III),[63] while the leakage current of 5×10^{-9} A/cm^2 at 2 V was measured for Al_2O_3/InAs-(3×1)-O.[66] As the reviewed studies also present, the crystalline oxidation can be combined with the ALD method, as one part of the passivation procedure. Because thin crystalline oxidized layers have been found to unstable in air and in ALD growth,[53,62] it is indeed reasonable to integrate the crystalline oxidation as one step of multistep passivation procedures, similarly to the above sulfur and Si ICL methods. On the other hand, the crystalline oxidation method allows one to modify (or continue) the preparation of clean and crystalline starting surfaces in UHV conditions, and after that to control the oxidation of III-V surfaces, which is difficult to avoid in practice.[63]

The crystalline oxidation approach can be considered to belong to a category of the intentional oxidation methods. Although the III-V community has strived to avoid any oxidation of the surfaces, promising thermal-oxidation results for III-V's have been reported, as mentioned in the introduction.[37-45,300-302] The resulting surface oxides have demonstrated an amorphous or disordered nature, as expected, but also a clear indication of interfacial crystallization has been measured for the thermal oxidation of InAs in non-UHV conditions.[45] Moreover, an interesting combination (O_2 flow in ozone cleaner + $(NH_4)_2S$ + ALD) has been recently used in processing of high-quality III-V MOSFET.[300] Another approach of the intentional oxidations has been the oxidation of relatively thick aluminum-containing III-V epitaxial insulating films (e.g. AlInP and AlGaAs).[38-44,301,302] Indeed this is a very promising method to develop both the III-V transistors and optoelectronics because it enables a selective oxidation of III-V layers via a strong oxidation tendency of aluminum, as compared to the other III-V elements. This subsection can be closed by citing Hollinger et al.[37] once again: "Our results show, in

contrast to what is generally assumed in the literature, that some specific native oxides are able to exhibit good electrical properties."

Similarly to the intentional surface oxidation approach, an intentional nitridation of III-V surfaces have been studied for the passivation.[303-307] For example the nitridation of GaAs to form a GaN surface layer is indeed a potential method to decrease the oxidation induced defects because the GaN bonding is strong, reducing the oxygen incorporation. Thus, a thin nitride passivation layer is more robust against air exposure than for example a sulfur layer.[307] On the other hand, it has been found that possible N dangling bonds are not harmful to electrical properties because the N dangling-bond induced electron levels lie deep in the valence band as compared to the GaAs band gap.[308]

C. Toward integration of crystalline oxidation with multistep passivation procedures

The sophisticated As-decapping technique has been previously used to integrate the crystalline oxidation in the studies of III-V passivation using electrical characterization.[54,63,64,66] In order to extend the device passivation tests of the crystalline oxidation, a more general and simple method to perform the cleaning step (i.e. the 1. step in Figure 4) should be considered. It is also worth noting that during the device processing, several mask or patterning stages have been done before the final surface passivation. That is; the passivated surface is often a three-dimensionally structured (e.g. mesa or nanowire surface).[309,310] Indeed, significant development of III-V nanowires has been obtained for future devices (e.g. Refs. 311-316). One obvious solution is to utilize the wet chemical etching that has been already used for long in the semiconductor industry,[317] as described in the Section III. Although the plasma-based dry etching is commonly used to produce uniform patterns of 3D structures, it is still possible to carry out a short, or gentle wet etching after the dry etching. That approach might be indeed useful because the surface parts become contaminated at least to some extent during the dry etching process.

It was presented in Figure 2 that the HCl-based etching of InP(100) in N_2 background combined with a proper UHV heating provided the clean surface with an improved crystal structure. This result is consistent with the previous surface-science results on HCl-etched GaAs(100).[120,121] Similar wet chemical etching was recently[65] combined with the crystalline oxidation in proof of concept manner to demonstrate that such an industrially potential route is possible. Here it is worth noting that all the crystalline oxidations described above were done for the III-V surfaces which were cleaned by either the Ar-ion sputtering or the As decapping technique. Therefore it is relevant to the technology that the full process was performed in industrially compatible way for the InSb(111)B surface, providing simultaneously a complementary HCl+IPA etching "test" for the III-V member of antimonides.[65]

After the HCl+IPA treatment, a piece of InSb(111)B was transferred to the vacuum system via air (about two minutes air exposure). Such an inert property of the HCl-etched surface can be understood by extra antimony formed during the etching, consistent also with the enrichment of arsenic at the III-V surfaces due to the HCl treatment.[120,121] Indeed Sb decapping technique has been also used previously on InSb and GaSb (e.g. Refs. 213, 318), in a similar way to the more common As decapping method. Thus, extra Sb prevents the spurious oxidation while oxidized Sb can be still removed by low temperature vacuum heating. Figure 28 presents how the vacuum heating around 300 ^{o}C results in a (2×2) LEED for InSb(111)B, and when the temperature was increased to 400 ^{o}C, the LEED changed to (3×3) pattern. During the latter heating, the InSb(111)B piece was exposed to a molecular hydrogen exposure (1×10^{-5} mbar), which was found to improve the (3×3) LEED pattern. The STM image in Figure 28 for this surface shows a smooth terrace-step structure, and a zoomed-in image shows atomic scale ordering. After that the (3×3) surface was still oxidized in the same way as described in Section VA, to produce the oxidized (2×2)-O layer.

As mentioned above, the wet chemical etching can be readily integrated with current passivation methods, and with three-dimensionally structured devices. For example, the HEMT gate area is often recess etched toward the channel to improve the gate control. After that, the HCl-based treatment provides a group-V enriched III-V gate surface which can be still vacuum treated and oxidized in the controlled way. Finally, the ALD can provide an elegant way to grow a thin insulator film in conformal way.[269,270]

VII. SUMMARY AND OUTLOOK

It can be expected that the use of III-V compounds will continue to expand in the electronics/photonics industry, particularly, in the application areas where the natural properties of III-V crystals are superior compared to the main workhorse of silicon. These devices include the light emitters, infrared sensors, and high-speed MMIC circuits. Furthermore, low-power transistor devices might form in future one application area of III-V crystals. As discussed in Ref. 300, it has been shown that state-of-the-art III-V MOSFET components can even outperform the corresponding large-scale integrated Si MOSFET within some metrics.

The vulnerability of most III-V devices (like semiconductor devices in more general) is that surfaces of the crystals become exposed to diverse processing conditions, leading to the electronic defect levels around the band gap and finally to the electrical degradation in many currently used III-V devices. The devices have different critical surface or interface areas; for example, at the insulator/III-V and metal/III-V junctions and on the mesa or chip sidewalls. One of the main reactions of III-V surfaces with the environment is the oxidation of III-V surfaces. The review shows that it is impossible to avoid the III-V oxidation in practical devices (Section II). Therefore, the long-standing goal to avoid any oxidation of III-V surfaces in the technology appears to be quite challenging. Such unintentional oxygen incorporation into device surfaces has occurred in non-controlled manner. Thus, a relevant hypothesis is

whether it is still beneficial to try to incorporate oxygen atoms intentionally and in more controlled manner during the multistep passivation procedure, to reduce losses in the current and future devices.

This review aims to explore and test that hypothesis. First it was recapitulated that already in 1986 the researchers concluded the potential of the intentional oxidation of III-V.[37] After that work, promising results have been obtained also by intentional oxidation of Al-containing III-V materials particularly. This review focused on the results obtained during the last 10 years for the intentionally oxidized III-V surfaces that remain crystalline in contrast to the normal amorphous surface oxides of III-V's typically reported. The key to observing these monolayer crystalline oxidized III-V surfaces was the preparation of clean and long-range ordered starting surfaces of III-V crystals, resembling the epitaxial SiO_2/Si interface, and thereby minimizing point defects, such as dangling bonds, at the interface.[91] In Section III, it has been emphasized how difficult it is to obtain and maintain the clean and crystalline semiconductor surface. Furthermore, most characterization methods, even surface-science techniques, are not conclusive enough to determine whether the topmost surface part is sufficiently crystallized. A justified conclusion about that arises typically from combining the complementary surface probes, and it is often very instructive to check the scanning probe microscopy image for the surface before a film growth.

It has been underlined that ultrahigh vacuum (UHV) technology plays an important role in preparing and keeping a clean and crystalline III-V surface for the controlled oxidation performed also in UHV conditions. Thus, it is suggested to combine the industrially applicable wet chemical etching and the UHV technology at one stage of the multistep procedure of the semiconductor surface passivation. It is interesting to test in future if less demanding vacuum conditions, as compared to UHV, can be utilized toward that target as well. The benefit of the HCl-based etching treatment is that it often provides a group-V enriched III-V surface which can tolerate even short air exposure, resembling the special As- or Sb- decapping technique. Then a subsequent UHV heating can be used to produce a clean and crystalline

III-V starting surface for growing an insulator/ or metal/III-V junction. A useful fingerprint for the clean and crystalline III-V surface is its reconstruction(s) which can be monitored by the common surface diffraction probes.

The RHEED and LEED diffraction techniques are useful also to monitor the crystalline oxidation because the most crystalline oxidized III-V surfaces have an own specific reconstruction lattice, different from the clean surface lattices. However, there are exceptions such as the oxidation of InSb(111) is a good example. The monolayer crystalline oxidation of pure GaAs or GaSb surface has not been demonstrated to date, although ordering of the deposited Ga_2O molecule layers on GaAs has been observed.[29,31] Furthermore, one of the earliest results[46] on the crystalline oxidation of III-V via the GaN oxidation indicates that increasing the Ga amount on GaAs or GaSb might be useful toward the crystalline oxidation. Moreover, adding even small amount of indium on the GaAs and GaSb surfaces enables the crystalline oxidation.[50,59,60] Future theoretical calculations can clarify the reason for such an indium-or gallium-mediated property.

Another interesting indium-related property is linked to the indium core-level spectra that are often used in the research and development of III-V materials. Namely there is now a significant body of the results showing that the crystalline oxidation and more generally indium oxidation at the insulator/III-V interfaces can decrease the indium core-level binding energy as compared to the In-V bulk crystal. Such oxidation-induced smaller binding-energy shifts are unusual because the oxidation of Si and Ge as well as group-V elements has been established to cause clear higher binding-energy shifts. This result should be taken into account in the widely used XPS analyses of indium core-level spectra, to find an answer to the question whether a III-V surface is oxidized, by means of the fitting procedure which is not unambiguous. To develop the XPS analysis, it is useful to combine theoretically calculations and simulated core-level shifts to understand the detailed atomic structures at III-V interfaces that can cause the core-level shifts.

The electrical measurements of HfO_2/III-V and Al_2O_3/III-V interfaces with the crystalline oxidation have shown a clear decrease in the interface defect density, as compared to reference samples without the crystalline oxidation. Some previous passivation methods have however provided even lower D_{it} values (Table III). In Section VI, we have summarized a large arsenal of currently used passivation methods. Each method has own strengths and weaknesses. The most promising passivation approach depends probably on the device type. However, it can be concluded that the finding of a proper combination of complementary methods among the large arsenal of the passivation methods is needed to develop the passivation for the current and future III-V devices, to decrease the performance degradation. The intentional oxidations, including the crystalline oxidation form one instrument for the arsenal.

In this review it has been attempted to make a comparison to the best possible insulator/semiconductor interface: SiO_2/Si. Although there are clear differences between the natural properties of Si and III-V (e.g. the heating tolerance; the ionic vs. covalent character of the oxygen bonds; intrinsic carrier lifetimes), the following observations: the crystallization of deposited Ga_2O and In_2O molecule layers,[29,31,47-49] and thermally oxidized crystalline InAs,[45] as well as the crystalline oxidized III-V surfaces (Section V) can be seen to resemble the crystalline tridymite SiO_2 interface layer at high quality SiO_2/Si junctions. Even if researchers and engineers have learned during the last 40 years to avoid the mimicking of Si interfaces, for very good reasons, there might be still, at least, one potential method to adopt from the Si community for testing more within the III-V interfaces. Namely, the field-effect passivation which has been intensively studied and developed, in particular, for silicon solar cells.[319-322] For example, it has been found to methods to produce so-called fixed negative charges at the Al_2O_3/Si and HfO_2/Si junctions, which provide an internal electric field to repel electrons away from the defect-containing interfaces. The origin of this field-effect passivation is still an open issue, but it has been associated with Al_2O_3/SiO_2 or HfO_2/SiO_2 interfaces.[319] This might open paths to modify the internal

electric field at the insulator/III-V device interfaces as well by growing a stack of the insulator films for example by ALD.

ACKNOWLEDGMENTS

First, we would like to thank our great students and colleagues in Turku: PhD Johnny Dahl, MSc Marjukka Tuominen, PhD Jaakko Mäkelä, and MSc Vicente Calvo, who have worked at Comptek Solutions Inc. Then we would like to thank our great colleagues in Tampere University: Dr Ville-Markus Korpijärvi, Dr Ville Polojärvi, Dr Antti Tukiainen, Dr Jari Lyytikäinen, and Prof. Mircea Guina, who have developed III-V technology for long, for fruitful collaboration. This work has been supported by the Academy of Finland (via the project #296469) and by the Business Finland (via TUTLI project; code: COMNINT). RMW wishes to acknowledge his former students, Dr. Xiaoye Qin and Dr. Dmitry Zhirnokletov for their work at the UT-Dallas on epi-oxide interfaces, and the support of the Erik Jonsson Distinguished Chair, the National Science Foundation (award Nos. ECCS 1802167, ECCS 1917025 and DMR 2002741), and the Semiconductor Research Corporation NEWLIMITs Center and NIST (award #70NANB177H041) during the preparation of this review.

* Correspondence emails: pekka.laukkanen@utu.fi, rmwallace@utdallas.edu

The data that support the findings of this study are available from the corresponding authors upon reasonable request

REFERENCES

[1] M. B. Panish, I. Hayashi, and S. Sumski, Double-heterostructure injection lasers with room-temperature thresholds as low as 2300 A/cm^2. Appl. Phys. Lett. **16**, 326 (1970).

[2] R. D. Dupuis, P. D. Dapkus, N. Jr. Holonyak, E. A. Rezek, and R. Chin, Room temperature operation of quantum-well $Ga_{(1-x)}Al_{(x)}As$-GaAs laser diodes grown by metalorganic chemical vapor deposition. Appl. Phys. Lett. **32**, 295 (1978).

[3] R. Dingle, H. L. Störmer, A. C. Gossard, and W. Wiegmann, Electron mobilities in modulation-doped semiconductor heterojunction superlattices. Appl. Phys. Lett. **33**, 665 (1978).

[4] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, A new field-effect transistor with selectively doped GaAs/n-AlGaAs heterostructures. Jpn. J. Appl. Phys. **19**, L225 (1980).

[5] G. P. Schwartz, Analysis of native oxide films and oxide-substrate reactions on III-V semiconductors using thermochemical phase diagrams. Thin Sol. Films **103**, 3 (1983).

[6] W. Wilmsen, Physics and Chemistry of III-V Compound Semiconductor Interfaces, Plenum (1985).

[7] P. D. Ye, Main determinants for III–V metal-oxide-semiconductor field-effect transistors. J. Vac. Sci. Technol. A **26**, 697 (2008).

[8] H. Hasegawa and M. Akazawa, Interface models and processing technologies for surface passivation and interface control in III-V semiconductor nanoelectronics. Appl. Surf. Sci. **254**, 8005 (2008).

[9] Fundamentals of III-V Semiconductor MOSFETs, edited by S. Oktyabrsky and P. D. Ye. Springer (2010).

[10] J. del Alamo, Nanometre-scale electronics with III-V compound semiconductors. Nature **479**, 317 (2011).

[11] M. Passlack, C. G. Bethea, W. S. Hobson, J. Lopata, E. F. Schubert, G. J. Zydzik, D. T. Nichols, J. F. de Jong, U. K. Chakrabarti, and N. K. Dutta, Infrared microscopy studies on high-power InGaAs-GaAs-InGaP lasers with Ga_2O_3 facet coating. IEEE J. Select. Top. Quant. Electr. **1**, 110 (1995).

[12] N. K. Dutta, W. S. Hobson, G. J. Zydzik, J. F. de Jong, P. Parayanthal, M. Passlack, and U. K. Chakrabart, Mirror passivation of InGaAs lasers. Electron. Lett. **33**, 213 (1997).

[13] M. S. Wong, D. Hwang, A. I. Alhassan, C. Lee, R. Ley S. Nakamura, and S. P. DenBaars, High efficiency of III-nitride micro-lightemitting diodes by sidewall passivation using atomic layer deposition. Optics Expr. **26**, 21324 (2018).

[14] David P. Bour, K. McGroddy, D. A. Haeger, J. M. Perkins, A. Chakraborty, and J.-J. P. Drolet, LED structures for reduced non-radiative sidewall recombination, US Patent US 9.484,492 B2 (2016).

[15] J. F. Klem, J. K. Kim, M. J. Cich, G. A. Keeler, S. D. Hawkins, and T. R. Fortune, Mesa-isolated InGaAs photodetectors with low dark current. Appl. Phys. Lett. **95**, 031112 (2009).

[16] A. Higuera-Rodriguez, B. Romeira, S. Birindelli, L. E. Black, E. Smalbrugge, P. J. van Veldhoven, W. M. M. Kessels, M. K. Smit, and A. Fiore, Ultralow surface recombination velocity in passivated InGaAs/InP nanopillars. Nano Lett. **17**, 2627 (2017).

[17] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, GaN MOS-HEMT using atomic layer deposition Al_2O_3 as gate dielectric and surface passivation. Intern. J. High Speed Electr. Systems **14**, 791 (2004).

[18] T.-W. Kim, D.-H. Kim, D. H. Koh, H. M. Kwon, R. H. Baek, D. Veksler, C. Huffman, K. Matthews, S. Oktyabrsky, A. Greene, Y. Ohsawa, A. Ko, H. Nakajima, M. Takahashi, T. Nishizuka, H. Ohtake, S. K. Banerjee, S. H. Shin, D.-H. Ko, C. Kang, D. Gilmer, R.J.W. Hill, W. Maszara, C. Hobbs, and P. D. Kirsch, Sub-100 nm InGaAs quantum-well (QW) tri-gate MOSFETs with Al_2O_3 /HfO_2 (EOT < 1 nm) for low-power logic applications. Int. Electr. Dev. Meet. IEDM13-426 16.3.1 (2013).

[19] J. A. del Alamo, InGaAs MOSFET electronics, The 17th International Symposium Physics of Semiconductors and Applications (2014).

[20] R. K. Basset: To the Digital Age: Research Labs, Start-Up Companies, and the Rise of MOS Technology. Johns Hopkins University Press, United States (2002).

[21] C. L. Hinkle, E. M. Vogel, P. D. Ye, and R. M. Wallace, Interfacial chemistry of oxides on $In_xGa_{(1-x)}As$ and implications for MOSFET applications. Curr. Opin. Sol. State Mat. Sci. **15**, 188 (2011).

[22] R.V. Galatage, D. M. Zhernokletov, H. Dong, B. Brennan, C. L. Hinkle, R. M. Wallace, and E. M. Vogel, Accumulation capacitance frequency dispersion of III-V metal-insulator-semiconductor devices due to disorder induced gap states. J. Appl. Phys. **116**, 014504 (2014).

[23] R. M. Wallace and P. C. McIntyre, Atomic layer deposition of high-k dielectrics on III-V materials. Reference Module in Materials Science and Materials Engineering, Elsevier (2016).

[24] M. Passlack, M. Hong, J. P. Mannaerts, J. R. Kwo, and L. W. Tu, Recombination velocity at oxide–GaAs interfaces fabricated by in situ molecular beam epitaxy. Appl. Phys. Lett. **68**, 3605 (1996).

[25] M. Passlack, M. Hong, and J. P. Mannaerts, Quasistatic and high frequency capacitance–voltage characterization of Ga_2O_3–GaAs structures fabricated by in situ molecular beam epitaxy. Appl. Phys. Lett. **68**, 1099 (1996).

[26] M. Passlack, M. Hong, J. P. Mannaerts, R. L. Opila, S. N. G. Chu, N. Moriya, F. Ren, and J. R. Kwo, Low D_{it} thermodynamically stable Ga_2O_3-GaAs interfaces: fabrication, characterization, and modeling. IEEE Trans. Electr. Dev. **44**, 214 (1997).

[27] J. Kwo, D. W. Murphy, M. Hong, R. L. Opila, J. P. Mannaerts, A. M. Sergent, and R. L. Masaitis, Passivation of GaAs using $(Ga_2O_3)_{1-x}(Gd_2O_3)_x$, $0 \leq x \leq 1.0$ films. Appl. Phys. Lett. **75**, 1116 (1999).

[28] M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent, Epitaxial cubic gadolinium oxide as a dielectric for gallium arsenide passivation. Science **283**, 1897 (1999).

[29] R. Droopad, M. Passlack, N. England, K. Rajagopalan, J. Abrokwah, and A. Kummel, Gate dielectrics on compound semiconductors. Microelectr. Engineer. **80**, 138 (2005).

[30] M. Passlack, J. K. Abrokwah, R. Droopad, Z. Yu, C. Overgaard, S. I. Yi, M. Hale, J. Sexton, and A. C. Kummel, Self-aligned GaAs p-channel enhancement mode MOS heterostructure field-effect transistor. IEEE Electr. Dev. Lett. **23**, 508 (2002).

[31] D. M. J. Hale, S. I. Yi, J. Z. Sexton, A. C. Kummel, and M. Passlack, Scanning tunneling microscopy and spectroscopy of gallium oxide deposition and oxidation on GaAs(001)-c(2×8)/(2×4). J. Chem. Phys. **119**, 6719 (2003).

[32] D. L. Winn, M. J. Hale, T. J. Grassman, J. Z. Sexton, A. C. Kummel, M. Passlack, and R. Droopad, Electronic properties of adsorbates on GaAs(001)-c(2×8)/(2×4). J. Chem. Phys. **127**, 134705 (2007).

[33] T. D. Lin, W. H. Chang, R. L. Chu, Y. C. Chang, Y. H. Chang, M. Y. Lee, P. F. Hong, M.-C. Chen, J. Kwo, and M. Hong, High-performance self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect-transistors by in-situ atomic-layer-deposited HfO_2. Appl. Phys. Lett. **103**, 253509 (2013).

[34] M. Hong, H. W. Wan, K. Y. Lin, Y. C. Chang, M. H. Chen, Y. H. Lin, T. D. Lin, T. W. Pi and J. Kwo, Perfecting the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfacial electronic structure in pushing metal-oxide-semiconductor field-effect-transistor device limits using in-situ atomic-layer-deposition. Appl. Phys. Lett. **111**, 123502 (2017).

[35] X. Lou, H. Zhou, S. B. Kim, S. Alghamdi, X. Gong, J. Feng, X. Wang, P. D. Ye, and R. G. Gordon, Epitaxial growth of $Mg_xCa_{1-x}O$ on GaN by atomic layer deposition. Nano Lett. **16**, 7650 (2016).

[36] X. Wang, L. Dong, J. Zhang, Y.Liu, P. D. Ye, and R. G. Gordon, Heteroepitaxy of La_2O_3 and $La_{2-x}Y_xO_3$ on GaAs (111)A by atomic layer deposition: achieving low interface trap density. Nano Lett. **13**, 594 (2013).

[37] Y. Robach, J. Joseph, E. Bergignat, B. Commere, G. Hollinger, and P. Viktorovitch, New native oxide of InP with improved electrical interface properties. Appl. Phys. Lett. **49**, 1281 (1986).

[38] J. M. Dallesasse, N. Holonyak, A. R. Sugg, T. A. Richard, and N. El-Zein, Hydrolyzation oxidation of $Al_xGa_{1-x}As$-AlAsGaAs quantum well heterostructures and superlattices. Appl. Phys. Lett. **57**, 2844 (1990).

[39] J. M. Dallesasse and N. Holonyak Jr., Oxidation of Al-bearing III-V materials: A review of key progress. J. Appl. Phys. **113**, 051101 (2013).

[40] E. F. Schubert, M. Passlack, M. Hong, J. Manner, R. L. Opila, L. N. Pfeiffer, K. W. West, C. G. Bethea, and G. J. Zydzik, Properties of Al_2O_3 optical coatings on GaAs produced by oxidation of epitaxial AIAs/GaAs films. Appl. Phys. Lett. **64**, 2976 (1994).

[41] T. Kagiyama, Y. Saito, K. Otobe, and S. Nakajima, Improvement of power performance in planar type AlGaAs/GaAs MESFET by substrate surface oxidation. Appl. Surf. Sci. **216**, 542 (2003).

[42] X. Li, Y. Cao, D. C. Hall, P. Fay, B. Han, A. Wibowo, and N. Pan, GaAs MOSFET using InAlP native oxide as gate dielectric. IEEE Electr. Dev. Lett. **25**, 772 (2004).

[43] Y. Cao, J. Zhang, X. Li, T. H. Kosel, P. Fay, D. C. Hall, X. B. Zhang, R. D. Dupuis, J. B. Jasinski, and Z. Liliental-Weber, Electrical properties of native oxides for metal–oxide–semiconductor device applications. Appl. Phys. Lett. **86**, 062105 (2005).

[44] J. Zhang, T. H. Kosel, D. C. Hall, and P. Fay, Fabrication and performance of 0.25-μm gate length depletion-mode GaAs-channel MOSFETs with self-aligned InAlP native oxide gate dielectric. IEEE Electr. Dev. Lett. **29**, 143 (2008).

[45] H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, E. Plis, H. S. Kim, S.-Y. Chen, M. Madsen, A. C. Ford, Y.-L. Chueh, S. Krishna, S. Salahuddin, and A. Javey, Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors. Nature **468**, 286 (2010).

[46] Y. Dong, R. M. Feenstra, and J. E. Northrup, Oxidized GaN(0001) surfaces studied by scanning tunneling microscopy and spectroscopy and by first-principles theory. J. Vac. Sci. Technol. B **24**, 2080 (2006).

[47] J. J. Shen, PhD thesis: Atomic and electronic structures of oxides on III-V semiconductors. University of California, San Diego, US (2010).

[48] D. J. Shen, E. A. Chagarov, D. L. Feldwinn, W. Melitz, N. M. Santagata, A. C. Kummel, R. Droopad, and M. Passlack, Scanning tunneling microscopy/spectroscopy study of atomic and electronic structures of In_2O on InAs and $In_{0.53}Ga_{0.47}As(100)(4\times2)$ surfaces. J. Chem. Phys. **133**, 164704 (2010).

[49] J. B. Clemens, S. R. Bishop, J. S. Lee, A. C. Kummel, and R. Droopad, Initiation of a passivated interface between hafnium oxide and In(Ga)As(001)−(4×2). J. Chem. Phys. **132**, 244701 (2010).

[50] M. P. J. Punkkinen, P. Laukkanen, J. Lång, M. Kuzmin, M. Tuominen, V. Tuominen, J. Dahl, M. Pessa, M. Guina, K. Kokko, J. Sadowski, B. Johansson, I. J. Väyrynen, and L. Vitos, Oxidized In-containing III-V(100) surfaces: Formation of crystalline oxide films and semiconductor-oxide interfaces. Phys. Rev. B **83**, 195329 (2011).

[51] P. Laukkanen, J. Lång, V. Tuominen, M. Tuominen, J. Dahl, M. P. J. Punkkinen, and J. Väyrynen, Method for treating a substrate and a substrate. Patent FI20106181 (2010); US10256290B2.

[52] M. P. J. Punkkinen, P. Laukkanen, J. Lång, M. Kuzmin, J. Dahl, H. L. Zhang, M. Pessa, M. Guina, L. Vitos, and K. Kokko, Structure of ordered oxide on InAs(100) surface. Surf. Sci. **606**, 1837 (2012).

[53] D. M. Zhernokletov, P. Laukkanen, H. Dong, R. V. Galatage, B. Brennan, M. Yakimov, V. Tokranov, J. Kim, S. Oktyabrsky, and R. M. Wallace, Surface and interfacial reaction Study of InAs(100)-crystalline oxide interface. Appl. Phys. Lett. **102**, 211601 (2013).

[54] C. H. Wang, S. W. Wang, G. Doornbos, G. Astromskas, K. Bhuwalka, R. Conteras-Guerrero, M. Edirisooriya, J. S. Rojas-Ramirez, G. Vellianitis, R. Oxland, M. C. Holland, C. H. Hsieh, P. Ramvall, E. Lind, W. C. Hsu, L.-E. Wernersson, R. Droopad, M. Passlack, and C. H. Diaz, InAs hole inversion and bandgap interface state density of 2×10^{11} $cm^{-2}eV^{-1}$ at HfO_2/InAs interfaces. Appl. Phys. Lett. **103**, 143510 (2013).

[55] X. Qin, H. Dong, J. Kim, and R. M. Wallace, A crystalline oxide passivation for Al_2O_3/AlGaN /GaN. Appl. Phys. Lett. **105**, 141604 (2014).

[56] M. Passlack, S.-W. Wang, G. Doornbos, C.-H. Wang, R. Contreras-Guerrero, M. Edirisooriya, J. Rojas-Ramirez, C.-H. Hsieh, R. Droopad, and C. H. Diaz, Lifting the off-state bandgap limit an InAs channel metal-oxide-semiconductor heterostructures of nanometer dimensions. Appl. Phys. Lett. **104**, 223501 (2014).

[57] J. J. K. Lång, M. P. J. Punkkinen, M. Tuominen, H.-P. Hedman, M. Vähä-Heikkilä, V. Polojärvi, J. Salmi, V.-M. Korpijärvi, K. Schulte, M. Kuzmin, R. Punkkinen, P. Laukkanen, M. Guina, and K. Kokko, Unveiling and controlling the electronic structure of oxidized semiconductor surfaces: crystalline oxidized InSb(100)(1×2)-O. Phys. Rev. B **90**, 045312 (2014).

[58] M. Tuominen, J. Lång, J. Dahl, M. Kuzmin, M. Yasir, J. Mäkelä, J. Osiecki, K. Schulte, M. P. J. Punkkinen, P. Laukkanen, K. Kokko, Oxidized crystalline (3×1)-O surface phases of InAs and InSb studied by high-resolution photoelectron spectroscopy. Appl. Phys. Lett. **106**, 011606 (2015).

[59] M. Tuominen, M. Yasir, J. Lång, J. Dahl, M. Kuzmin, J. Mäkelä, M. Punkkinen, P. Laukkanen, K. Kokko, K. Schulte, R. Punkkinen, V.-M. Korpijärvi, V. Polojärvi, and M. Guina, Oxidation of GaAs semiconductor at the Al_2O_3/GaAs junction. Phys. Chem. Chem. Phys. **17**, 7060 (2015).

[60] J. Mäkelä, M. Tuominen, M. Yasir, M. Kuzmin, J. Dahl, M. P. J. Punkkinen, P. Laukkanen, K. Kokko, and R. M. Wallace: Oxidation of GaSb(100) and its control studied by scanning tunneling microscopy and spectroscopy. Appl. Phys. Lett. **107**, 061601 (2015).

[61] R. Oxland, X. Li, S. W. Chang, S. W. Wang, T. Vasen, P. Ramvall, R. Contreras-Guerrero, J. Rojas-Ramirez, M. Holland, G. Doornbos, Y. S. Chang, D. S. Mcintyre, S. Thoms, R. Droopad, Y.-C. Yeo, C. H. Diaz, I. G. Thayne, and M. Passlack, InAs FinFETs with H_{fin} = 20 nm fabricated using a top-down etch process. IEEE Electr. Dev. Lett. **37**, 261 (2016).

[62] X. Qin, W.-E. Wang, M. S. Rodder, and R. M. Wallace, In situ surface and interface study of crystalline (3×1)-O on InAs. Appl. Phys. Lett. **109**, 041601 (2016).

[63] X. Qin, W.-E. Wang, R. Droopad, M. S. Rodder, and R. M. Wallace, A crystalline oxide passivation on $In_{0.53}Ga_{0.47}As$(100). J. Appl. Phys. **121**, 125302 (2017).

[64] J. Mäkelä, M. Tuominen, J. Dahl, S. Granroth, M. Yasir, J.-P. Lehtiö, R.-R. Uusitalo, M. Kuzmin, M. Punkkinen, P. Laukkanen, K. Kokko, R. Félix, M. Lastusaari, V. Polojärvi, J. Lyytikäinen, A. Tukiainen, and M. Guina, Decreasing defect-state density of $Al_2O_3/Ga_xIn_{1-x}As$ device interfaces with InO_x structures. Adv. Mater. Int. **4**, 1700722 (2017).

[65] J. Mäkelä, Z. Jahanshah Rad, J.-P. Lehtiö, M. Tuominen, J. Dahl, M. Kuzmin, M. P. J. Punkkinen, P. Laukkanen, and K. Kokko: Crystalline oxide phases on InSb(111)B revealed with scanning tunneling microscopy and spectroscopy. Sci. Rep. **8**, 14382 (2018).

[66] M. Tuominen, J. Mäkelä, M. Yasir, J. Dahl, S. Granroth, J.-P. Lehtiö, R. Félix, P. Laukkanen, M. Kuzmin, M. Laitinen, M. P. J. Punkkinen, H.-P. Hedman, R. Punkkinen, V. Polojärvi, J. Lyytikäinen, A. Tukiainen, M. Guina, and K. Kokko, Oxidation-induced changes in the ALD-Al_2O_3/InAs(100) interface and control of the changes for device processing. ACS Appl. Mat. Interf. **10**, 44932 (2018).

[67] J. Mäkelä, PhD thesis: Investigation and suppression of semiconductor-oxide related defect states: From surface science to device tests. Univeristy of Turku, Finland (2019).

[68] W.-E Wang, M. S. Rodder, R. M. Wallace, and X. Qin, Method of forming crystalline oxides on III-V Materials. US Patent 10475930B2 (2019).

[69] G. Hollinger, R. Skheyta-Kabbani, and M. Gendry, Oxides on GaAs and InAs surfaces: An x-ray-photoelectron-spectroscopy study of reference compounds and thin oxide layers. Phys. Rev. B **49**, 11159 (1994).

[70] W. M. Haynes, CRC Handbook of Chemistry and Physics. CRC Press (2012).

[71] H. H. Tompkins, Vacuum Technology: A beginning. AVS Monograph (2002).

[72] S. S. Li, Semiconductor Physical Electronics. Springer (2006).

[73] Fundamental Aspects of Silicon Oxidation, edited by Y. J. Chabal. Springer (2001).

[74] J. Robertson and R. M. Wallace, High-K Materials and Metal Gates for CMOS Applications. Mater. Sci. Eng. R **88**, 1 (2015).

[75] T. Wang, T.-E. Chang, and C. Huang, Interface trap induced thermionic and field emission current in off-state MOSFET's, IEEE Int. Electr. Dev. Meet. IEDM 161 (1994).

[76] D. M. Fleetwood, P. S. Winokur, R. A. Reber Jr., T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, Effects of oxide traps, interface traps, and ‘‘border traps’’ on metal-oxide-semiconductor devices. J. Appl. Phys. **73**, 5058 (1993).

[77] Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, A distributed model for border traps in Al_2O_3−InGaAs MOS devices. IEEE Electr. Dev. Lett. **32**, 485 (2011).

[78] A. Vais, H.-C. Lin, C. Dou, K. Martens, T. Ivanov, Q. Xie, F. Tang, M. Givens, J. Maes, N. Collaert, J.-P. Raskin, K. DeMeyer, and A. Thean, Temperature dependence of frequency dispersion in III–V metal-oxide-semiconductor C-V and the capture/emission process of border traps. Appl. Phys. Lett. **107**, 053504 (2015).

[79] R. T. Tung, The physics and chemistry of the Schottky barrier height. Appl. Phys. Rev. **1**, 011304 (2014).

[80] H. Lu, Y. Guo, H. Li, and J. Robertson, Modeling of surface gap state passivation and Fermi level de-pinning in solar cells. Appl. Phys. Lett. **114**, 222106 (2019).

[81] A. Agrawal, J. Lin, M. Barth, R. White, B. Zheng, S. Chopra, S. Gupta, K. Wang, J. Gelatos, S. E. ohney, and S. Datta, Fermi level depinning and contact resistivity reduction using a reduced titania interlayer in n-silicon metal-insulator-semiconductor ohmic contacts. Appl. Phys. Lett. **104**, 112101 (2014).

[82] T. G. Allen, J. Bullock, Q. Jeangros, C. Samundsett, Y. Wan, J. Cui, A. Hessler-Wyser, S. De Wolf, A. Javey, and A. Cuevas, A low resistance calcium/reduced titania passivated contact for high efficiency crystalline silicon solar cells. Adv. Energy Mat. **7**, 1602606 (2017).

[83] H.-P. Komsa and A. Pasquarello, Dangling bond charge transition levels in AlAs, GaAs, and InAs, Appl. Phys. Lett. **97**, 191901 (2010).

[84] L. Lin and J. Robertson, Defect states at III-V semiconductor oxide interfaces. Appl. Phys. Lett. **98**, 082903 (2011).

[85] W. Wang, K. Xiong, R. M. Wallace, and K. Cho, Impact of interfacial oxygen content on bonding, stability, band offsets, and interface states of GaAs:HfO_2 interfaces. J. Phys. Chem. C **114**, 22610 (2010).

[86] M. Passlack, R. Droopad, P. Fejes, and L. Wang, Electrical properties of Ga_2O_3/GaAs interfaces and GdGaO dielectrics in GaAs-based MOSFETs. IEEE Electr. Dev. Lett. **30**, 1 (2009).

[87] G. Hollinger and E. Bergignat, On the nature of oxides on InP surfaces. J. Vac. Sci. Techn. A **3**, 2082 (1985).

[88] G. Hollinger, G. Hughes, F. J. Himpsel J. L. Jordan, J. F. Morar, and F. Houzay, Early stages in the formation of the oxide-InP(110) interface. Surf. Sci. **168**, 617 (1986).

[89] E. Bergignat, G. Hollinger, and Y. Robach, A study of thermal oxide-InP interaces. Surf. Sci. **189–190**, 353 (1987).

[90] Y. Chen, H. Liang, X. Xia, Renshengshen, Y. Liu, Y. Luo, and G. Du, Effect of growth pressure on the characteristics of β-Ga2O3 films grown on GaAs(100) substrates by MOCVD method. Appl. Surf. Sci. **325**, 258 (2015).

[91] A. Ourmazd, D. W. Taylor, J. A. Rentschler, and J. Bevk, $Si \rightarrow SiO_2$ transformation: Interfacial structure and mechanism. Phys. Rev. Lett. **59**, 213 (1987).

[92] J. Bevk, L. C. Feldman, T. P. Pearsall, G.P. Schwartz, and A. Ourmazd, Strain effects in epitaxial monolayer structures: Si/Ge and Si/SiO_2 systems. Mat. Sci. Eng. B **6**, 159 (1990).

[93] A. Munkholm, S. Brennan, F. Comin, and L. Ortega, Observation of a distributed epitaxial oxide in thermally grown SiO_2 on Si(001). Phys. Rev. Lett. **75**, 4254 (1995).

[94] V. V. Afanas'ev, A. Stesmans, and M. E. Twigg, Epitaxial growth of SiO_2 produced in silicon by oxygen ion implantation. Phys. Rev. Lett. **77**, 4206 (1996).

[95] M. Kuzmin, J.-P. Lehtiö, J. Mäkelä, M. Yasir, Z. Jahanshah Rad, E. Vuorinen, A. Lahti, M. Punkkinen, P. Laukkanen, K. Kokko, H.-P. Hedman, R. Punkkinen, M. Lastusaari, P. Repo, and H. Savin, Observation of Crystalline Oxidized Silicon Phase. Adv. Mat. Interf. **6**, 1802033 (2019).

[96] X.-Y. Zhang, C.-H. Hsu, S.-Y. Lien, W.-Y. Wu, S.-L. Ou, S.-Y. Chen, W. Huang, W.-Z. Zhu, F.-B. Xiong, and S. Zhang, Temperature-dependent HfO_2/Si interface structural evolution and its mechanism. Nanosc. Res. Lett. **14**, 83 (2019).

[97] C. Heyn and D. E. Jesson, Congruent evaporation temperature of molecular beam epitaxy grown GaAs (001) determined by local droplet etching. Appl. Phys. Lett. **107**, 161601 (2015).

[98] Z. Y. Zhou, C. X. Zheng, W. X. Tang, D. E. Jesson, and J. Tersoff, Congruent evaporation temperature of GaAs(001) controlled by As flux. Appl. Phys. Lett. **97**, 121912 (2010).

[99] G. J. Davies, R. Heckingbottom, H. Ohno, C. E. C. Wood, and A. R. Calawa, Arsenic stabilization of InP substrates for growth of $Ga_xIn_{1-x}As$ layers by molecular beam epitaxy. Appl. Phys. Lett. **37**, 290 (1980).

[100] B. J. O'Sullivan, P. K. Hurley, E. O'Connor, M. Modreanu, H. Roussel, C. Jimenez, C. Dubourdieu, M. Audier, and J. P. Senateur, Electrical evaluation of defects at the Si (100)/HfO_2 interface. J. Electrochem. Soc. **151**, G493 (2004).

[101] É. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanasev, and P. K. Hurley, Temperature and frequency

dependent electrical characterization of $HfO_2/In_xGa_{1-x}As$ interfaces using capacitance-voltage and conductance methods. Appl. Phys. Lett. **94**, 102902 (2009).

[102] G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces. Appl. Phys. Lett. **95**, 202109 (2009).

[103] Y. Hwang, R. Engel-Herbert, N. G. Rudawski, and S. Stemmer, Effect of postdeposition anneals on the Fermi level response of $HfO_2/In_{0.53}Ga_{0.47}As$ gate stacks. J. Appl. Phys. **108**, 034111 (2010).

[104] Y Hwang, R. Engel-Herbert, N. Rudawski, and S. Stemmer, Fermi-level unpinning of $HfO_2/In_{0.53}Ga_{0.47}As$ gate stack using hydrogen anneals. ECS Trans. **33** 117 (2010).

[105] B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle, and P. C. McIntyre, Origin and passivation of fixed charge in atomic layer deposited aluminum oxide gate insulators on chemically treated InGaAs substrates. Appl. Phys. Lett. **96**, 152908 (2010).

[106] R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S. H. Kim, T. Hoshii, T. Yasuda, W. Jevasuwan, T. Maeda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, 1-nm-capacitance-equivalent-thickness HfO_2/Al_2O_3/InGaAs metal-oxide-semiconductor structure with low interface trap density and low gate leakage current density. Appl. Phys. Lett. **100**, 132906 (2012).

[107] J. Massies, J. Chaplart, M. Laviron, and N. T. Linh, Monocrystalline aluminium ohmic contact to n-GaAs by H_2S adsorption. Appl. Phys. Lett. **38**, 693 (1981).

[108] E. Yablonovitch, C. J. Sandroff, R. Bhat, and T. Gmitter, Nearly ideal electronic properties of sulfide coated GaAs surfaces. Appl. Phys. Lett. **51**, 439 (1987).

[109] G. Eftekhari, Electrical properties of sulfur-passivated III–V compound devices. Vacuum **67**, 81 (2002).

[110] B. Brennan, M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, G. Hughes, and R. M. Wallace, Optimisation of the ammonium sulphide $(NH_4)_2S$ passivation process on $In_{0.53}Ga_{0.47}As$. Appl. Surf. Sci. **257**, 4028 (2011).

[111] E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley. A systematic study of $(NH_4)_2S$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $Al_2O_3/In_{0.53}Ga_{0.47}As$/InP system for n-type and p-type $In_{0.53}Ga_{0.47}As$ epitaxial layers. J. Appl. Phys. **109**, 024101 (2011).

[112] B. Brennan, D. M. Zhernokletov, H. Dong, C. L. Hinkle, J. Kim, and R. M. Wallace, In situ surface pre-treatment study of GaAs and $In_{0.53}Ga_{0.47}As$. Appl. Phys. Lett. **100**, 151603 (2012).

[113] W. Wang, K. Xiong, R. M. Wallace, and K. Cho, First-principles study of initial growth of Ga_XO layer on GaAs-β2(2×4) surface and interface passivation by F. J. Appl. Phys. **110**, 103714 (2011).

[114] A. Lahti, H. Levämäki, J. Mäkelä, M. Tuominen, M. Yasir, J. Dahl, M. Kuzmin, P. Laukkanen, K. Kokko, and M. P. J. Punkkinen, Electronic structure and relative stability of the coherent and semi-coherent HfO_2/III-V interfaces. Appl. Surf. Sci. **427**, 243 (2018).

[115] M. Passlack, E. F. Schubert, W. S. Hobson, M. Hong, N. Moriya, S. N. G. Chu, K. Konstadinidis, J. P. Mannaerts, M. L. Schnoes, and G. J. Zydzik, Ga_2O_3 films for electronic and optoelectronic applications. J. Appl. Phys. **77**, 686 (1995).

[116] Z. Yu, C. D. Overgaard, and R. Droopad, M. Passlack, and J. K. Abrokwah, Growth and physical properties of Ga_2O_3 thin films on GaAs(001) substrate by molecular-beam epitaxy. Appl. Phys. Lett. **82**, 2978 (2003).

[117] M. Holland, C. R. Stanley, W. Reid, R. J. W. Hill, D. A. J. Moran, I. Thayne, G. W. Paterson, and A. R. Long, Ga_2O_3 grown on GaAs by molecular beam epitaxy for metal oxide semiconductor field effect transistors. J. Vac. Sci. Techn. B **25**, 1706 (2007).

[118] G. W. Paterson, J. A. Wilson, D. Moran, R. Hill, A. R. Long, I. Thayne, M. Passlack, and R. Droopad. Gallium oxide (Ga_2O_3) on gallium arsenide-A low defect, high-k system for future devices. Mat. Sci. Engineer. B **135**, 277 (2006).

[119] M. J. Guittet, J. P. Crocombette, and M. Gautier-Soyer, Bonding and XPS chemical shifts in $ZrSiO_4$ versus SiO_2 and ZrO_2: Charge transfer and electrostatic effects. Phys. Rev. B **63** 125117 (2001).

[120] O. E. Tereshchenko, S. I. Chikichev, and A. S. Terekhov, Atomic structure and electronic properties of HCl–isopropanol treated and vacuum annealed GaAs(100) surface. Appl. Surf. Sci. **142**, 75 (1999).

[121] P. Laukkanen, M. Kuzmin, R. E. Perälä, R.-L. Vaara, and I. J. Väyrynen, Scanning tunneling microscopy study of GaAs(100) surface prepared by HCl-isopropanol treatment. Appl. Surf. Sci. **206**, 2 (2003).

[122] J. Mäkelä, M. Tuominen, T. Nieminen, M. Yasir, M. Kuzmin, J. Dahl, M. P. J. Punkkinen, P. Laukkanen, K. Kokko, J. R. Osiecki, K. Schulte, M. Lastusaari, H. Huhtinen, and P. Paturi, Comparison of chemical, electronic, and optical properties of Mg-doped $Al_{0.5}Ga_{0.5}N$. J. Phys. Chem. C **120**, 28591 (2016).

[123] M. D. Pashley, K. W. Haberern, W. Friday, J. M. Woodall, and P. D. Kirchner, Structure of GaAs(001) (2×4)−c(2×8) determined by scanning tunneling microscopy. Phys. Rev. Lett. **60**, 2176 (1988).

[124] D. K. Biegelsen, R. D. Bringans, J. E. Northrup, and L.-E. Swartz, Surface reconstructions of GaAs(100) observed by scanning tunneling microscopy. Phys. Rev. B **41**, 5701 (1990).

[125] J. E. Northrup and S. Froyen, Structure of GaAs(001) surfaces: The role of electrostatic interactions. Phys. Rev. B **50**, 2015 (1994).

[126] T. Hashizume, Q.-K. Xue, J. Zhou, A. Ichimiya, and T. Sakurai, Structures of As-rich GaAs(001)-(2×4) reconstructions. Phys. Rev. Lett. **73**, 2208 (1995).

[127] H. Yamaguchi and Y. Horikoshi, Surface structure transitions on InAs and GaAs (001) surfaces. Phys. Rev. B **51**, 9836 (1995).

[128] W. G. Schmidt and F. Bechstedt, Geometry and electronic structure of GaAs(001)(2×4) reconstructions. Phys. Rev. B **54**, 16742 (1996).

[129] W. G. Schmidt, S. Mirbt, and F. Bechstedt, Surface phase diagram of (2×4) and (4×2) reconstructions of GaAs(001). Phys. Rev. B **62**, 8087 (2000).

[130] M. Göthelid, Y. Garreau, M. Sauvage-Simkin, R. Pinchaux, A. Cricenti, and G. Le Lay, Atomic structure of the As-rich InAs(100) β2(2×4) surface, Phys. Rev. B **59**, 15285 (1999).

[131] C. Ratsch, W. Barvosa-Carter, F. Grosse, J. H. G. Owen, and J. J. Zinck, Surface reconstructions for InAs(001) studied with density-functional theory and STM. Phys. Rev. B **62**, R7719 (2000).

[132] R. H. Miwa and G. P. Srivastava, Structure and electronic states of InAs(001)−(2×4) surfaces. Phys. Rev. B **62**, 15778 (2000).

[133] P. Laukkanen, M. Kuzmin, R.E. Perälä, M. Ahola, S. Mattila, I. J. Väyrynen, J. Sadowski, J. Konttinen, T. Jouhti, C. Peng, M. Saarinen, and M. Pessa: Electronic and structural properties of GaAs(100)(2×4) and InAs(100)(2×4) surfaces studied by core-level photoemission and scanning tunneling microscopy. Phys. Rev. B **72**, 045321 (2005).

[134] K. Seino, W. G. Schmidt, and A. Ohtake, Ga-rich GaAs(001) surface from ab initio calculations: Atomic structure of the (4×6) and (6×6) reconstructions. Phys. Rev. B **73**, 035317 (2006).

[135] S.-H. Lee, W. Moritz and M. Scheffler, GaAs(001) surface under conditions of low As pressure: evidence for a novel surface geometry. Phys. Rev. Lett. **85**, 3890 (2000).

[136] C. Kumpf, L. D. Marks, D. Ellis, D. Smilgies, E. Landemark, M. Nielsen, R. Feidenhans'l, J. Zegenhagen, O. Bunk, J. H. Zeysing, Y. Su, and R. L. Johnson, Subsurface dimerization in III-V semiconductor (001) surfaces. Phys. Rev. Lett. **86**, 3586 (2001).

[137] C. Kumpf, D. Smilgies, E. Landemark, M. Nielsen, R. Feidenhans’l, O. Bunk, J. H. Zeysing, Y. Su, R. L. Johnson, L. Cao, J. Zegenhagen, B. O. Fimland, L. D. Marks, and D. Ellis, Structure of metal-rich (001) surfaces of III-V compound semiconductors. Phys. Rev. B **64**, 075307 (2001).

[138] P. Laukkanen, M. P. J. Punkkinen, M. Ahola-Tuomi, J. Lång, K. Schulte, A. Pietzsch, M. Kuzmin, J. Sadowski, J. Adell, R. E. Perälä, M. Ropo, K. Kokko, L. Vitos, B. Johansson, M. Pessa, and I. J.

Väyrynen: Core-level shifts of the c(8×2)-reconstructed InAs(100) and InSb(100) surfaces. J. Electr. Spectr. Rel. Phenom. **177**, 52 (2011).

[139] W. G. Schmidt, F. Bechstedt, N. Esser, M. Pristovsek, Ch. Schultz, and W. Richter, Atomic structure of InP(001)-(2×4): A dimer reconstruction. Phys. Rev. B **57**, 14596 (1998).

[140] S. Mirbt, N. Moll, K. Cho, and J. D. Joannopoulos, Cation-rich (100) surface reconstructions of InP and GaP. Phys. Rev. B **60**, 13283 (1999).

[141] K. Lüdge, P. Vogt, O. Pulci, N. Esser, F. Bechstedt, and W. Richter, Clarification of the GaP(001)(2×4) Ga-rich reconstruction by scanning tunneling microscopy and ab initio theory. Phys. Rev. B **62**, R11046 (2000).

[142] G. E. Franklin, D. H. Rich, A. Samsavar, E. S. Hirschorn, F. M. Leibsle, T. Miller, and T.-C. Chiang, Photoemission and scanning-tunneling-microscopy study of GaSb(100). Phys. Rev. B **41**, 12619 (1990).

[143] M. T. Sieger, T. Miller, and T.-C. Chiang, Reflection high-energy electron diffraction and photoemission study of GaSb(100) reconstructions. Phys. Rev. B **52**, 8256 (1995).

[144] U. Resch-Esser, N. Esser, B. Brar, and H. Kroemer, Microscopic structure of GaSb(001)c(2×6) surfaces prepared by Sb decapping of MBE-grown samples. Phys. Rev. B **55**, 15401 (1997).

[145] W. Barvosa-Carter, A. S. Bracker, J. C. Culbertson, B. Z. Nosho, B. V. Shanabrook, L. J. Whitman, Hanchul Kim, N. A. Modine, and E. Kaxiras, Structure of III-Sb(001) growth surfaces: The role of heterodimers. Phys. Rev. Lett. **84**, 4649 (2000).

[146] T. Nakada and T. Osaka, T. Sb trimer structure of the InSb(111)B-(2 × 2) surface as determined by transmission electron diffraction. Phys. Rev. Lett. **67**, 2834 (1991).

[147] A. J. Noreika, M. H. Francombe, and C. E. C. Wood, Growth of Sb and InSb by molecular beam epitaxy. J. Appl. Phys. **52**, 7416 (1981).

[148] K. Oe, S. Ando, and K. Sugiyama, RHEED study of InSb films grown by molecular beam epitaxy. Jpn. J. Appl. Phys. **19**, L417 (1980).

[149] K. E. Johnson, P.K. Wu, M. Sander, and T. Engel, The mesoscopic and microscopic structural consequences from decomposition and desorption of ultrathin oxide layers on Si(100) studied by scanning tunneling microscopy. Surf. Sci. **290**, 213 (1993).

[150] Y. Wei, R. M. Wallace, and A. C. Seabaugh, Void formation on ultrathin thermal silicon oxide films on the Si(100) surface. Appl. Phys. Lett. **69**, 1270 (1996).

[151] C. W. Wilmsen and S. Szpak, MOS processing for III–V compound semiconductors: Overview and bibliography, Thin Sol. Films **46**, 17 (1977).

[152] R. M. Wallace, In-situ studies of interfacial bonding of high-k dielectrics for CMOS beyond 22nm. Electroch. Soc. Transact. **16**, 255 (2008).

[153] A. Zangwill, Physics at Surfaces. Cambridge University Press (1988).

[154] R. Wiesendanger, Scanning Probe Microscopy and Spectroscopy Methods and Applications. Cambridge University Press (1994).

[155] F. Bechstedt, Principles of Surface Physics. Springer (2003).

[156] R. M. Wallace, High-k dielectrics: A perspective on applications from silicon to 2D materials, ECS Transact. **80**, 17 (2017).

[157] C. Nordling, E. Sokolowski, and K. Siegbahn, Precision method for obtaining absolute values of atomic binding energies. Phys. Rev. **105**, 1676 (1957).

[158] K. Siegbahn, D. Hammond, H. Fellner-Feldegg, and E. F. Barnett, Electron spectroscopy with monochromatized x-rays. Science, **176**, 245 (1972).

[159] S. Huefner, Photoelectron Spectroscopy. Springer Verlag (1995).

[160] N. Mårtensson, E. Sokolowski, and S. Svensson, 50 years anniversary of the discovery of the core level chemical shifts. The early years of photoelectron spectroscopy. J. Electr. Spectr. Rel. Phenom. **193**, 27 (2014).

[161] A. G. Shard, Detection limits in XPS for more than 6000 binary systems using Al and Mg Kα X-rays. Surf. Int. Anal. **46**, 175 (2014).

[162] L. Walsh, PhD thesis: Applications of hard x-ray photoelectron spectroscopy in semiconductor materials characterization. Dublin City University, Ireland (2014).

[163] C. J. Powell and A. Jablonski, Measurement of silicon dioxide film thicknesses by X-ray photoelectron spectroscopy. AIP Confer. Proc. **550**, 591 (2001).

[164] D. A. Cole, J. R. Shallenberger, S. W. Novak, and R. L. Moore, M. J. Edgell, S. P. Smith, C. J. Hitzman, J. F. Kirchhoff, and E. Principe, W. Nieveen and F. K. Huang, S. Biswas, R. J. Bleiler, and K. Jones, SiO_2 thickness determination by x-ray photoelectron spectroscopy, Auger electron spectroscopy, secondary ion mass spectrometry, Rutherford backscattering, transmission electron microscopy, and ellipsometry. J. Vac. Sci. Technol. B **18**, 440 (2000).

[165] E. Holmström, W. Olovsson, I. A. Abrikosov, A. M. N. Niklasson, B. Johansson, M. Gorgoi, O. Karis, S. Svensson, F. Schäfers, W. Braun, G. Öhrwall, G. Andersson, M. Marcellini, W. Eberhardt: Sample preserving deep interface characterization technique. Phys. Rev. Lett. **97**, 266106 (2006).

[166] W. F. Egelhoff, Core-level binding-energy shifts at surfaces and in solids. Surf. Sci. Rep. **6**, 253 (1987).

[167] E. Pehlke and M. Scheffler, Evidence for site-sensitive screening of core holes at the Si and Ge (001) surface. Phys. Rev. Lett. **71**, 2338 (1993).

[168] M. M. B. Holl, S. Lee, and F. R. McFeely, Core-level photoemission and the structure of the Si/SiO_2 interface: A reappraisal. Appl. Phys. Lett. **65**, 1097 (1994).

[169] A. Pasquarello, M. S. Hybertsen, and R. Car, Si 2p core-level shifts at the $Si(001)$-SiO_2 interface: A first-principles study. Phys. Rev. Lett. **74**, 1024 (1995).

[170] Yuhai Tu and J. Tersoff, Structure and energetics of the Si-SiO_2 interface. Phys. Rev. Lett. **84**, 4393 (2000).

[171] G. Miceli and A. Pasquarello, First principles study of As 2p core-level shifts at GaAs/Al_2O_3 interfaces, Appl. Phys. Lett. **102**, 201607 (2013).

[172] J. Mäkelä, A. Lahti, M. Tuominen, M. Yasir, M. Kuzmin, P. Laukkanen, K. Kokko, M. P. J. Punkkinen, H. Dong, B. Brennan, and R. M. Wallace, Unusual oxidation-induced core-level shifts at the HfO_2/InP interface. Sci. Rep. **9**, 1462 (2019).

[173] F. J. Himpsel, F. R. McFeely, A. Taleb-Ibrahimi, J. A. Yarmoff, and G. Hollinger, Microscopic structure of the SiO_2/Si interface. Phys. Rev. B **38**, 6084 (1988).

[174] M. B. Holl and F. R. McFeely, Si/SiO_2 interface: new structures and well-defined model systems. Phys. Rev. Lett. **71**, 2441 (1993).

[175] K. Z. Zhang, M. M. B. Holl, J. E. Bender, S. Lee, and F. R. McFeely, Si 2p core-level shifts at the Si(100)/SiO_2 interface: An experimental study. Phys. Rev. B **54**, 7686 (1996).

[176] J. W. Keister and J. E. Rowe, J. J. Kolodziej, H. Niimi, H.-S. Tao, T. E. Madey, and G. Lucovsky, Structure of ultrathin SiO_2/Si(111) interfaces studied by photoelectron spectroscopy. J. Vac. Sci. Technol. A **17**, 1250 (1999).

[177] D. B. Williams and C. B. Carter, Transmission Electron Microscopy: A Textbook for Materials Science. Springer (2009).

[178] A. Rosenauer, Transmission Electron Microscopy of Semiconductor Nanostructures: Analysis of Composition and Strain State. Springer (2003).

[179] D. J. Smith, H. W. Wu, S. Lu, and T. Aoki, Recent studies of oxide-semiconductor heterostructures using aberration-corrected scanning transmission electron microscopy. J. Mat. Res. **32**, 912 (2017).

[180] N. P. Dasgupta, J. Sun, C. Liu, S. Brittman, S. C. Andrews, J. Lim, H. Gao, R. Yan, and P. Yang, Semiconductor nanowires – synthesis, characterization, and applications. Adv. Mater. **26**, 2137 (2014).

[181] P. Longo, A. J. Craven, M. C. Holland, D. A. J. Moran, and I. G. Thayne, A nanoanalytical investigation of high-k dielectric gate stacks for GaAs based MOSFET devices. Microelectr. Engineer. **86**, 214 (2009).

[182] M. Holland, P. Longo, G. W. Paterson, W. Reid, A. R. Long, C. R. Stanley, A. J. Craven, I. Thayne, and R. Gregory, Characteristics of GdGaO grown by MBE. Microelectr. Engineer. **86**, 244 (2009).

[183] V. Chobpattana, T. E. Mates, J. Y. Zhang, and S. Stemmer, Scaled ZrO_2 dielectrics for $In_{0.53}Ga_{0.47}As$ gate stacks with low interface trap densities. Appl. Phys. Lett. **104**, 182912 (2014).

[184] K. K. Smith, Photoluminescence of semiconductor materials. Thin Sol. Films **84**, 171 (1981).

[185] D. E. Aspnes, Recombination at semiconductor surfaces and interfaces. Surf. Sci. **132**, 406 (1983).

[186] T. Saitoh, H. Iwadate, and H. Hasegawa, In situ surface state spectroscopy by photoluminescence and surface current transport for compound semiconductors. Jpn. J. Appl. Phys. **30**, 12B (1991).

[187] M. Passlack, M. Hong, E. F. Schubert, J. R. Kwo, J. P. Mannaerts, S. N. G. Chu, N. Moriya, and F. A. Thiel, In situ fabricated Ga_2O_3–GaAs structures with low interface recombination velocity. Appl. Phys. Lett. **66**, 625 (1995).

[188] M. Passlack, Methodology for development of high-k stacked gate dielectrics on III-V semiconductors, in the book of Materials Fundamentals of Gate Dielectrics, edited by A. A. Demkov and A. Navrotsky. 403-467 (2005).

[189] M. Passlack, R. Droopad, Z. Yu, N. Medendorp, D. Braddock, X. W. Wang, T. P. Ma, and T. Buyuklimanli, Screening of oxide/GaAs interfaces for MOSFET applications. IEEE Electr. Dev. Lett. **29,** 1181 (2008).

[190] L. Bergman and J. L. McHale, Handbook of Luminescent Semiconductor Materials, CRS Press Taylor Francis (2012).

[191] L. Wang, Doctoral thesis: Design of scaled electronic devices based on III-V materials. University of California, San Diego (2009).

[192] E. H. Nicollian and J. R. Brews, MOS Physics and Technology. Wiley (1982).

[193] C. L. Hinkle, A. M. Sonnet, and E. M. Vogel, S. McDonnell and G. J. Hughes, Frequency dispersion reduction and bond conversion on n-type GaAs by in situ surface oxide removal and passivation. Appl. Phys. Lett. **91**, 163512 (2007).

[194] R. Engel-Herbert, Y. Hwang, and S. Stemmer, Comparison of methods to quantify interface trap densities at dielectric/IIIV semiconductor interfaces. J. Appl. Phys. **108**, 124101 (2010).

[195] B. Yao, Z. B. Fang, Y. Y. Zhu, T. Ji, and G. He, A model for the frequency dispersion of the high-k metal-oxide-semiconductor capacitance in accumulation. Appl. Phys. Lett. **100**, 222903 (2012).

[196] S. Stemmer, V. Chobpattana, and S. Rajan, Frequency dispersion in III-V metal-oxide-semiconductor capacitors. Appl. Phys. Lett. **100**, 233510 (2012).

[197] R. V. Galatage, D. M. Zhernokletov, H. Dong, B. Brennan, C. L. Hinkle, R. M. Wallace, and E. M. Vogel. Accumulation capacitance frequency dispersion of III-V metal-insulator-semiconductor devices due to disorder induced gap states. J. Appl. Phys. **116**, 014504 (2014).

[198] I. Krylov, D. Ritter, and M. Eizenberg, The physical origin of dispersion in accumulation in InGaAs based metal oxide semiconductor gate stacks. J. Appl. Phys. **117**, 174501 (2015).

[199] J. Lin, S. Monaghan K. Cherkaoui, I. Povey, É. O'Connor, B. Sheehan, P. Hurley, A study of capacitance–voltage hysteresis in the HfO_2/InGaAs metal-oxide-semiconductor system. Microelectr. Engineer. **147**, 273 (2015).

[200] K. Tang, A. C. Meng, R. Droopad, and P. C. McIntyre, Temperature dependent border trap response produced by a defective interfacial oxide layer in Al_2O_3/InGaAs gate stacks. ACS Appl. Mater. Interfac. **8**, 30601 (2016).

[201] A. Vais, J. Franco, K. Martens, D. Lin, S. Sioncke, V. Putcha, L. Nyns, J. Maes, Q. Xie, M. Givens, F. Tang, X. Jiang, A. Mocuta, N. Collaert, A. Thean, and K. De Meyer. A new quality metric for III–

V/high-k MOS gate stacks based on the frequency dispersion of accumulation capacitance and the CET. IEEE Electr. Dev. Lett. **38**, 318 (2017).

[202] K. Tang, F. R. Palumbo, L. Zhang, R. Droopad, and P. C. McIntyre, Interface defect hydrogen depassivation and capacitance−voltage hysteresis of Al_2O_3/InGaAs gate stacks. ACS Appl. Mater. Interf. **9**, 7819 (2017).

[203] E. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, Border traps in Al_2O_3/$In_{0.53}Ga_{0.47}As$ (100) gate stacks and their passivation by hydrogen anneals. Appl. Phys. Lett. **96**, 012906 (2010).

[204] E. Caruso, J. Lin, S. Monaghan, K. Cherkaoui, F. Gity, P. Palestri, D. Esseni, L. Selmi, and P. K. Hurley, The role of oxide traps aligned with the semiconductor energy gap in MOS systems. IEEE Trans. Electr. Dev. **67**, 4372 (2020).

[205] S.-W. Wang, T. Vasen, G. Doornbos, R. Oxland, S.-W. Chang, X. Li, R. Contreras-Guerrero, M. Holland, C.-H. Wang, M. Edirisooriya, J. S. Rojas-Ramirez, P. Ramvall, S. Thoms, D. S. Macintyre, G. Vellianitis, G. C. H. Hsieh, Y.-S. Chang, K. M. Yin, Y.-C. Yeo, C. H. Diaz, R. Droopad, I. G. Thayne, and M. Passlack, Field-effect mobility of InAs surface channel nMOSFET with low D_{it} scaled gate-stack. IEEE Trans. Electr. Dev. **62**, 2429 (2015).

[206] C. H. Wang, G. Doornbos, G. Astromskas, G. Vellianitis, R. Oxland, M. C. Holland, M. L. Huang, C. H. Lin, C. H. Hsieh, Y. S. Chang, T. L. Lee, Y. Y. Chen, P. Ramvall, E. Lind, W. C. Hsu, L.-E. Wernersson, R. Droopad, M. Passlack, and C. H. Diaz, High-k dielectrics on (100) and (110) n-InAs: Physical and electrical characterizations. AIP Adv. **4**, 047108 (2014).

[207] M. Scarrozza, G. Pourtois, M. Houssa, M. Caymax, A. Stesmans, M. Meuris, and M. M. Heyns, A first-principles study of the structural and electronic properties of III–V/thermal oxide interfaces. Microelectr. Engineer. **86**, 1747 (2009).

[208] P. Laukkanen, M. P. J. Punkkinen, J. Lång, M. Tuominen, M. Kuzmin, V. Tuominen, J. Dahl, J. Adell, J. Sadowski, J. Kanski, V. Polojärvi, J. Pakarinen, K. Kokko, M. Guina, M. Pessa, and I. J. Väyrynen:

Ultrathin (1×2)-Sn layer on GaAs(100) and InAs(100) substrates: A catalyst for removal of amorphous surface oxides. Appl. Phys. Lett. **98**, 231908 (2011).

[209] P. Laukkanen, J. J. K. Lång, M. P. J. Punkkinen, M. Tuominen, J. Dahl, V. Tuominen, K. Kokko, M. Kuzmin, V. Polojärvi, J. Salmi, V.-M. Korpijärvi, A. Aho, A. Tukiainen, M. Guina, H.-P. Hedman, and R. Punkkinen: Synthesis and Characterization of Layered Tin Monoxide Thin Films with Monocrystalline Structure on III-V Compound Semiconductor. Adv. Mat. Interf. **1** (2014).

[210] J. J. K. Lång, M. P. J. Punkkinen, P. Laukkanen, M. Kuzmin, V. Tuominen, M. Pessa, M. Guina, I. J. Väyrynen, K. Kokko, B. Johansson, and L. Vitos: Ab initio and scanning tunneling microscopy study of indium-terminated GaAs(100) surface: An indium-induced surface reconstruction change in the c(8×2) structure. Phys. Rev. B **81**, 245305 (2010).

[211] C. L. Hinkle, M. Milojevic, B. Brennan, A. M. Sonnet, F. S. Aguirre-Tostado, G. J. Hughes, E. M. Vogel, and R. M. Wallace, Detection of Ga suboxides and their impact on III-V passivation and Fermi-level pinning. Appl. Phys. Lett. **94**, 162101 (2009).

[212] J. Dahl, V. Polojärvi, J. Salmi, P. Laukkanen, and M. Guina, Properties of the SiO_2- and SiN_x-capped GaAs(100) surfaces of GaInAsN/GaAs quantum-well heterostructures studied by photoelectron spectroscopy and photoluminescence. Appl. Phys. Lett. **99**, 102105 (2011).

[213] J. Mäkelä, M. Tuominen, M. Yasir, M. Kuzmin, J. Dahl, M.P.J. Punkkinen, P. Laukkanen, and K. Kokko, Thermally assisted oxidation of GaSb(100) and the effect of initial oxide phases. Appl. Surf. Sci. **369**, 520 (2016).

[214] M. S. Miao, J. R. Weber, and C. G. Van de Walle, Oxidation and the origin of the two-dimensional electron gas in AlGaN/GaN heterostructures. J. Appl. Phys. **107**, 123713 (2010).

[215] X. Qin, A. Lucero, A. Azcatl, J. Kim, and R. M. Wallace, In situ x-ray photoelectron spectroscopy and capacitance voltage characterization of plasma treatments for Al_2O_3/AlGaN/GaN stacks. Appl. Phys. Lett. **105**, 011602 (2014).

[216] Monolithic Microwave IC (MMIC) Market analysis in 2019 by MarketsandMarkets™ INC, https://www.marketsandmarkets.com/PressReleases/monolithic-microwave-ic.asp.

[217] F. Roccaforte, G. Greco, P. Fiorenza, and F. Iucolan, An overview of normally-off GaN-based high electron mobility transistors, Materials **12**, 1599 (2019).

[218] D. J. Cheney, E. A. Douglas, L. Liu, C.-F. Lo, B. P. Gila, F. Ren, and S. J. Pearton, Degradation mechanisms for GaN and GaAs high speed transistors, Materials **5**, 2498 (2012).

[219] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, GaN metal-oxide-semiconductor highelectron-mobility-transistor with atomic layer deposited as gate dielectric. Appl. Phys. Lett. **86**, 063501 (2005).

[220] M. Hua, J. Wei, G. Tang, Z. Zhang, Q. Qian, X. Cai, N. Wang, and K. J. Chen, Normally-off LPCVD-SiN_x/GaN MIS-FET with crystalline oxidation interlayer. IEEE Electr. Dev. Lett. **38**, 929 (2017).

[221] S. Liu, S. Yang, Z. Tang, Q. Jiang, C. Liu, M. Wang, B. Shen, and K. J. Chen, Interface/border trap characterization of Al_2O_3/AlN/GaN metal-oxide-semiconductor structures with an AlN interfacial layer. Appl. Phys. Lett. **106**, 051605 (2015).

[222] G. Greco, P. Fiorenza, P. Lucolano, A. Severino, F. Giannazzo, and F. Roccaforte, Conduction mechanisms at interface of AlN/SiN dielectric stacks with AlGaN/GaN heterostructures for normally-off high electron mobility transistors: correlating device behavior with nanoscale interfaces properties. ACS Appl. Mater. Int. **9**, 35383 (2017).

[223] X. Liu, X. Wang, Y. Zhang, K. Wei, Y. Zheng, X. Kang, H. Jiang, J. Li, W. Wang, X. Wu, X. Wang, and S. Huang, Insight into the near-conduction band states at the crystallized interface between GaN and SiN_x grown by low-pressure chemical vapor deposition. ACS Appl. Mater. Int. **10**, 21721 (2018).

[224] T. Hashizume, K. Nishiguchi, S. Kaneki, J. Kuzmik, and Z. Yatabe, State of the art on gate insulation and surface passivation for GaN-based power HEMTs. Mat. Sci. Semic. Proc. **78**, 85 (2018).

[225] Y. G. Xie, S. Kasai, H. Takahashi, C. Jiang, and H. Hasegawa, A novel InGaAs/InAlAs insulated gate pseudomorphic HEMT with a silicon interface control layer showing high DC- and RF-performance. IEEE Electr. Dev. Lett. **22**, 312 (2001).

[226] D.-H. Kim and J. A. Del Alamo, Lateral and vertical scaling of $In_{0.7}Ga_{0.3}As$ HEMTs for post-Si-CMOS logic applications. IEEE Trans. Electr. Dev. **55**, 2546 (2008).

[227] H.-C. Chiu, Y.-C. Huang, C.-W. Chen, and L.-B. Chang, Electrical characteristics of passivated pseudomorphic HEMTs With $P_2S_5/(NH_4)_2S_X$ pretreatment. IEEE Trans. Electr. Dev. **55**, 721 (2008).

[228] M. Malmkvist, S. Wang, and J. Grahn, Epitaxial Optimization of 130-nm gate-length InGaAs/InAlAs/InP HEMTs for low-noise applications. IEEE Trans. Electr. Dev. **56**, 126 (2009).

[229] N. Kharche, G. Klimeck, D.-H. Kim, J. A. del Alamo, and M. Luisier, Performance analysis of ultra-scaled InAs HEMTs. IEEE Intern. Electr. Dev. Meet. (2009).

[230] K.-W. Lee, H.-C. Lin, F.-M. Lee, H.-K. Huang, and Y.-H. Wang, Improved microwave and noise performance of InAlAs/InGaAs metamorphic high-electron-mobility transistor with a liquid phase oxidized InGaAs gate without gate recess. Appl. Phys. Lett. **96**, 203506 (2010).

[231] T.-W. Kim, J.S. Kim, D.-K. Kim, S.H. Shin, W.-S. Park, S. Banerjee, and D.-H. Kim, High-frequency characteristics of L_g = 60 nm InGaAs MOS high-electron-mobility-transistor (MOS-HEMT) with Al_2O_3 gate insulator. Electr. Lett. **52**, 870 (2016).

[232] Y. Sun, E. W. Kiewra, J. P. de Souza, J. J. Bucchignano, K. E. Fogel, D. K. Sadana, and G. G. Shahidi, High-Performance $In_{0.7}Ga_{0.3}As$-Channel MOSFETs With High-κ Gate Dielectrics and α-Si Passivation. IEEE Electr. Dev. Lett. **30**, 5 (2009).

[233] M. Hermle, F. Feldmann, M. Bivour, J. C. Goldschmidt, and S. W. Glunz, Passivating contacts and tandem concepts: Approaches for the highest silicon-based solar cell efficiencies. Appl. Phys. Rev. **7**, 021305 (2020).

[234] A. Rogalski, Infrared detectors: status and trends, Prog. Quant. Electron. **27**, 59 (2003).

[235] A. K. Dutta and M. Saif Islam, Novel broadband photodetector for optical communication, Proc. of SPIE **6014**, 60140C-1 (2005).

[236] C. L. Chen, D.-R. Yost, J. M. Knecht, J. Wey, D. C. Chapman, D. C. Oakley, A. M. Soares, L. J. Mahoney, J. P. Donnelly, C. K. Chen, V. Suntharalingam, R. Berger, W. Hu, B. D. Wheeler, C. L. Keast, and D. C. Shaver, Wafer-scale 3D integration of InGaAs photodiode arrays with Si readout circuits by oxide bonding and through-oxide vias. Microel. Engin. **88**, 131 (2011).

[237] Yang, M. Shi, X. Shao, T. Li, X. Li, N. Tang, H. Gong, R. Liu, H. Tang, and Z.-J. Qiu, Low leakage of $In_{0.83}Ga_{0.17}As$ photodiode with Al_2O_3/SiN_x stacks. Infrared Phys. Techn. **71**, 272 (2015).

[238] M. Takenaka, Y. Kim, J. Han, J. Kang, Y. Ikku, Y. Cheng, J. Park, M. Yoshida, S. Takashima, and S. Takagi, Heterogeneous CMOS photonics based on SiGe/Ge and III–V semiconductors integrated on Si platform. IEEE J. Sel. Top. Quant. Electron. **23**, 8200713 (2017).

[239] A. Rogalski, P. Martyniuk, and M. Kopytko, InAs/GaSb type-II superlattice infrared detectors: Future prospect. Appl. Phys. Rev. **4**, 031304 (2017).

[240] A. T. Aho, J. Viheriälä, H. Virtanen, T. Uusitalo, and M. Guina, High-power 1.5-μm broad area laser diodes wavelength stabilized by surface gratings, IEEE Photon. Techn. Lett. **30**, 1870 (2018).

[241] B. J. Isaac, B. Song, S. Pinna, L. A. Coldren, and J. Klamkin, Indium phosphide photonic integrated circuit transceiver for FMCW LiDAR, IEEE J. Sel. Top. Quant. Electr. **25**, 8000107 (2019).

[242] F. Capasso and G. F. Williams, A proposed hydrogenation/nitridization passivation mechanism for GaAs and other III–V semiconductor devices, including InGaAs long wavelength photodetector. J. Electrochem. Soc. **129**, 4 (1982).

[243] J. G. Bauer and R. Trommer, Long-Term Operation of Planar InGaAs/InP p-i-n Photodiodes. IEEE Trans. Electr. Dev. **35**, 2349 (1988).

[244] M. R. Ravi, A. DasGupta, and N. DasGupta, Silicon nitride and polyimide capping layers on InGaAs/InP PIN photodetector after sulfur treatment, J. Cryst. Growth **268**, 359 (2004).

[245] K. Zhang, H. Tang, X. Wu, Y. Li, T Li, X. Li, and H. Gong, Effects of an anodic oxide passivation layer on mesa-type InGaAs (PIN) photodetectors. Semicond. Sci. Techn. **24**, 015008 (2008).

[246] A. Hood and M. Razeghia, On the performance and surface passivation of type II InAs⁄GaSb superlattice photodiodes for the very-long-wavelength infrared. Appl. Phys. Lett. **87**, 151113 (2005).

[247] R. T. Ley, J. M. Smith, M. S. Wong, T. Margalith, S. Nakamura, S. P. DenBaars, and M. J. Gordon, Revealing the importance of light extraction efficiency in InGaN/GaN microLEDs via chemical treatment and dielectric passivation. Appl. Phys. Lett. **116**, 251104 (2020).

[248] H. S. Wasisto, J. D. Prades, J. Gülink, and A. Waag, Beyond solid-state lighting: Miniaturization, hybrid integration, and applications of GaN nano- and micro-LEDs. Appl. Phys. Rev. **6**, 041315 (2019).

[249] Y. Boussadi, N. Rochat, J.-P. Barnes, B. B. Bakir, P. Ferrandis, B. Masenelli, C. Licitra, Characterization of micro-pixelated InGaP/AlGaInP quantum well structures. Proc. of SPIE **11302**, 1130221 (2020).

[250] M. Borselli, T. J. Johnson, C. P. Michael, M. D. Henry, and O. Painter, Surface encapsulation for low-loss silicon photonics. Appl. Phys. Lett. **91**, 131117 (2007).

[251] M. Borselli, T. J. Johnson, and O. Painter, Measuring the of surface chemistry in silicon microphotonic. Appl. Phys. Lett. **88**, 131114 (2006).

[252] J. Fan, P. Anantha, C. Y. Liu, M. Bergkvist, H. Wang, and C. S. Tan, Thermal characteristics of InP-Al_2O_3/Si low temperature heterogeneous direct bonding for photonic device integration. ECS J. Sol. State Sci. Techn. **2**, N169 (2013).

[253] N. Pan, C. Youtsey, D. S. McCallum, V. C. Elarde, and J. M. Dallesasse, High efficiency group III-V compound semiconductor solar cell with oxidized window layer. US patent, US 20120227798A1 (2012).

[254] T. J. Jenkins, Kehias, P. Parikh, J. Ibbetson, U. Mishra, D. Docter, M. Le, J. Pusl, and D. Widman, Ultrahigh efficiency obtained with GaAs-on-insulator MESFET technology. IEEE J. Solid-State Circ. **34**, 1239 (1999).

[255] T. Kagiyama, Y. Saito, K. Otobe, and S. Nakajima, Improvement of power performance in planar type AlGaAs/GaAs MESFET by substrate surface oxidation. Appl. Surf. Sci. **216**, 542 (2003).

[256] H. Hasegawa, M. Akazawa, K. Matsuzaki, H. Ishii, and H. Ohno, GaAs and $In_{0.53}Ga_{0.47}As$ MIS structures having an ultrathin pseudomorphic interface control layer of Si prepared by MBE. Jpn. J. Appl. Phys. **27**, 2265 (1988).

[257] S. Tiwari, S. L. Wright, and J. Batey, Unpinned GaAs MOS capacitors and transistors. Electr. Dev. Lett. **9**, 488 (1988).

[258] H. Hasegawa, MBE growth and applications of silicon interface control layers. Thin Sol. Films **367**, 58 (2000).

[259] I. Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J. C. Lee, Self-Aligned n- and p-channel GaAs MOSFETs on undoped and p-type substrates using HfO_2 and silicon interface passivation layer. IEEE Electr. Dev. Meet. (2006).

[260] J. Sandroff, R. N. Nottenburg, J.-C. Bischoff, and R. Bhat, Dramatic enhancement in the gain of a GaAs/AlGaAs heterostructure bipolar transistor by surface chemical passivation. Appl. Phys. Lett. **51**, 33 (1987).

[261] R. Iyer, R. R. Chang, and D. L. Lile, Sulfur as a surface passivation for InP. Appl. Phys. Lett. **53**, 134 (1988).

[262] A. Kapila and V. Malhotra, Passivation of the InP surface using polysulfide and silicon nitride overlayer. Appl. Phys. Lett. **62**, 1009 (1993).

[263] H.-C. Lin, W.-E. Wang, G. Brammertz, M. Meuris, and M. Heyns, Electrical study of sulfur passivated $In_{0.53}Ga_{0.47}As$ MOS capacitor and transistor with ALD Al_2O_3 as gate insulator. Microelectr. Engin. **86**, 1554 (2009).

[264] L. S. Wang, J. P. Xu, S. Y. Zhu, Y. Huang, and P. T. Lai, Improved interfacial and electrical properties of GaAs metal-oxide-semiconductor capacitors with HfTiON as gate dielectric and TaON as passivation interlayer. Appl. Phys. Lett. **103**, 092901 (2013).

[265] A. Alian, G. Brammertz, C. Merckling, A. Firrincieli, W.-E Wang, H. C Lin, M. Caymax, M. Meuris, K. De Meyer, and M. Heyns, Ammonium sulfide vapor passivation of $In_{0.53}Ga_{0.47}As$ and InP surfaces. Appl. Phys. Lett. **99**, 112114 (2011).

[266] Y. V. Medvedev, Thermodynamic stability of GaAs sulfur passivation, Appl. Phys. Lett. **64**, 3458 (1994).

[267] T. Hou, C. M. Greenlief, S. W. Keller, L. Nelen, and J. F. Kauffman, Passivation of GaAs (100) with an adhesion promoting self-assembled monolayer. Chem. Mater. **9**, 3181 (1997).

[268] C.-C. Chang, C.-Y. Chi, M. Yao, N. Huang, C.-C. Chen, J. Theiss, A. W. Bushmaker, S. LaLumondiere, T.-W. Yeh, M. L. Povinelli, C. Zhou, P. D. Dapkus, and S. B. Cronin, Electrical and optical characterization of surface passivation in GaAs nanowires, Nano Lett. **12**, 4484 (2012).

[269] V. Cremers, R. L. Puurunen, and J. Dendooven, Conformality in atomic layer deposition: Current status overview of analysis and modelling. Appl. Phys. Rev. **6**, 021302 (2019).

[270] D. J. Hagen, M. E. Pemble, and M. Karppinen, Atomic layer deposition of metals: Precursors and film growth. Appl. Phys. Rev. **6**, 041309 (2019).

[271] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, S. N. G. Chu, S. Nakahara, H.-J. L. Gossmann, J. P. Mannaerts, M. Hong, K. K. Ng, and J. Bude, GaAs metal–oxide–semiconductor field-effect transistor with nanometer-thin dielectric grown by atomic layer deposition. Appl. Phys. Lett. **83**, 180 (2003).

[272] C. L. Hinkle, A. M. Sonnet, E. M. Vogel, S. McDonnell, G. J. Hughes, M. Milojevic, B. Lee, F. S. Aguirre-Tostado, K. J. Choi, H. C. Kim, J. Kim, and R. M. Wallace, GaAs interfacial self-cleaning by atomic layer deposition. Appl. Phys. Lett. **92**, 071901 (2008).

[273] M. M. Frank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, HfO_2 and Al_2O_3 gate dielectrics on GaAs grown by atomic layer deposition. Appl. Phys. Lett. **86**, 152904 (2005).

[274] M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong. Surface passivation of III-V compound semiconductors using atomic-layer-deposition-grown Al_2O_3. Appl. Phys. Lett. **87**, 252104 (2005).

[275] Y. Xuan, Y. Q. Wu, H. C. Lin, T. Shen, and P. D. Ye. Submicrometer inversiontype enhancement-mode InGaAs MOSFET with atomic-layer-deposited Al_2O_3 as gate dielectric. IEEE Electr. Dev. Lett. **28**, 935 (2007).

[276] R. M. Wallace, P. C. McIntyre, J. Kim, and Y. Nishi. Atomic layer deposition of dielectrics on Ge and III-V materials for ultrahigh performance transistors. MRS Bullet. **34**, 493 (2009).

[277] Y.-C. Byun, S. Choi, Y. An, P. C. McIntyre, and H. Kim, Tailoring the interface quality between HfO_2 and GaAs via in situ ZnO passivation using atomic layer deposition. ACS Appl. Mater. Interf. **6**, 10482 (2014).

[278] Q. H. Luc, E. Y. Chang, H. D. Trinh, Y. C. Lin, H. Q. Nguyen, Y. Y. Wong, H. B. Do, S. Salahuddin, and C. C. Hu, Electrical characteristics of n, p- $In_{0.53}Ga_{0.47}As$ MOSCAPs with in situ PEALD-AlN interfacial passivation layer. IEEE Trans. Electr. Dev. **61**, 2774 (2014).

[279] A. T. Lucero, Y.-C. Byun, X. Qin, L. Cheng, H. Kim, R. M. Wallace, and J. Kim, Formation of a ZnO/ZnS interface passivation layer on $(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$: Electrical and in-situ X-ray photoelectron spectroscopy characterization. Jpn. J. Appl. Phys. **55**, 08PC02 (2016).

[280] S. Kundu, T. Shripathi, P. Banerji, Interface engineering with an MOCVD grown ZnO interface passivation layer for ZrO_2–GaAs metal–oxide–semiconductor devices. Sol. State Comm. **151**, 1881 (2011).

[281] N. A. Valisheva, M. S. Aksenov, V. A. Golyashov, T. A. Levtsova, A. P. Kovchavtsev, A. K. Gutakovskii, S. E. Khandarkhaeva, A. V. Kalinkin, I. P. Prosvirin, V. I. Bukhtiyarov, and O. E. Tereshchenko, Oxide-free InAs(111)A interface in metaloxide-semiconductor structure with very low density of states prepared by anodic oxidation. Appl. Phys. Lett. **105**, 161601 (2014).

[282] M. H. Zhang, F. Zhu, H. S. Kim, I. J. Ok, and J. C. Lee, Fluorine passivation in gate stacks of poly-Si/TaN/HfO2 (and HfSiON/HfO2)/Si through gate ion implantation, IEEE Electr. Dev. Lett. **28**, 195 (2007).

[283] M. Dammann, M. Chertouk, W. Jantz, K. Kohler, and G. Weimann, Reliability of InAIAs/InGaAs HEMTs grown on GaAs substrate with metamorphic buffer. Microelectr. Reliab. **40**, 1709 (2000).

[284] X. Cai, J. Lin, D. A. Antoniadis, and J. A. del Alamo, Electric-field induced F-migration in self aligned InGaAs MOSFETs and mitigation. IEEE Int. Electr. Dev. Meet. IEDM16-63 (2016).

[285] Y. Wang, S. Huang, X. Wang, X. Kang, R. Zhao, Y. Zhang, S. Zhang, J. Fan, H. Yin, C. Liu, W. Shi, Q. He, Y. Li, K. Wei, Y. Zheng, and X. Liu, Effects of fluorine plasma treatment on Au-free ohmic contacts to ultrathin-barrier AlGaN/GaN heterostructure. IEEE Transact. Electr. Dev. **66**, 2932 (2019).

[286] A. Troian, J. V. Knutsson, S. R. McKibbin, S. Yngman, A. S. Babadi, L.-E. Wernersson, A. Mikkelsen, and R. Timm, InAs-oxide interface composition and stability upon thermal oxidation and high-k atomic layer deposition. AIP Advances **8**, 125227 (2018).

[287] H. Kim, Y. Kwon, and B. J. Choi, AlN passivation effect on Au/GaN Schottky contacts. Thin Sol. Films **670**, 41 (2019).

[288] Y. Ando, K. Nagamatsu, M. Deki, N. Taoka, A. Tanaka, S. Nitta, Y. Honda, T. Nakamura, and H. Amano, Low interface state densities at Al_2O_3/GaN interfaces formed on vicinal polar and nonpolar surfaces. Appl. Phys. Lett. **117**, 102102 (2020).

[289] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo, M. Umeno, Investigations of SiO_2/n-GaN and Si_3N_4/n-GaN insulator-semiconductor interfaces with low interface state density. Appl. Phys. Lett. **73**, 809 (1998).

[290] Z. Liu, S. Cui, P. Shekhter, X. Sun, L. Kornblum, J. Yang, M. Eizenberg, K. S. Chang-Liao, and T. P. Ma. Effect of H on interface properties of Al_2O_3/$In_{0.53}Ga_{0.47}As$. Appl. Phys. Lett. **99**, 222104 (2011).

[291] R. D. Long, C. M. Jackson, J. Yang, A. Hazeghi, C. Hitzman, S. Majety, A. R. Arehart, Y. Nishi, T. P. Ma, S. A. Ringel, and P. C. McIntyre, Interface trap evaluation of Pd/Al_2O_3/GaN metal oxide semiconductor capacitors and the influence of near-interface hydrogen. Appl. Phys. Lett. **103**, 201607 (2013).

[292] M. Losurdo, P. Capezzuto, and G. Bruno, G. Perna, V. Capozzi, $N_2 – H_2$ remote plasma nitridation for GaAs surface passivation. Appl. Phys. Lett. **81**, 16 (2002).

[293] A.-M. El-Sayed, Y. Wimmer, W. Goes, T. Grasser, V. V. Afanas'ev, and A. L. Shluger, Theoretical models of hydrogen-induced defects in amorphous silicon dioxide. Phys. Rev. B **92**, 014107.

[294] Y. Liang, J. Kulik, T. C. Eschrich, R. Droopad, Z. Yu, and P. Maniar, Hetero-epitaxy of perovskite oxides on GaAs(001) by molecular beam epitaxy. Appl. Phys. Lett. **85**, 1217 (2004).

[295] M. Passlack, R. Droopad, P. Fejes, L. Wang. Electrical properties of Ga_2O_3/GaAs Interfaces and GdGaO Dielectrics in GaAs-Based MOSFETs. IEEE Electr. Dev. Lett. **30**, 2 (2009).

[296] H.W. Wan, Y.H. Lin, K.Y. Lin, T.W. Chang, R.F. Cai, J. Kwo, M. Hong, Ultra-high thermal stability and extremely low D_{it} on HfO_2/p-GaAs(001) interface. Microelectr. Engin. **178**, 154 (2017).

[297] C. Merckling, Method for manufacturing a low defect interface between a dielectric and III-V compound. US Patent US 8,314,017 B2 (2012).

[298] K. N. Huang, Y.-C. Lin, J.-C. Lin, C. C. Hsu, J. H. Lee, C.-H. Wu, J. N. Yao, H.-T. Hsu, V. Nagarajan, K. Kakushima, K. Tsutsui, H. Iwai, C. H. Chien, and E. Y. Chang, Study of e-mode AlGaN/GaN MIS-HEMT with La-silicate gate insulator for power applications. J. Electr. Mat. **49**, 1348 (2020).

[299] G. J. Burek, Y. Hwang, A. D. Carter, V. Chobpattana, J. J. M. Law, W. J. Mitchell, B. Thibeault, S. Stemmer, and M. J. W. Rodwell, Influence of gate metallization processes on the electrical characteristics of high-k/$In_{0.53}Ga_{0.47}As$ interfaces. J. Vac. Sci. Techn. B **29**, 040603 (2011).

[300] C. B. Zota, Doctoral Thesis, III-V MOSFETs for high-frequency and digital applications, Lund University, Sweden (2017).

[301] P.-C. Ku and C. J. Chang-Hasnain, Thermal oxidation of AlGaAs: modeling and process control. IEEE J. Quant. Electr. **39**, 577 (2003).

[302] F. Chouchane, G. Almuneau, N. Cherkashin, A. Arnoult, G. Lacoste, and C. Fontaine, Local stress-induced effects on AlGaAs/AlO_x oxidation front shape. Appl. Phys. Lett. **105**, 041909 (2014).

[303] J. I. Pankove, J. E. Berkeyheiser, S. J. Kilpatrick, and C. W. Magee, Passivation of GaAs surfaces. J. Electr. Mat. **12**, 359 (1983).

[304] S. Anantathanasarn, S. Ootomo, T. Hashizume, and H. Hasegawa, Surface passivation of GaAs by ultra-thin cubic GaN layer. Appl. Surf. Sci. **159–160**, 456 (2000).

[305] J. Riikonen, J. Sormunen, H. Koskenvaara, M. Mattila, M. Sopanen, and H. Lipsanen, Passivation of GaAs surface by ultrathin epitaxial GaN layer. J. Cryst. Growth **272**, 621 (2004).

[306] Y. Guo, L. Lin, and J. Robertson, Nitrogen passivation at GaAs:Al_2O_3 interfaces. Appl. Phys. Lett. **102**, 091606 (2013).

[307] P. A. Alekseev, M. S. Dunaevskiy, V. P. Ulin, T. V. Lvova, D. O. Filatov, A. V. Nezhdanov, A. I. Mashin, and V. L. Berkovits, Nitride surface passivation of GaAs nanowires: impact on surface state density. Nano Lett. **15**, 63 (2015).

[308] J. Robertson, Y. Guo, and L. Lin, Defect state passivation at III-V oxide interfaces for complementary metal–oxide–semiconductor devices. J. Appl. Phys. **117**, 112806 (2015).

[309] N. I. Goktas, P. Wilson, A. Ghukasyan, D. Wagner, S. McNamee, and R. R. LaPierre, Nanowires for energy: A review. Appl. Phys. Rev. **5**, 041305 (2018).

[310] M. Kang and R. S. Goldman, Ion irradiation of III–V semiconductor surfaces: From self-assembled nanostructures to plasmonic crystals. Appl. Phys. Rev. **6**, 041307 (2019).

[311] T. Mårtensson, J. B. Wagner, E. Hilner, A. Mikkelsen, C. Thelander, J. Stangl, B. J. Ohlsson, A. Gustafsson, E. Lundgren, L. Samuelson, and W. Seifert, Epitaxial growth of indium arsenide nanowires on silicon using nucleation templates formed by self-assembled organic coatings. Adv. Mater. **19**, 1801 (2007).

[312] S. Roddaro, K. Nilsson, G. Astromskas, L. Samuelson, L.-E. Wernersson, O. Karlström, and A. Wacker, InAs nanowire metal-oxide-semiconductor capacitors. Appl. Phys. Lett. **92**, 253509 (2008).

[313] M. Egard, S. Johansson, A.-C. Johansson, K.-M. Persson, A. W. Dey, B. M. Borg, C. Thelander, L.-E. Wernersson, and E. Lind, Vertical InAs nanowire wrap gate transistors with f_t>7 GHz and f_{max}>20 GHz. Nano Lett. **10**, 809 (2010).

[314] B. Mandl, J. Stangl, E. Hilner, A. A. Zakharov, K. Hillerich, A. W. Dey, L. Samuelson, G. Bauer, K. Deppert, and A. Mikkelsen, Growth mechanism of self-catalyzed group III-V nanowires. Nano Lett. **10**, 4443 (2010).

[315] M. Hjort, J. Wallentin, R. Timm, A. A. Zakharov, U. Hakanson, J. N. Andersen, E. Lundgren, L. Samuelson, M. T. Borgstrom, and A. Mikkelsen, Surface chemistry, structure, and electronic properties from microns to the atomic scale of axially doped semiconductor nanowires. ACS Nano **6**, 9679 (2012).

[316] E. Lind, E. Memišević, A. W. Dey, and L.-E. Wernersson, III-V heterostructure nanowire tunnel FETs. IEEE J. Electr. Dev. Soc. **3**, 96 (2015).

[317] P. Ponath, A. B. Posadas, and A. A. Demkov, Ge(001) surface cleaning methods for device integration. Appl. Phys. Rev. **4**, 021308 (2017).

[318] D. M. Zhernokletov, H. Dong, B. Brennan, M. Yakimov, V. Tokranov, S. Oktyabrsky, J. Kim, and R. M. Wallace, Surface and interfacial reaction study of half cycle atomic layer deposited HfO_2 on chemically treated GaSb surfaces. Appl. Phys. Lett. **102**, 131602 (2013).

[319] L. Lin and J. Robertson, Atomic mechanism of electric dipole formed at high-K: SiO_2 interface. J. Appl. Phys. **109**, 094502 (2011).

[320] G. Dingemans and W. M. M. Kessels, Status and prospects of Al_2O_3-based surface passivation schemes for silicon solar cells. J. Vac. Sci. Technol. A **30**, 040802 (2012).

[321] E. O'Connor, K. Cherkaoui, S. Monaghan, D. O'Connell, I. Povey, P. Casey, S. B. Newcomb, Y. Y. Gomeniuk, G. Provenzano, F. Crupi, G. Hughes, and P. K. Hurley, Observation of peripheral charge induced low frequency capacitance-voltage behaviour in metal-oxide-semiconductor capacitors on Si and GaAs substrates. J. Appl. Phys. **111**, 124104 (2012).

[322] M. A. Juntunen, J. Heinonen, V. Vähänissi, P. Repo, D. Valluru, and H. Savin, Near-unity quantum efficiency of broadband black silicon photodiodes with an induced junction. Nat. Photon. **10**, 777 (2016).

TABLE I: Selected milestones for III-V technology.

Milestone	Reference
1961 GaAs infrared LED	J. R. Biard and G. Pittman, Semiconductor radiant diode. US Patent 3293513, (1962)
1962 GaAs-based red LED	N. Holonyak and S. F. Bevacqua, Coherent (visible) light emission from Ga(As1−x Px) junctions. Appl. Phys. Lett. 1, 82 (1962).
1967 Growth of III-V p-n junction	Zh. I. Alferov, Possible development of a rectifier for very high current densities on the bases of a p-i-n structure with heterojunctions. Sov. Phys. Semicond. 1, 358 (1967).
1970 III-V laser diode	M. B. Panish, I. Hayashi, and S. Sumski, Double-heterostructure injection lasers with room-temperature thresholds as low as 2300 A/cm2. Appl. Phys. Lett. 16, 326 (1970).
1970 III-V laser diode	Zh. I. Alferov, Electroluminescence of heavily-doped heterojunctions p AlxGa12x-nGaAs. J. Lumin. 1, 869. (1970).
1970 GaAs solar cell	Zh. I. Alferov, V. M. Andreev, M. B. Kagan, I. I. Protasov, and V. G. Trofim, Solar-energy converters based on p-n AlxGa12xAs-GaAs heterojunctions. Sov. Phys. Semicond. 4, 2047 (1971).
1971 Growth of GaAs p-n junctions	A. Y. Cho, Film deposition by molecular-beam techniques. J. Vac. Sci. Techn. 8, S31 (1971).
1971 Growth of AlGaAs/GaAs quantum Wells	A. Y. Cho, Growth of periodic structures by the molecular-beam method. Appl. Phys. Lett. 19, 467 (1971).
1976 GaAs metal semiconductor field-effect transistor	A. Y. Cho, GaAs MESFET prepared by molecular beam epitaxy. Appl. Phys. Lett. 28, 30 (1976).
1977 InGaAs photodiode.	T. P. Pearsall and R. W. Hopson, Growth and characterization of lattice-matched epitaxial films of GaxIn1−xAs/InP by liquid-phase epitaxy. J. Appl. Phys. 48, 4407 (1977).
1978 Quantum well laser	R. D. Dupuis, P. D. Dapkus, N. Jr. Holonyak, E. A. Rezek, and R. Chin, Room temperature operation of quantum-well Ga(1-x)Al(x)As-GaAs laser diodes grown by metalorganic chemical vapor deposition. Appl. Phys. Lett. 32, 295 (1978).
1978 HEMT electron channel	R. Dingle, H. L. Störmer, A. C. Gossard and W. Wiegmann, Electron mobilities in modulation-doped semiconductor heterojunction superlattices, Appl. Phys. Lett. 33, 665 (1978).
1980 HEMT device	T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, A new field-effect transistor with selectively doped GaAs/n-AlGaAs heterostructures. Jpn. J. Appl. Phys. 19, L225 (1980).
1982 AlGaAs/GaAs bipolar junction transistor	W. V. McLevige, H. T. Yuan, W. M. Duncan, W. R. Frensley, F. H. Doerbeck, H. Morkoc, T. J. Drummond. GaAs/AlGaAs heterojunction bipolar transistors for integrated circuit applications. IEEE Electr. Dev. Lett. 3, 43 (1982).
1983 1.55 micron laser diode	H. Temkin, K. Alavi, W. R. Wagner, T. P. Pearsall, A. Y. Cho. 1.5-1.6 micron GaInAs/AlInAs multiquantum well laser grown by molecular beam epitaxy. Appl. Phys. Lett. 42, 845 (1983).
1989 P-type doping of GaN	H. Amano, M. Kito, K. Hiramatsu, and I. Akasaki, P-Type Conduction in Mg-Doped GaN Treated with Low-Energy Electron Beam Irradiation (LEEBI). Jpn. J. Appl. Phys. 28, L2112 (1989).
1993 GaN-based HEMT	M. Khan, A. Bhattarai, J. Kuznia, and D. Olson, High Electron Mobility Transistor Based on a GaN-AlGaN Heterojunction. Appl. Phys. Lett. 63, 1214 (1993).
1994 Efficient blue LED	S. Nakamura, T. Mukai & M. Senoh, Candela-class high-brightness InGaN/AlGaN double-heterostructure blue-light-emitting diodes. Appl. Phys. Lett. 64, 1687 (1994).
2005 III-V laser integration with silicon waveguide in CMOS-compatible way	H. Park, A. Fang, S. Kodama, and J. Bowers, Hybrid silicon evanescent laser fabricated with a silicon waveguide and III-V offset quantum wells, Opt. Express 13, 9460 (2005).
2009 Monolithic InP HBT integration with silicon CMOS	T.E. Kazior, J.R. LaRoche, D. Lubyshev, J. M. Fastenau, W. K. Liu, M. Urteaga, W. Ha, J. Bergman, M. J. Choe, M. T. Bulsara, E. A. Fitzgerald, D. Smith, D. Clark, R. Thompson, C. Drazek, N. Daval, L. Benaissa, and E. Augendre, High performance differential amplifier through the direct monolithic integration of InP HBTs and Si CMOS on silicon substrates. IEEE MTT-S International Microwave Symposium Digest, 1113 (2009)
2014 Solar-efficiency higher than 45% using III-V multijunctions	New world record for solar cell efficiency at 46%, Presseinformation of Fraunhofer, CEA-LETI, and Soitec, December 1st, No. 26/14 Freiburg (2014).
2015 First THz HEMT device	X. Mei, W. Yoshida, M Lange, J. Lee, J. Zhou, P.-H. Liu, K. Leong, A. Zamora, J. Padilla, S. Sarkozy, R. Lai, and W. R. Deal, First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process IEEE Electron Device Letters. 36, 327 (2015).

TABLE II: Summary of surface cleaning and crystalline oxidation parameters for different crystalline III-V surfaces.

Starting surface parameters	Monolayer oxidation parameters	Material characterization
As-decapping (400 ºC) → GaAs(100)(2×4) (Fig. 3a)	Deposition of Ga_2O molecules in 10^{-5} mbar at 400 ºC using high temperature Ga_2O_3 effusion cell	**Ordered Ga_2O molecule layer on GaAs** shows 2x periodicity, RHEED, STM, PL, C-V, FET, Ref. 29
MBE of GaN + extra Ga on surface → GaN(0001)(1×1)-Ga	1×10^{-5} mbar O_2, 550 ºC, 2×10^5 L exposure	**GaN(0001)(3√3×3√3)-O-R30º**: LEED, STM, STS, AES, theory, Ref. 46
As-decapping → InAs(100)(4×2) (Fig. 3c	Deposition of In_2O molecules (effusion cell) at room temperature + 380 ºC post annealing	**Ordered In_2O molecule layer on InAs:** 2x or 3x periodicity rows, STM, STS, theory Refs. 47, 48
As-decapping → $In_{0.53}Ga_{0.47}As$(100)(4×2)	Deposition of In_2O molecules (effusion cell) at room temperature + 380 ºC post annealing	**Ordered In_2O molecule layer on $In_{0.53}Ga_{0.47}As$:** 2x or 3x periodicity, STM, STS, theory Refs. 47, 48
Sputtering (1 kV, 10 mA) + heating (450 ºC) → InAs(100)(4 × 2) (Fig. 3c)	4×10^{-6} mbar O_2, 30 min, 350 ºC; simultaneous stop of heating and oxygen	**InAs(100)(3×1)-O**: LEED, STM, theory Ref. 50
As-decapping (380 ºC) → InAs(100)(4×2) (Fig. 3c)	8×10^{-6} mbar O_2, 5 min, 350 ºC; simultaneous stop of heating and oxygen	**InAs(100)(3×1)-O**: LEED, XPS, ALD; Ref. 53
As-decapping → InAs(100)(2×4) (Fig. 3a)	4×10^{-6} mbar O_2, 30 min, 350 ºC	**InAs(100)(3×1)-O**: RHEED, XPS, AFM, C-V; Ref. 54
Sputtering (2 kV, 15 mA) + heating (450 ºC) → InAs(100)(4×2) (Fig. 3c)	4×10^{-6} mbar O_2, 15 min, 400 ºC; simultaneous stop of heating and oxygen	**InAs(100)(3×1)-O**: LEED, synchrotron XPS; Ref. 58
As-decapping (380ºC) → InAs(100)(4×2) (Fig. 3c)	3×10^{-6} mbar O_2, 20 min, 290-330 ºC + post-heating without O_2 for 10 min	**InAs(100)(3×1)-O**: LEED, XPS, ALD; Ref. 62
Sputtering (1 kV, 10 mA) + heating (400 ºC) → InAs(100)(4×2) (Fig. 3c)	8×10^{-6} mbar O_2, 15 min, 360 ºC; simultaneous stop of heating and oxygen	**InAs(100)(3×1)-O**: LEED, STM synchrotron XPS, leakage current; Ref. 66
Sputtering (1 kV, 10 mA) + heating (450 ºC) → InAs(100)(4×2) (Fig. 3c)	4×10^{-6} mbar O_2, 15 min, 400 ºC; simultaneous stop of heating and oxygen	**InAs(100)c(4×2)-O**: LEED, STM; Ref. 50
As-decapping (380ºC) → InAs(100)(4×2) (Fig. 3c)	4×10^{-6} mbar O_2, 15 min, 380 ºC; simultaneous stop of heating and oxygen	**InAs(100)c(4×2)-O**: LEED, XPS; Ref. 53
Sputtering (2 kV, 15 mA) + heating (450 ºC) → InAs(100)(4x2) (Fig. 3c)	4×10^{-6} mbar O_2, 15 min, 450 ºC; simultaneous stop of heating and oxygen	**InAs(100)c(4×2)-O**: LEED, synchrotron XPS; Ref. 59
Sputtering (1 kV, 10 mA) + heating (400 ºC) → InAs(100)(4×2) (Fig. 3c)	4×10^{-6} mbar O_2, 10 min, 380 ºC; simultaneous stop of heating and oxygen	**InAs(100)c(4×2)-O**: LEED, STM synchrotron XPS, leakage current; Ref. 66
Sputtering (2 kV, 15 mA) + heating (400 ºC) → InSb(100)(4×2) (Fig. 3c)	4×10^{-6} mbar O_2, 15 min, 400 ºC; simultaneous stop of heating and oxygen	**InSb(100)(3×1)-O**: LEED, synchrotron XPS; Ref. 58
Sputtering (1 kV, 10 mA) + heating (450 ºC) → InSb(100)(4×2) (Fig. 3c)	4×10^{-7} - 1×10^{-5} mbar O_2, 5-15 min, 320-440 ºC; simultaneous stop of heating and oxygen	**InSb(100)(1×2)-O**: LEED, synchrotron XPS, STM, theory; Ref. 57
Sputtering (1 kV, 15 mA) + heating (400 ºC) → InSb(111)B(3×3) (Fig. 3f)	1×10^{-5} mbar O_2, 10 min, 400 ºC; simultaneous stop of heating and oxygen	**InSb(111)B(3×3)-O**: LEED, STM, STS; Ref. 65
Sputtering (1 kV, 15 mA) + heating (400 ºC) → InSb(111)B(3×3) (Fig. 3f)	1×10^{-5} mbar O_2, 10 min, 360 ºC; simultaneous stop of heating and oxygen	**InSb(111)B(2×2)-O**: LEED, XPS, STM, STS; Ref. 65
HCl:IPA (1:3) wet etching (150 s) + IPA (60 s) + 1 min air exposure + heating (300 ºC) + H_2 exposure (5×10^{-5} mbar) 30 min at 300 ºC → InSb(111)B(3×3) (Fig. 3f)	1×10^{-5} mbar O_2, 10 min, 360 ºC; simultaneous stop of heating and oxygen	**InSb(111)B(2×2)-O**: LEED, XPS, STM, STS; Ref. 65
Sputtering (1 kV, 10 mA) + heating (450 ºC) → InP(100)(2×4) (Fig. 3d)	4×10^{-6} mbar O_2, 15 min, 500 ºC; simultaneous stop of heating and oxygen	**InP(100)(2×3)-O**: LEED, STM; Ref. 50
Sputtering (1 kV, 10 mA) + heating (550 ºC) + In deposition (2 ML) + heating (500 ºC) → GaAs(100)(4×2)-In (Fig. 3c)	4×10^{-6} mbar O_2, 15 min, 520 ºC; simultaneous stop of heating and oxygen	**GaAs(100)(4×3)-InO**: LEED, STM, theory; Ref. 50
Sputtering (1 kV, 10 mA) + heating (450 ºC) + In deposition (2 ML) + heating (450 ºC) → GaAs(100)(4x2)-In (Fig. 3c)	4×10^{-6} mbar O_2, 15 min, 470 ºC; simultaneous stop of heating and oxygen	**GaAs(100)(4×3)-InO**: LEED, synchrotron XPS, PL; Ref. 64
Sputtering (1 kV, 10 mA) + heating (550 ºC) + In deposition (1 ML) + heating (500 ºC) → GaAs(100)(4×2)-In (Fig. 3c)	2×10^{-7} mbar O_2, 5 min, 470 ºC; simultaneous stop of heating and oxygen	**GaAs(100)c(4×2)-InO**: LEED, XPS, PL; Ref. 59
Sputtering (1 kV, 10 mA) + heating (450 ºC) + In deposition (1 ML) + heating (450 ºC) → GaAs(100)(4×2)-In (Fig. 3c)	4×10^{-6} mbar O_2, 5 min, 470 ºC; simultaneous stop of heating and oxygen	**GaAs(100)c(4×2)-InO**: LEED, synchrotron XPS, PL; Ref. 64
Sputtering (1 kV, 10 mA) + heating (450 ºC) + In deposition (0.5 ML) + heating (450 ºC) → GaAs(100)(4×2)-In (Fig. 3c)	4×10^{-6} mbar O_2, 5 min, 470 ºC; simultaneous stop of heating and oxygen	**GaAs(100)(1×1)-InO**: LEED, synchrotron XPS, PL; Ref. 64
As-decapping (350ºC) → $In_{0.53}Ga_{0.47}As$(100)(4×2)	5×10^{-5} mbar O_2, 5 min, 350 ºC; simultaneous stop of heating and oxygen	**$In_{0.53}Ga_{0.47}As$(100)(3×1)**: LEED, XPS, ALD, CV; Ref. 63
Over-oxidized $In_{0.53}Ga_{0.47}As$(100)(4×2) at 1×10^{-4} mbar, 2 min, 320 ºC→ amorphous $In_{0.53}Ga_{0.47}As$(100) surface	Atomic-hydrogen exposure at 1×10^{-6} mbar, 5 min, 350 ºC	**$In_{0.53}Ga_{0.47}As$(100)(3×2)**: LEED, XPS, ALD, CV; Ref. 63
Sputtering (1 kV, 4 mA) + heating (450 ºC) + In deposition (2 ML) + heating (400 ºC) → GaSb(100)(4×2)-In	2×10^{-6} mbar O_2, 15 min, 400 ºC; simultaneous stop of heating and oxygen	**GaSb(100)(1×3)-InO**: LEED, XPS, STM, STS; Ref. 60
Acetone (1 min) + methanol (1 min) + and isopropanol (1 min) → $Al_{0.25}Ga_{0.75}N$ (0001)(1×1)	N_2 : O_2 flow ratio was 45 sccm : 0.5 sccm, and the AlGaN temperature was 550 ºC for 10 min	**$Al_{0.25}Ga_{0.75}N$(0001)(1×1)**: LEED, XPS, ALD, CV; Ref. 55

TABLE III: Comparison of different passivation approaches to decrease the oxidation-related defect-level densities (D_{it}) at III-V interfaces.

Passivation system	**D_{it}**	**Comment**
Anodic InP oxidation for Al_2O_3/InP interface; Ref. 37 (1986)	4×10^{10} $eV^{-1}cm^{-2}$	Study of thin $In(PO_3)_y$ oxide layer
Si interface control layer passivation of SiO_2/GaAs; Ref. 256 (1988)	$\sim10^{12}$ $eV^{-1}cm^{-2}$	MOSFET inversion
Sulfur-passivated SiO_2/InP; Ref. 261 (1988)	10^{10} - 10^{12} $eV^{-1}cm^{-2}$	Enhancement MOSFET
Sulfur-passivated SiN_x/InP; Ref. 262 (1993)	$\sim10^{12}$ $eV^{-1}cm^{-2}$	Excess sulfur and phosphorous pentasulfide.
MBE Ga_2O_3 passivation of GaAs; Ref. 26 (1997)	5×10^{10} $eV^{-1}cm^{-2}$	
SiO_2/GaN; Ref. 289 (1998)	2.5×10^{12} $eV^{-1}cm^{-2}$	
Si interface control layer of SiN_x/InP; Ref. 258 (2000)	$\sim10^{10}$ $eV^{-1}cm^{-2}$	
ALD self cleaning of Al_2O_3/GaAs; Ref. 271 (2003)	5×10^{11} $eV^{-1}cm^{-2}$	Oxide leakage 1×10^{-7} A/cm^2 at ±2V
ALD self cleaning of InGaAs; Ref. 274 (2005)	$\sim10^{12}$ $eV^{-1}cm^{-2}$	Oxide leakage 2×10^{-9} A/cm^2 at ±2V
Si interface control layer of HfO_2/GaAs; Ref. 259 (2006)	1×10^{12} $eV^{-1}cm^{-2}$	
MBE Ga_2O_3 and GdGaO passivation of GaAs, Ref. 295 (2009).	1×10^{11} $eV^{-1}cm^{-2}$	Oxide leakage 2×10^{-8} A/cm^2 at ±2V
$(NH_4)_2S$ passivation of Al_2O_3/InGaAs; Ref. 263 (2009)	3×10^{12} $eV^{-1}cm^{-2}$	MOSFET study
$(NH_4)_2S$ passivation of Al_2O_3/InGaAs; Ref. 111 (2011)	2.5×10^{12} cm^{-2}	Wet chemistry before ALD
Hydrogen passivation of Al_2O_3/InGaAs; Ref. 290 (2011)	3.7×10^{11} $eV^{-1}cm^{-2}$	Insulator deposition in hydrogen environment
Vapor $(NH_4)_2S$ passivation of Al_2O_3/InP; Ref. 265 (2011)	$\sim10^{12}$ $eV^{-1}cm^{-2}$	Buried channel transistor test (HEMT type)
ZnO-passivated ZrO2/GaAs interface Ref. 280 (2011)	2.5×10^{11} $eV^{-1}cm^{-2}$	Oxide leakage $\sim10^{-7}$ A/cm^2 at ±2V
MBE-mediated sulfur of III-V's; Ref. 297 (2012)		Sulfur induced (2x1) surface structure
$(NH_4)_2S$ + TaON passivation of HfTiON/GaAs; Ref. 264 (2013)	1×10^{12} $eV^{-1}cm^{-2}$	Oxide leakage $\sim10^{-5}$ A/cm^2 at ±2V
Crystalline oxidation of HfO_2/InAs interfaces, Ref. 54 (2013)	2×10^{11} $cm^{-2}eV^{-1}$	
Hydrogen passivation of Al2O3/GaN; Ref. 291 (2013)	$\sim10^{11}$ $eV^{-1}cm^{-2}$	
ALD of epitaxial La_2O_3/GaAs; Ref. 35 (2013)	3×10^{11} $cm^{-2}eV^{-1}$	
ALD-AlN interface for Al_2O_3/InGaAs; Ref. 278 (2014)	$\sim10^{11}$ $eV^{-1}cm^{-2}$	Oxide leakage $\sim10^{-9}$ A/cm^2 at ±2V; crystalline AlN interface layer
F passivation of InAs with fluorinated anodic layer; Ref. 281 (2014)	$2\text{-}12\times10^{10}$ $eV^{-1}cm^{-2}$	Atomic resolution TEM of crystalline InAs interface
ZnS passivation of HfO_2/InGaAs; Ref. 279 (2016)	$\sim10^{11}$ $eV^{-1}cm^{-2}$	In-situ XPS characterization
MBE passivation of HfO_2/GaAs; Ref. 296 (2017)	1×10^{11} $eV^{-1}cm^{-2}$	Oxide leakage leakage 2×10^{-8} A/cm^2 at ±2V
Crystalline oxidation of HfO_2/InGaAs interface; Ref. 63 (2017)	$\sim10^{12}$ $eV^{-1}cm^{-2}$	In-situ XPS characterization
AlN interface layer on GaN; Ref. 287 (2019)	$\sim10^{12}$ $eV^{-1}cm^{-2}$	Metal contact passivation
ALD- Al_2O_3/GaN; Ref. 288 (2020)	3×10^{10} $eV^{-1}cm^{-2}$	
MBD method for La-silicate passivation of AlGaN; Re. 298 (2020)	0.5×10^{12} $eV^{-1}cm^{-2}$	E-mode MOSHEMT of AlGaN/GaN

FIGURE CAPTIONS

FIG. 1. (a) Schematic presenting how an oxidized III-V surface (red line) lies at the interface between a III-V crystal and a film. The film is usually insulating or metallic in device applications. The oxidized III-V surfaces include defects such as point defects (e.g. broken dangling bonds) and line defects (e.g. grain boundaries) which cause performance degradation in the current and future devices. (b) Schematic of the band-gap structure for an insulator/III-V interface, where the oxidized III-V layer cause many defect-induced electron levels (short red lines) in the crucial band gap area. Charge carriers (electrons and holes) can be consumed due to the recombination via the defect levels. Note that border traps in the insulator side are excluded here. (c) Schematic of the band-gap structure for an Ohmic metal/III-V interface, which also includes oxygen atoms in the III-V side because it is difficult to avoid oxygen incorporation. Here the oxygen-induced defect levels can cause the carrier recombination. In addition, resistive losses often occur at metal-semiconductor interfaces because it is difficult to prepare high-quality Ohmic contacts.

FIG. 2. (a) LEED pattern from an etched InP(100) surface, showing (1×1) LEED spots, arising from the crystal planes below the topmost amorphous layer. Note that the (0,0) reciprocal spot is not seen due to a shadowing electron gun. (b) LEED pattern of (2×4) from the same InP surface after a post-treatment in vacuum conditions at about 350 ºC. (c and e) STM images from the etched surface before any vacuum treatment showing a disordered (amorphous) structure for the topmost layer. (d and f) STM images from after the vacuum treatment, which improves ordering and crystal quality of the topmost layer.

FIG. 3. Established atomic models for some common III-V reconstructions. (a) The GaAs(100)(2×4) and InAs(100)(2×4) surfaces exhibit two different structures depending on the As amount: so called β-2 and α-2. The latter is shown here, while in the β-2 structure has the second As-As dimer in the topmost layer instead of group-III dimers. (b) GaAs(100)(6×6) typically coexists with GaAs(100)(4×2) reconstructed areas when the amount of As is decreased on the surface. [Reprinted with permission from Ref. 134, Phys. Rev. B **73**, 035317 (2006). © 2006 by the American Physical Society.] (c) III-V(100)(4×2) structures contain specific sub-surface dimers. The indium-containing III-V surfaces tend to have a structure with a higher concentration of group-III elements (the left model). These unusual models are energetically stable and reproduce all experimental data to date. [Reprinted with permission from Ref. 210, Phys. Rev. B **81**, 245305 (2010). © 2006 by the American Physical Society.] (d) InP(100) has a different (2×4) structure as compared to GaAs and InAs when the amount of group-V elements decreases. It is noted that InP(100) does not result in a (4×2) reconstruction. (e) GaSb(100) also differs drastically from III-As(100) because GaSb(100) does not result in either (2×4) or (4×2) reconstructions. In contrast, GaSb(100) shows various (4×3) building blocks with different Sb/Ga ratio, which often appears as a (1×3) diffraction pattern. When indium is added on GaSb, the (4×2) appears. [Reprinted with permission from Ref. 60, Appl. Phys. Lett. **107**, 061601 (2015). © 2015 by the American Institute of Physics.] (f) InSb(111)B shows the (3×3) reconstruction, as many other III-V(111) too, when the Sb/In surface ratio decreases. [Reprinted with permission from from Ref. 65, Sci. Rep. **8**, 14382 (2018). © 2018 by the Springer Nature.]

FIG. 4. Basic steps to include the ultrahigh-vacuum (UHV) based heating and crystalline oxidation in the processing of III-V device interfaces. First, the wet chemistry is technologically one of the most common methods to remove most of the native oxides and contaminants from various starting III-V

surfaces. The air-exposure time after a chemical treatment should be minimized during the sample transfer to a vacuum chamber (see Section II). Heating under UHV conditions typically enhances a degree of crystalline order at III-V surfaces. Note that the topmost surface is very disordered after a wet chemical treatment. During the UHV heating, it is also possible utilize different gas exposures as well: e.g. H_2 or NH_3 to decrease the amounts of remaining oxygen and carbon contaminants. When crystalline order of the starting III-V surface has been obtained, the controlled oxidation can be performed by feeding oxygen gas via a leak valve (pressures 10^{-7} to 10^{-5} mbar, see Table II). Finally, the sample can be transferred to the next step of a film growth via air or using an interconnected multi-chamber system.

FIG. 5. Examples of the results obtained by the common interface probes. (a) High-resolution XPS spectra measured with a synchrotron source from SiN_x/InGaAs: the semiconductor bulk peak is commonly used as the reference energy ("0" eV relative binding energy), and the interface-related emissions can be seen as shoulders or tails of the substrate bulk peak or even as separate peaks. The largest interface-related shifts for Ga and In are around 1 eV in this example, while the interface-induced shifts of As extend up to 5 eV; reproduced from Ref. 162. (b) TEM data from the interfaces of an InAs film transferred on SiO_2/Si substrate. Thermal oxidation of InAs surfaces under non-UHV conditions has induced crystallization of the oxidized InAs ($InAsO_x$ layer) which interestingly resembles the crystalline tridymite SiO_2/Si interface.[91] [Reprinted with permission from Ref. 45, Nature **468**, 286 (2010). © 2010 by the Springer Nature.] (c) Photoluminescence (PL) from different GaAs interfaces: the PL intensity for Ga_2O_3/GaAs is almost the same as that for epitaxial AlGaAs/GaAs, while for a bare GaAs surface oxidized in air, the PL intensity has decreased due to the high density of surface defects [Reprinted with permission from Ref. 187, Appl. Phys. Lett. **66**, 625 (1995). © 1995 by the American Institute of Physics.] (d) Capacitance-voltage curves as a function the modulation frequency which increases as

indicated with the arrow in the curves. The frequency dispersion in the depletion region (around 0 V), appearing as a hump of the capacitance increase, is due to the interface defects of which the density can be decreased by a proper forming-gas passivation annealing, ("FGA"). [Reprinted with permission from Ref. 202, ACS Appl. Mater. Interf. **9**, 7819 (2017). © 2006 by the American Chemical Society.]

FIG. 6. LEED patterns from InAs(100) surfaces. (a) Before any cleaning, an amorphous oxidized surface is so thick that no (1×1) pattern arises from the bulk plane(s). (b) After the Ar-ion sputtering+vacuum heating, the LEED shows a (4×2) pattern for clean InAs(100); note that (4×2) and c(8×2) describe the same surface in practice. (c) After the controlled oxidation in the UHV chamber, LEED shows c(4×2) pattern. (d) After an alternative oxidation, the LEED shows a (3×1) pattern. The large white squares mark the (1×1) reciprocal lattice cells for the bulk planes, and the rectangles show the surface reciprocal unit cells, as visualized in real space. All images show a shadow of the electron beam source, and the (0,0) diffraction spot is hidden. [Reprinted by permission from Ref. 66, ACS Appl. Mat. Int. **10**, 44932 (2018). © 2018 by the American Chemical Society.]

FIG. 7. STM images from the different InAs(100) surfaces corresponding to the LEED patterns in Figure 6(a)-(d). The InAs surface which is oxidized in air (native oxide) in (a) does not show any long-range order, as compared to the crystalline oxidized InAs in (e). Another typical feature of the crystalline oxidized surfaces is their two-dimensional terrace-step structure seen in the large-scale images (c)-(d). In the zoomed-in image (e), the surface was oxidized in such way that both the (3×1)-O and c(4×2)-O phases coexisted together with white line features which were associated with extra AsO_x. [Reprinted by permission from Ref. 66, ACS Appl. Mat. Interf. **10**, 44932 (2018). © 2018 by the American Chemical Society.] (f) RHEED patterns from InAs(100)(3×1)-O after the vacuum preparation as well as after air

exposure of this surface. Bright white diffraction lines mark the (1×1) distance in the reciprocal space, which becomes divided into three equal parts by two less bright lines, indicating the 3× periodicity for the surface. After air exposure, these RHEED intensity lines become weaker, but they can be still resolved.

FIG. 8. High-resolution synchrotron photoemission spectroscopy (PES) spectra and their fitting analysis for the (3×1)-O surface: (a) As3d, (b) In4d, and (c) O1s. The surface sensitivity of the spectra has been changed by changing the photon energy and thus the kinetic energy of photoelectrons in the synchrotron-radiation center. The surface sensitivity increases from the top to bottom spectra. The *B* components mark the bulk substrate emission while the *S* components are surface related features. [Reprinted with permission from Ref. 58, Appl. Phys. Lett. **106**, 011606 (2015). © 2015 by the American Institute of Physics.]

FIG. 9. Initial atomic models proposed for the c(4×2)-O and (3×1)-O surfaces: blue spheres are In atoms, red spheres are As atoms, and green spheres are O atoms. The comparison of the measured and simulated (based on the models) STM images for the c(4×2)-O surface: (a vs. b in the filled state) and (c vs. d in the empty state), respectively. The comparison of the measured and simulated (based on the models) STM images for the (3×1)-O surface: (e vs. f in the filled state) and (g vs. h in the empty state), respectively. [Reprinted with permission from Ref. 50, Phys. Rev. B **83**, 195329 (2011). © 2011 by the American Physical Society.]

FIG. 10. Characterization of the InAs(100)(4×2) surface after the deposition of 1 ML of In_2O molecules and post annealing at 380 ^oC. (a) and (b) STM images show ordering of In_2O molecules after the post

annealing with 3× periodicity. Label *A* marks a local area of the initial InAs(100)(4×2) surface. (c) Potential atomic models to describe the In_2O adsorption. [Reprinted with permission from Ref. 48, J. Chem. Phys. **133**, 164704 (2010). © 2010 by the American Institute of Physics.]

FIG. 11. Capacitance-voltage curves measured from (a) the HfO_2/InAs reference sample with HCl surface treatment and (b) the HfO_2/InAs sample with the (3×1)-O interface [Reprinted with permission from Ref. 54, Appl. Phys. Lett. **103**, 143510 (2013). © 2013 by the American Institute of Physics.] (c) and (d) Characterization of InAs MOSFET with ZrO_2/(3×1)-O/InAs gate [Reprinted with permission from Ref. 205, IEEE Trans. Electr. Dev. **62**, 2429 (2015). © 2015 by the IEEE.]

FIG. 12. Mapping the parameter space for the InSb(100)(1×2)-O surface. The InSb temperature, oxygen pressure, and oxidation time have a complex interplay in the crystalline oxide formation. One expected trend is that decreasing the oxygen pressure increases the oxidation time. It also appears that increasing the InSb substrate temperature enables one to increase the oxygen pressure or the oxidation time (exposure). This indicates the presence of a competing oxide desorption kinetic process at the elevated temperatures and/or the formation a thicker oxide (i.e. increased oxygen diffusion toward bulk) with the same surface reconstruction. [Reprinted with permission from Ref. 57, Phys. Rev. B **90**, 045312 (2014). © 2014 by the American Physical Society.]

FIG. 13. Atomic models as a function of oxygen concentration for the InSb(100)(1×2)-O. Among many possible oxygen-containing structures, these models explain the measurements of the surface to date. At the initial stages of oxidation, oxygen atoms tend to occupy the subsurface Sb sites-1 in (a), suggesting the Sb diffusion toward the surface. The oxygen concentration varies between 0.5 - 2 ML among the

different models, but the same (1×2) periodicity remains. In the 2-ML model in (d), there are 4 oxygen atoms incorporated per the (1×2) area, leading to the formation of local InO, InO_3, SbO_2, and SbO_3 bonding configurations. Yet, the calculated core-level shifts show only small high binding-energy shift around +0.2 eV for indium, while the most positive shift is about +1.0 eV for antimony according to the model. [Reprinted with permission from Ref. 57, Phys. Rev. B **90**, 045312 (2014). © 2014 by the American Physical Society.]

FIG. 14. (a) Calculated band structure for the atomic model with 0.5 ML of oxygen (i.e. Figure 13a) showing the metallic nature for this structure having bands crossing the Fermi energy around 0 eV. Metallic bands largely arise from the dimer-atoms 2 and 3 of the model in Figure 13a. (b) Calculated band structure for the atomic model with 2.0 ML of oxygen (i.e. Figure 13d) showing an insulating structure. Red circles show the filled indium dangling-bond related band. (c) Measured band gap at the (1×2)-O surface using scanning tunneling spectroscopy, showing a clear zero dI/dV intensity around the Fermi level (= 0 eV). [Reprinted and adapted with permission from Ref. 57, Phys. Rev. B **90**, 045312 (2014). © 2014 by the American Physical Society.]

FIG. 15. (a) The (3×3) LEED pattern has been observed before and after the oxidation of InSb(111)B surface. (b) The (2×2) LEED pattern has been observed before and after the oxidation of InSb(111)B surface. (c) XPS characterization of InSb(111)-B as a function of the oxidation reveals small oxidation-induced features, tails in the spectra. (d) STM from InSb(111)B(3×3) surface after the oxidation that induces formation of (2×2)-O phase, which is seen as the formation of a bright island on the top of upper terrace. Local oxidation-induced (2×2)-O formation is also seen on the lower terrace. [Reprinted and adapted with permission from from Ref. 65, Sci. Rep. **8**, 14382 (2018). © 2018 by the Springer Nature]

FIG. 16. Summary for the oxidized InP(100)(2×3)-O surface. Large-scale STM image shows a two-dimensional epitaxial structure. Inset exemplifies LEED pattern in which 2× spots are typically sharper than ×3 spots. Core-level spectra measured by traditional XPS. Because of the poor resolution (due to a non-monochromatized x-ray source and of the difficulty to determine the substrate peak position carefully) the presented fitting of In3d is not as justified as the clear oxidation-induced feature in P2p at +4.7 eV. [Reprinted with permission from Ref. 50, Phys. Rev. B **83**, 195329 (2011). © 2011 by the American Physical Society.]

FIG. 17. Characterization of the GaAs surface after deposition of Ga_2O molecules. (a) Zoomed-in STM image shows that adsorption of Ga_2O starts on the top of the intial As-dimer rows, causing specific bright features which have not been seen on the clean GaAs(100)(2×4). (b) The model to describe the Ga_2O bonding sites. (c) and (d) STS data indicate the unpinned Fermi level at the Ga_2O/GaAs system because the surface Fermi-level lies near the valence-band maximum on the p-GaAs substrate and near the conduction-band minimum on n-GaAs. [Reprinted with permission from Ref. 29, Microelectr. Engineer. **80**, 138 (2005). © 2005 the Elsevier.]

FIG. 18. (a) STM image from GaAs(100)(4×3)-InO surface. Inset shows the LEED pattern where a smaller rectangle visualizes the (4×3) reciprocal lattice cell in real space. (b) Zoomed-in STM image showing oxidation-induced building blocks between the initial dimer rows. (c) Simulated STM image based on the first atomic model presented in (d): red spheres are As atoms, gray spheres are In atoms, green spheres are O atoms, and blue spheres are Ga atoms. [Reprinted with permission from Ref. 50, Phys. Rev. B **83**, 195329 (2011). © 2011 by the American Physical Society.]

FIG. 19. STM images from a sputter-cleaned GaAs(100)(6×6) substrate, and after the indium deposition + oxidation for the GaAs(100)(1×1)-InO surface of which LEED images are shown below for two different electron energies. The sputtering combined with UHV heating has led to a non-optimized starting GaAs(100)(6×6) surface with a small island size. The formed GaAs(100)(1×1)-InO layer appears to follow the initial large-scale morphology. The inset STM image is zoomed in (5 nm × 5nm) for (1×1)-InO, showing a local ordering which is also consistent with sharp (1×1) LEED patterns. [Reprinted with permission from Ref. 64, Adv. Mater. Int. **4**, 1700722 (2017). © 2017 by the Wiley.]

FIG. 20. Effects of crystalline oxidized GaAs(100)c(4×2)-InO on photoluminescence (PL) intensity and the Ga3d core-level spectrum measured from Al_2O_3/GaAs. The Ga3d spectra show that the c(4×2)-InO interface layer decreases the oxidation-induced changes in the Ga bonding structure. This spectral change in Ga3d can be linked to the decrease in defect density at the Al_2O_3/GaAs with the c(4×2)-InO interface structure, as the PL-intensity comparison indicates, if the Ga oxidation leads to the formation of dangling bonds, for example. (See also the text in Section IV). [Reprinted with permission from Ref. 59, Phys. Chem. Chem. Phys. **17**, 7060 (2015). © 2015 the Royal Society of Chemistry.]

FIG. 21. XPS characterization for the crystalline $In_{0.53}Ga_{0.47}As$(100)(100)(3×1)-O surface. Electrical characterization of $HfO_2/In_{0.53}Ga_{0.47}As$ capacitors shows that interface defect density as well as border-trap density can be decreased by incorporating the crystalline oxidized layers into the interface. [Reprinted with permission from Ref. 63, J. Appl. Phys. **121**, 125302 (2017). © 2017 by the American Institute of Physics.]

FIG. 22. STM images from the crystalline oxidized GaSb(100)(4×2)-In surface, causing the formation of (1×3)-InO phase coexisting with (4×2)-In areas. The electron density is more localized in the (1×3)-InO areas appearing as bright dots in the rows, which resembles the InAs(100)(3×1)-O system (see Section VAa) where the strain might be relieved through the formation of a corrugated structure. The STS curves indicate that (1×3)-InO structure does not have gap levels. [Reprinted with permission from Ref. 60, Appl. Phys. Lett. **107**, 061601 (2015). © 2015 by the American Institute of Physics.]

FIG. 23. (a) and (b) Synchrotron XPS results for the oxidation of pure GaSb(100) causing defect clusters. The defects can be linked to increasing the Ga^{3+} oxidation state (G2) and Sb-Sb type component (S2). (c) STM image showing the defect clusters which can be categorized into A type along the intial dimer rows and B type which interconnect the dimer rows. (d) Atomic models for the clean GaSb(100)(4×3) showing potential atomic sites (red arrows) where oxygen becomes incorporated. [Reprinted with permission from Ref. 213, Appl. Surf. Sci. **369**, 520 (2016). © 2016 the Elsevier.]

FIG. 24. Characterization of the GaN(0001) surface oxidized at 550 °C in O_2 pressure of 1.5×10^{-5} Torr. (a) LEED indicates $(3\sqrt{3}\times3\sqrt{3})$-R30° periodicity. (b) and (c) STM images from the oxidized GaN surface showing smooth islands with an ordered $(3\sqrt{3}\times3\sqrt{3})$-R30° type structure. (d) Possible atomic models determined by first-principles calculations for the oxidized GaN. [Reprinted with permission from Ref 46, J. Vac. Sci. Technol. B **24**, 2080 (2006). © 2014 by the American Vacuum Society.]

FIG. 25. LEED patterns from $Al_{0.25}Ga_{0.75}N$ after (a) native oxide without any cleaning, (b) heating at 550 °C in $N_2 + O_2$ flow of 45 sccm + 0.5 sccm, (c) heating 300 °C in plasma of $N_2 + O_2$ flow of 45 sccm + 0.5 sccm, and (d) heating 550 °C in plasma of $N_2 + O_2$ flow of 45 sccm + 0.5 sccm. Increasing the

substrate temperature from 300 ºC to 550 ºC during the plasma oxidation significantly increases a degree of crystalline order at the oxidized surface because in the pattern (c) the background intensity dominates while the pattern (d) shows the diffraction intensity similar to the starting crystal surface. [Reprinted with permission from Ref. 55, Appl. Phys. Lett. **105**, 141604 (2014). © 2014 by the American Institute of Physics.]

FIG. 26. Atomic models for the clean AlGaN surface and for the crystalline oxidized surface obeying electron counting (EC) rule, which means that the surface electron levels below the Fermi level in the valence band are completely filled with available valence electrons, while the electron levels in the conduction band above the Fermi level remain completely empty. Capacitance-voltage curves as a function of modulation frequency for Al_2O_3/AlGaN capacitors including the different AlGaN surface treatments corresponding to LEED images in Figure 25. The first step of capacitance around -10 V or -6 V is due to the 2D electron-gas formation at the epitaxial AlGaN/GaN interface while the second capacitance step corresponds to the Al_2O_3/AlGaN interface. The plasma oxidation (D) provides an increased slope and a decreased frequency dispersion around the depletion-region step, indicating a decrease in the interface defect density. [Reprinted with permission Ref. 55, Appl. Phys. Lett. **105**, 141604 (2014). © 2014 by the American Institute of Physics.]

FIG. 27. Examples of contemporary III-V devices which get a benefit from the surface passivation development. (a) Insulator gated HEMT, so-called MOSHEMT. [Left structure reprinted with permission from Ref. 232, IEEE Electr. Dev. Lett. **30**, 5 (2009). © 2009 the IEEE. Right structure reprinted with permission from Ref. 219, Appl. Phys. Lett. **86**, 063501 (2005). © 2005 by the American Institute of Physics.] (b) 1.55 μm photodiode or detector. [Reprinted with permission from Ref. 243, IEEE Transact.

Electr. Dev. **35**, 2349 (1988). © 2009 the IEEE.] (c) MicroLED structure and device image. [Reprinted with permission from Ref. 247, Appl. Phys. Lett. **116**, 251104 (2020). © 2020 by the American Institute of Physics.]

FIG. 28. Wet chemical cleaning and UHV treatments were combined to test whether the crystalline oxidation could be included in the III-V passivation processes in a simplified way. LEED patterns from HCl+IPA etched InSb(111)B, which was transferred via air (about 2 min), after the vacuum heating around 300 ºC (a) and 400 ºC (b) show the fingerprint (2×2) and (3×3) reconstructions (see Section VAb) for a clean and ordered InSb(111)B. Molecular hydrogen (H_2) exposure (1×10^{-5} mbar) during 400 ºC heating improved (3×3) LEED pattern. Two-dimensional terrace-step structure with a long-range order is observed in the STM images (c) and (d). [Reprinted and adapted with permission from Ref. 65, Sci. Rep. 8, 14382 (2018). © 2018 by the Springer Nature.]

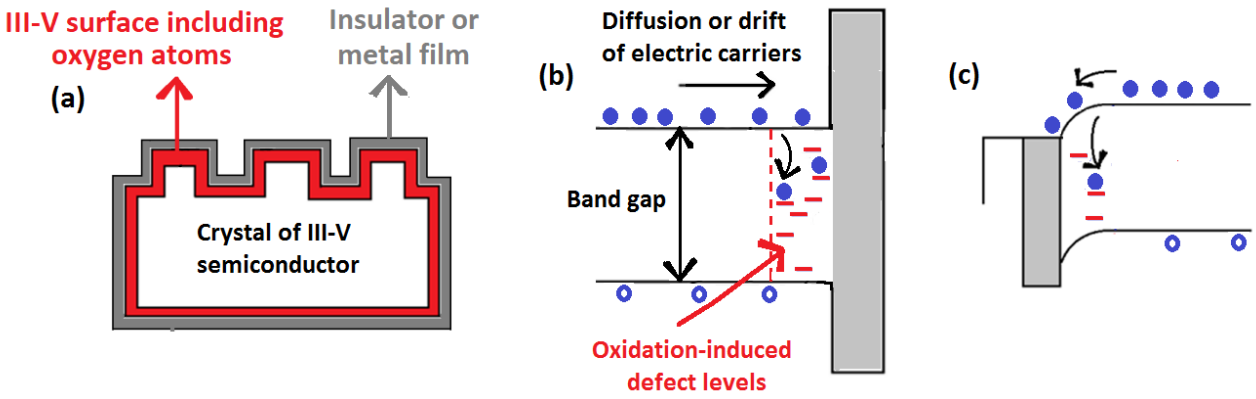
III-V surface including oxygen atoms
Insulator or metal film
(a)
Crystal of III-V semiconductor
(b)
Diffusion or drift of electric carriers
Band gap
Oxidation-induced defect levels
(c)

FIG. 1.

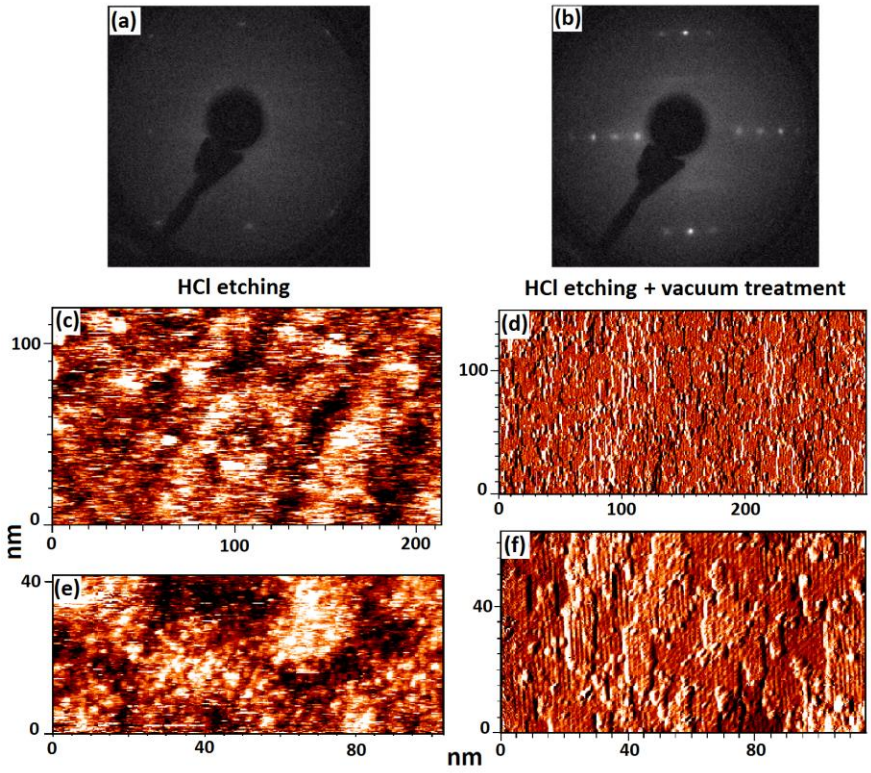
(a)
(b)
HCl etching
HCl etching + vacuum treatment
(c)
(d)
(e)
(f)
100
0
200
40
80
nm

FIG. 2.

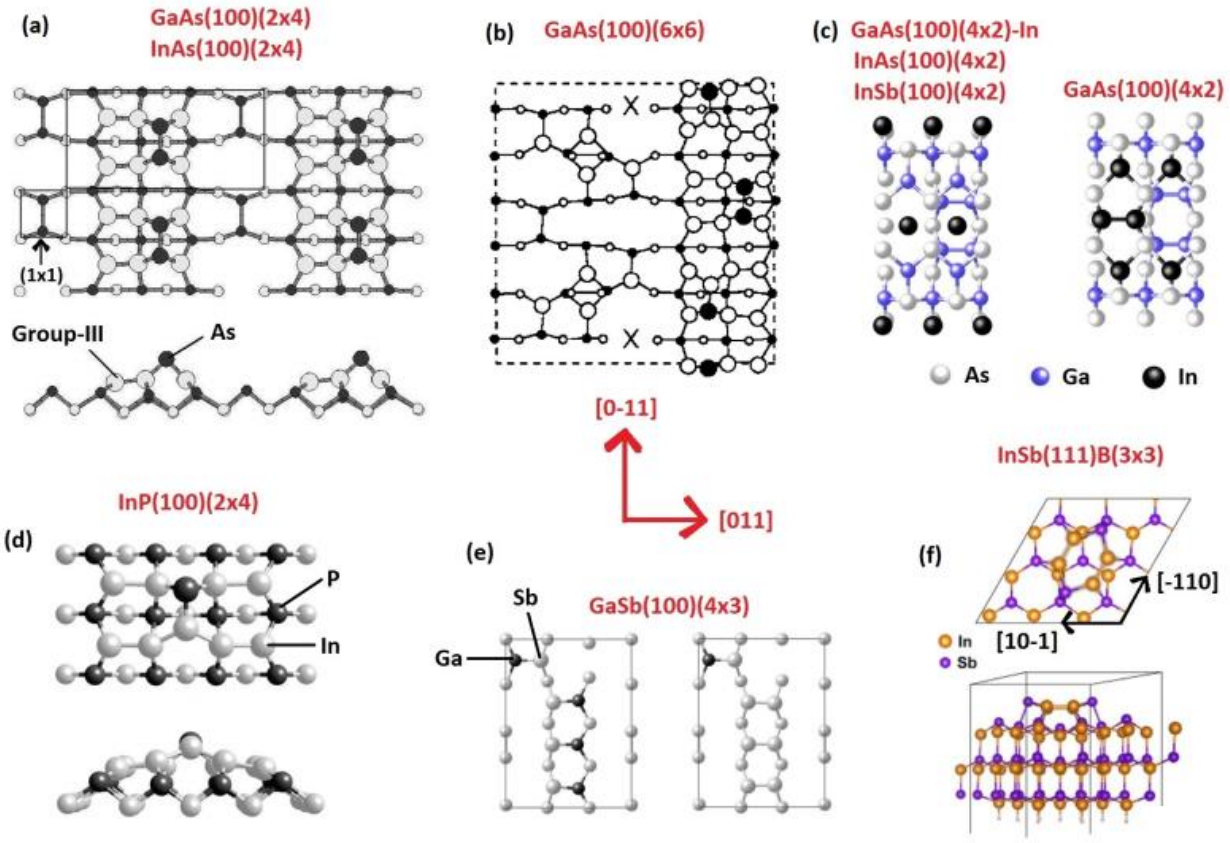
(a)
GaAs(100)(2x4)
InAs(100)(2x4)
(1x1)
Group-III
As
(b)
GaAs(100)(6x6)
X
X
[0-11]
[011]
(c)
GaAs(100)(4x2)-In
InAs(100)(4x2)
InSb(100)(4x2)
GaAs(100)(4x2)
As
Ga
In
(d)
InP(100)(2x4)
P
In
(e)
Sb
GaSb(100)(4x3)
Ga
(f)
InSb(111)B(3x3)
[-110]
[10-1]
In
Sb

FIG. 3.

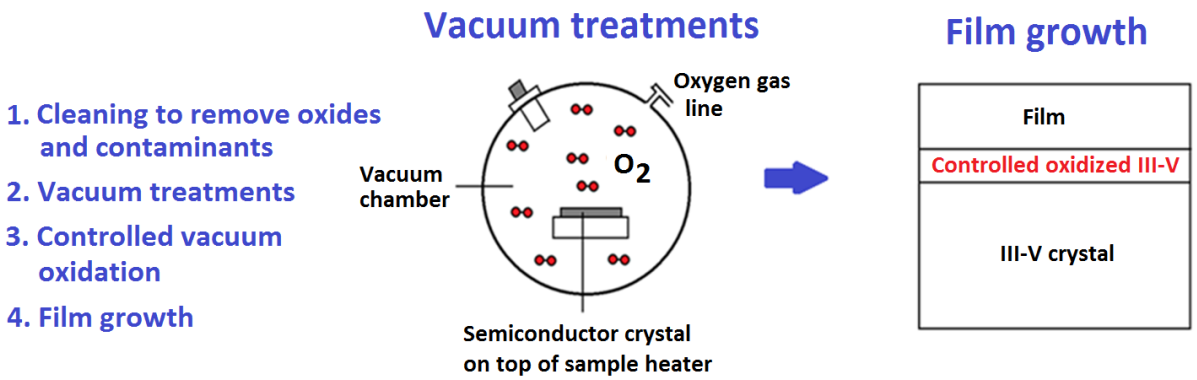
1. Cleaning to remove oxides and contaminants
2. Vacuum treatments
3. Controlled vacuum oxidation
4. Film growth
Vacuum treatments
Oxygen gas line
Vacuum chamber
O_2
Semiconductor crystal on top of sample heater
Film growth
Film
Controlled oxidized III-V
III-V crystal

FIG. 4.

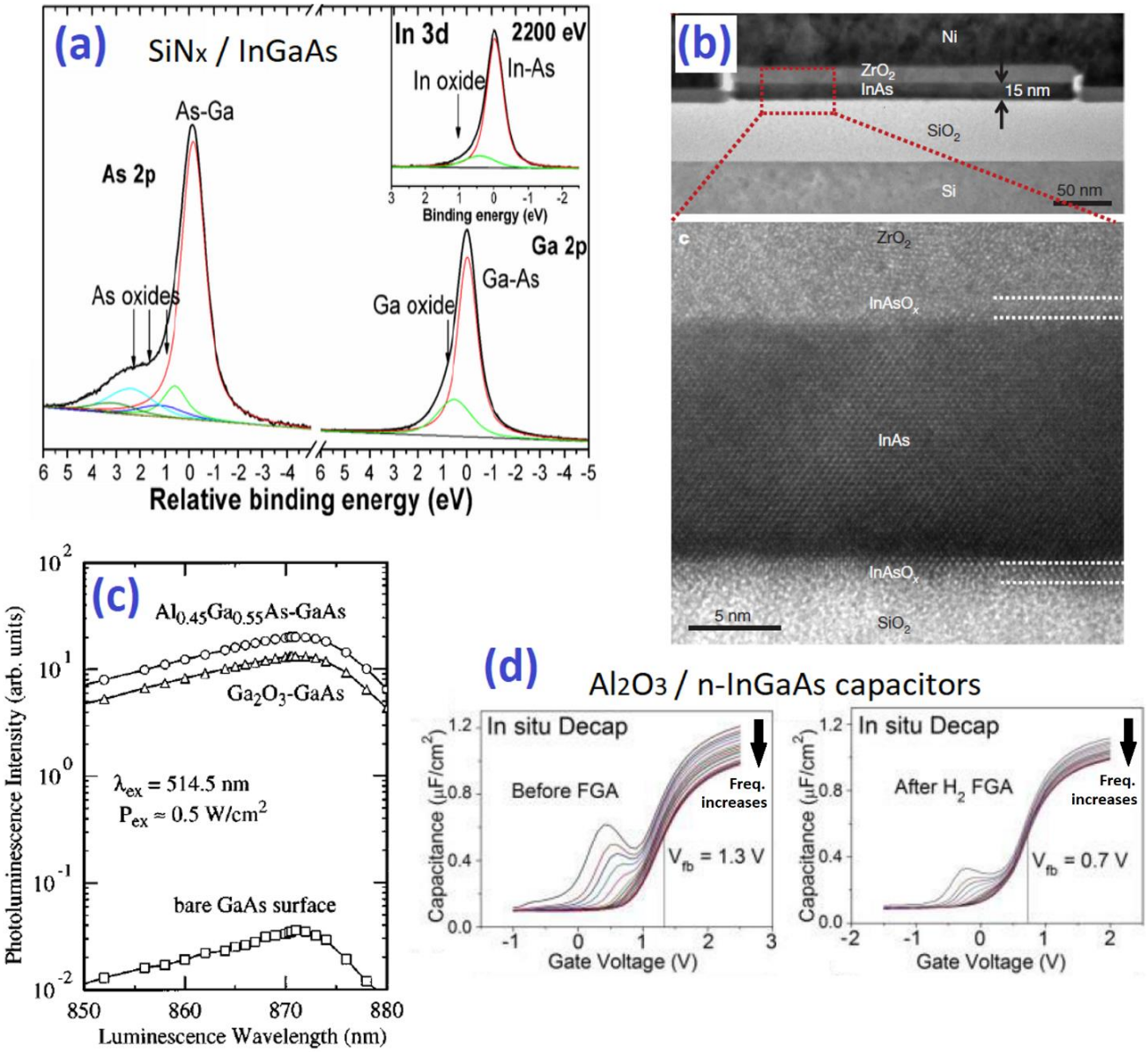
(a)
SiNx / InGaAs
In 3d
2200 eV
In oxide
In-As
Binding energy (eV)
As-Ga
As 2p
As oxides
Ga 2p
Ga-As
Ga oxide
Relative binding energy (eV)
(b)
Ni
ZrO2
InAs
15 nm
SiO2
Si
50 nm
c
ZrO2
InAsOx
InAs
InAsOx
5 nm
SiO2
(c)
Al0.45Ga0.55As-GaAs
Ga2O3-GaAs
λex = 514.5 nm
Pex ≈ 0.5 W/cm2
bare GaAs surface
Photoluminescence Intensity (arb. units)
Luminescence Wavelength (nm)
(d)
Al2O3 / n-InGaAs capacitors
In situ Decap
Before FGA
Freq. increases
Vfb = 1.3 V
Capacitance (μF/cm2)
Gate Voltage (V)
In situ Decap
After H2 FGA
Freq. increases
Vfb = 0.7 V
Capacitance (μF/cm2)
Gate Voltage (V)

FIG. 5.

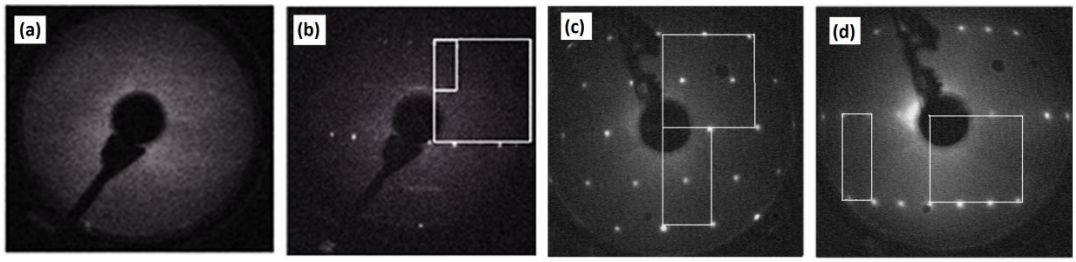

FIG. 6.

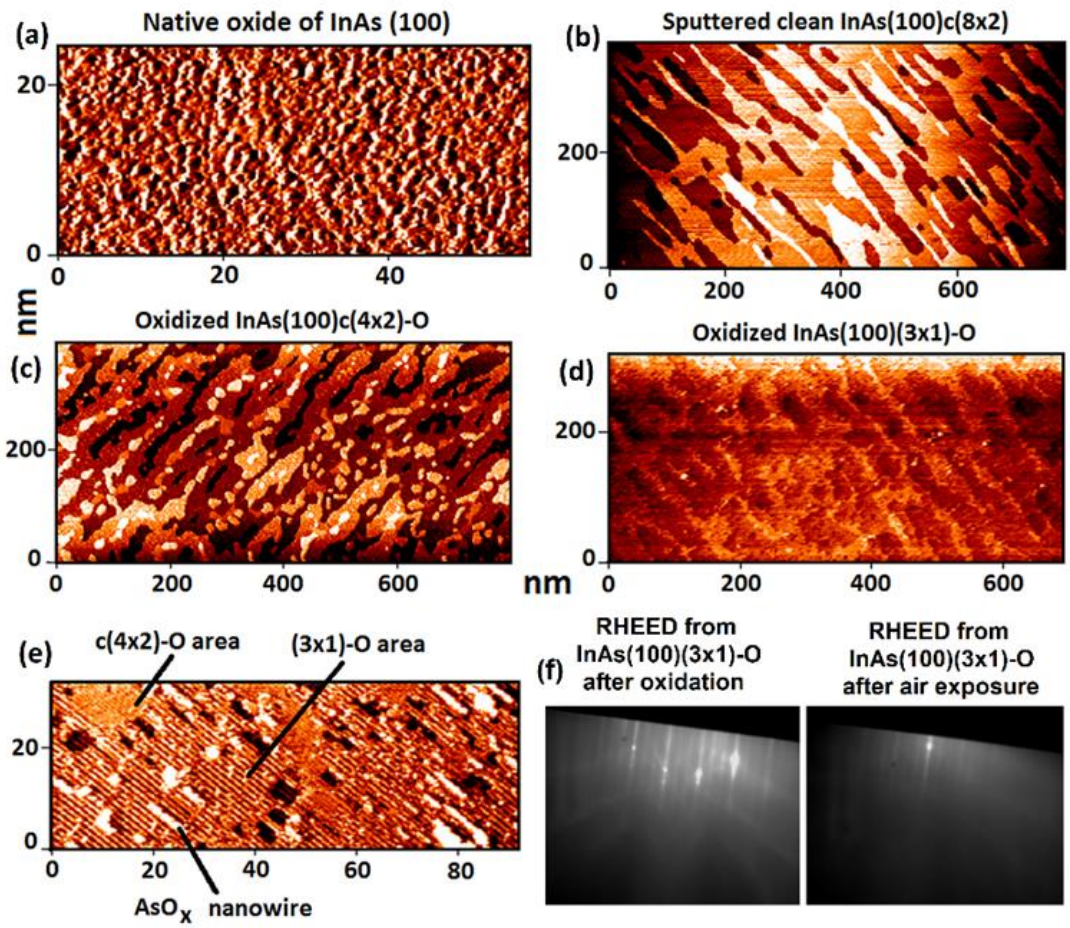
(a)
Native oxide of InAs (100)
(b)
Sputtered clean InAs(100)c(8x2)
Oxidized InAs(100)c(4x2)-O
(c)
Oxidized InAs(100)(3x1)-O
(d)
nm
(e)
c(4x2)-O area
(3x1)-O area
AsOx
nanowire
(f)
RHEED from InAs(100)(3x1)-O after oxidation
RHEED from InAs(100)(3x1)-O after air exposure

FIG. 7.

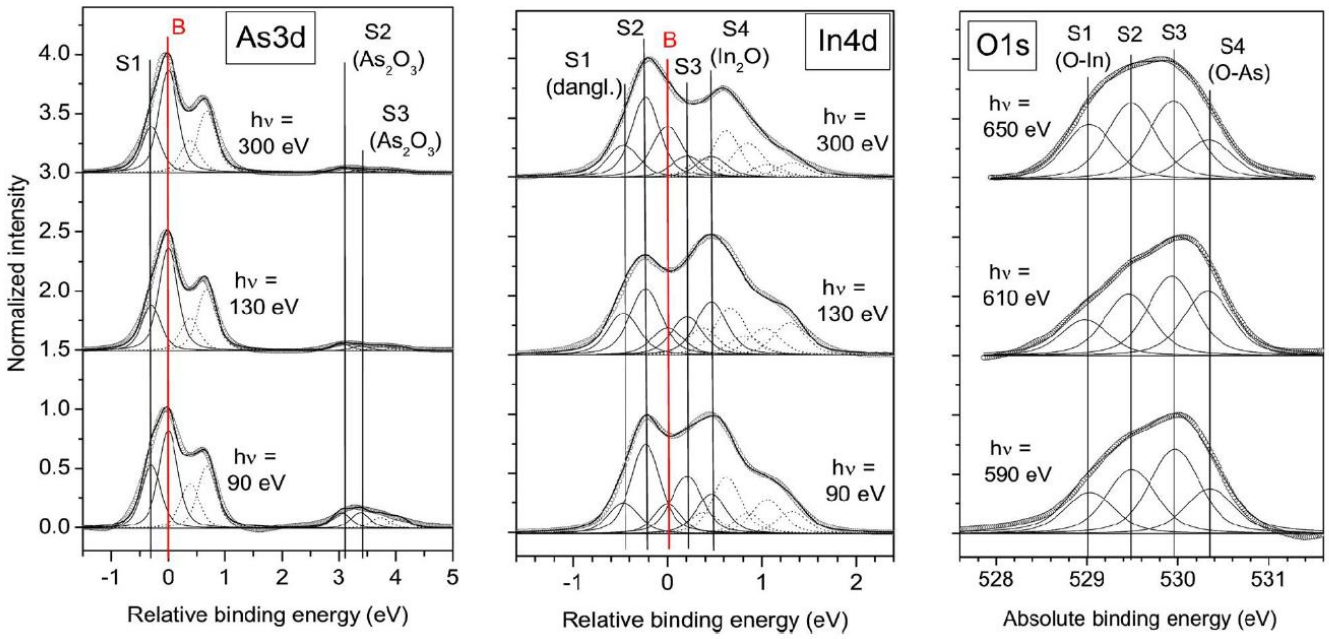
As3d
B
S1
S2
(As2O3)
S3
(As2O3)
hν =
300 eV
hν =
130 eV
hν =
90 eV
Normalized intensity
Relative binding energy (eV)
In4d
S2
B
S4
(In2O)
S1
(dangl.)
S3
hν =
300 eV
hν =
130 eV
hν =
90 eV
Relative binding energy (eV)
O1s
S1
(O-In)
S2
S3
S4
(O-As)
hν =
650 eV
hν =
610 eV
hν =
590 eV
Absolute binding energy (eV)

FIG. 8.

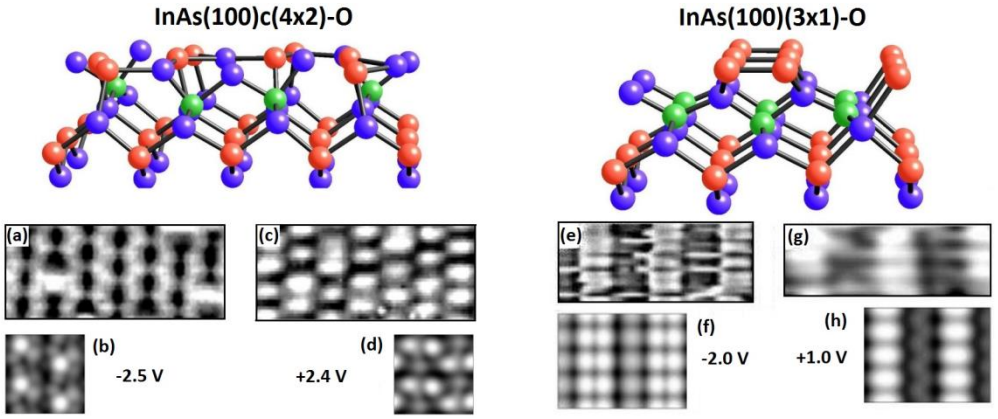

FIG. 9.

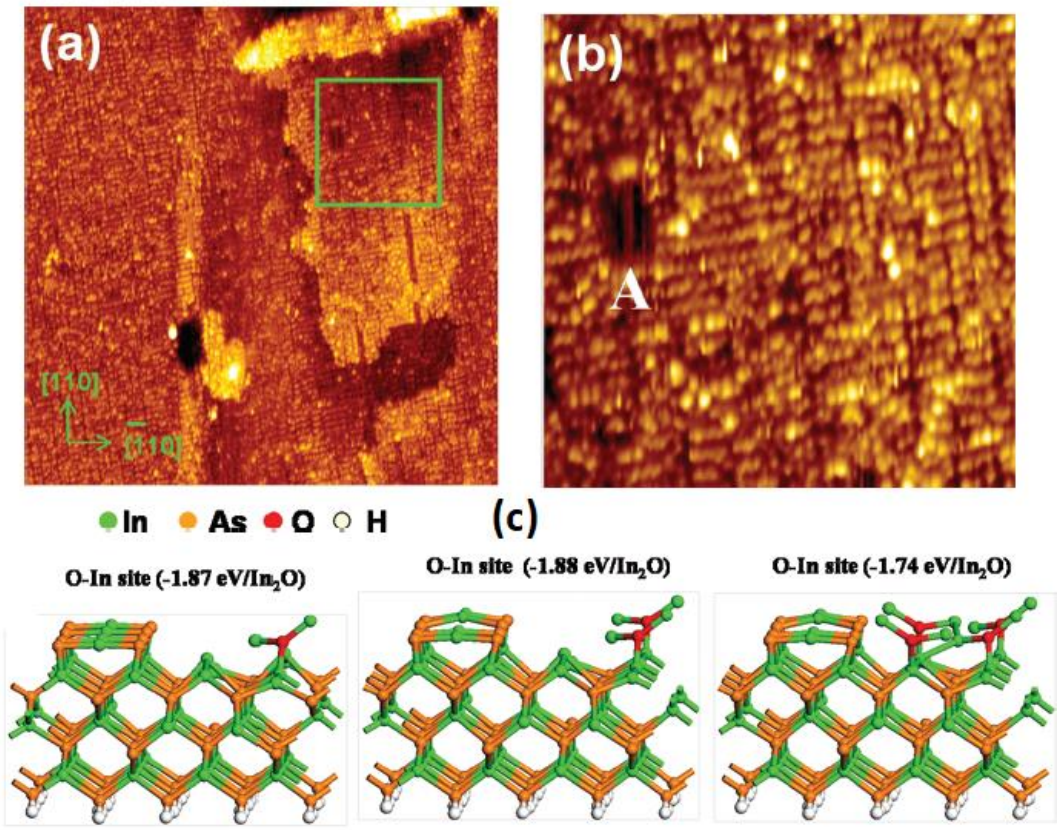
(a)
[110]
[1̄10]
(b)
A
In
As
O
H
(c)
O-In site (-1.87 eV/In2O)
O-In site (-1.88 eV/In2O)
O-In site (-1.74 eV/In2O)

FIG. 10.

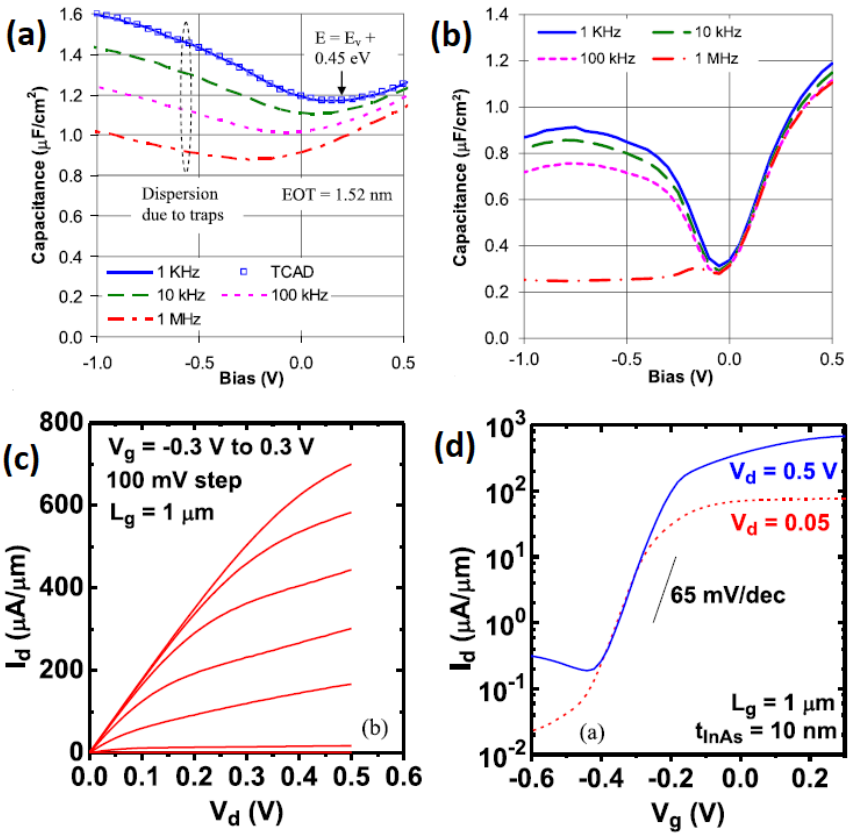
(a)
E = Ev + 0.45 eV
Dispersion due to traps
EOT = 1.52 nm
1 KHz
TCAD
10 kHz
100 kHz
1 MHz
Capacitance (μF/cm²)
Bias (V)
(b)
1 KHz
10 kHz
100 kHz
1 MHz
Capacitance (μF/cm²)
Bias (V)
(c)
Vg = -0.3 V to 0.3 V
100 mV step
Lg = 1 μm
(b)
Id (μA/μm)
Vd (V)
(d)
Vd = 0.5 V
Vd = 0.05
65 mV/dec
Lg = 1 μm
tInAs = 10 nm
(a)
Id (μA/μm)
Vg (V)

FIG. 11.

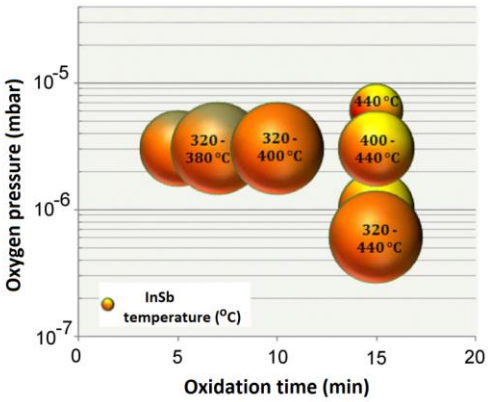
Oxygen pressure (mbar)
10-5
10-6
10-7
0
5
10
15
20
Oxidation time (min)
320 - 380 °C
320 - 400 °C
440 °C
400 - 440 °C
320 - 440 °C
InSb temperature (°C)

FIG. 12.

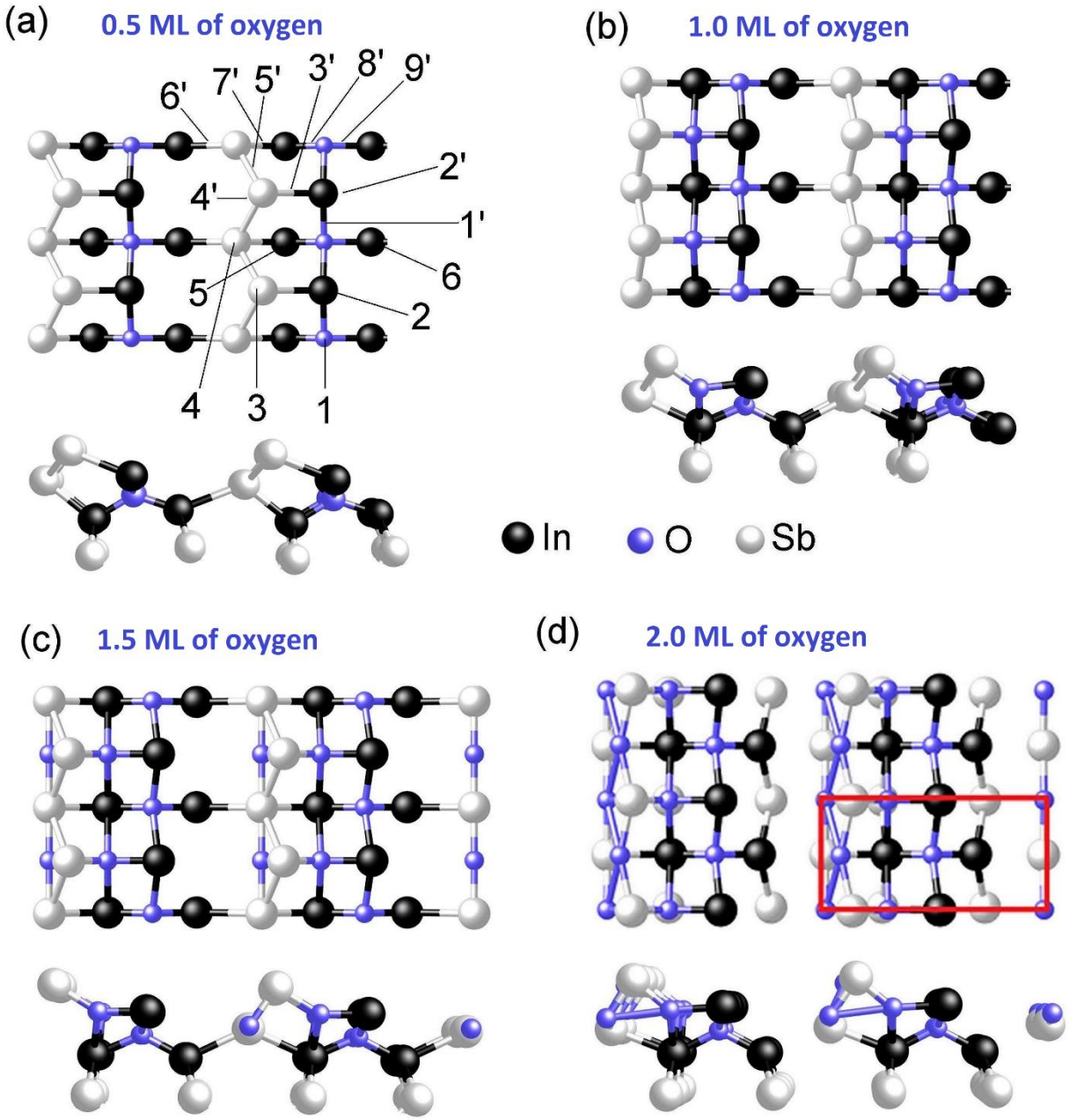
(a)
0.5 ML of oxygen
6'
7'
5'
3'
8'
9'
2'
4'
1'
6
5
2
4
3
1
(b)
1.0 ML of oxygen
In
O
Sb
(c)
1.5 ML of oxygen
(d)
2.0 ML of oxygen

FIG. 13.

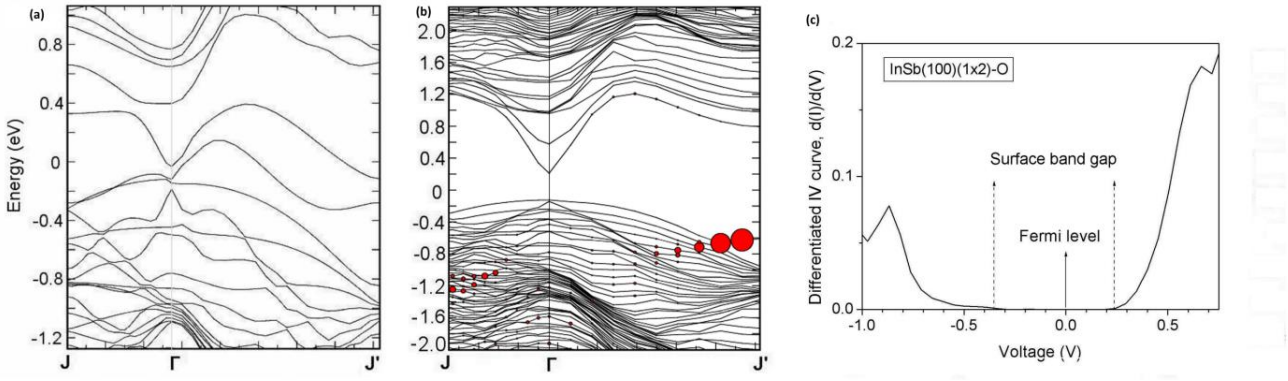
(a)
(b)
(c)
Energy (eV)
J
Γ
J'
InSb(100)(1x2)-O
Surface band gap
Fermi level
Differentiated IV curve, d(I)/d(V)
Voltage (V)

FIG. 14.

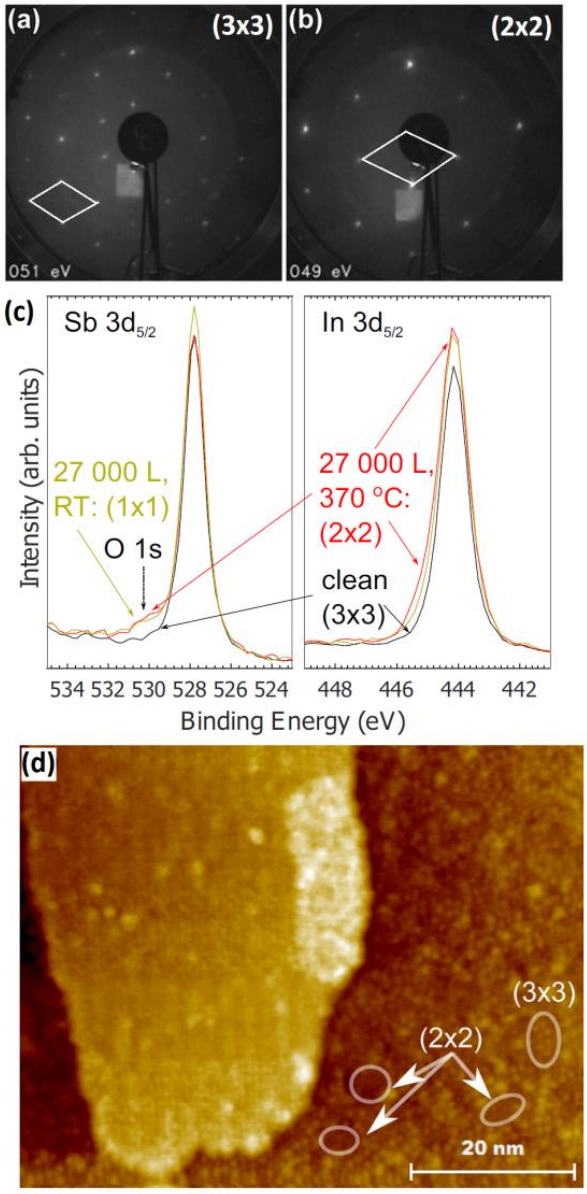
(a)
(3x3)
051 eV
(b)
(2x2)
049 eV
(c)
Sb 3d5/2
In 3d5/2
Intensity (arb. units)
27 000 L,
RT: (1x1)
O 1s
27 000 L,
370 °C:
(2x2)
clean
(3x3)
534 532 530 528 526 524
448 446 444 442
Binding Energy (eV)
(d)
(3x3)
(2x2)
20 nm

FIG. 15.

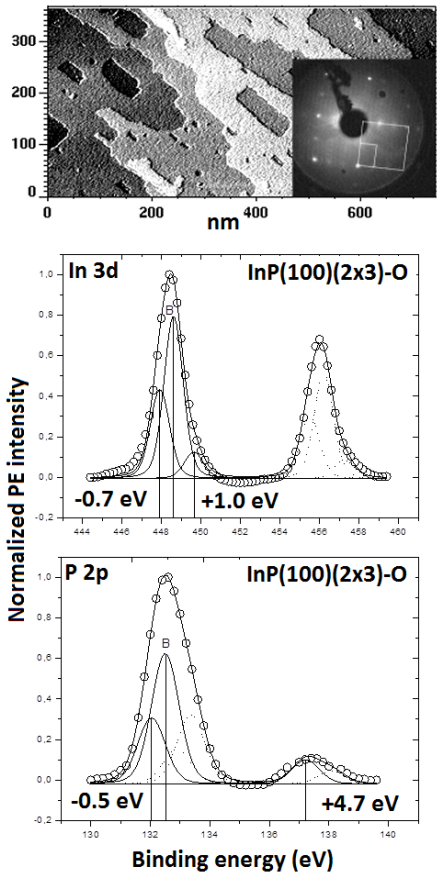
300
200
100
0
0
200
400
600
nm
In 3d
InP(100)(2x3)-O
B
-0.7 eV
+1.0 eV
P 2p
InP(100)(2x3)-O
B
-0.5 eV
+4.7 eV
Normalized PE intensity
Binding energy (eV)

FIG. 16.

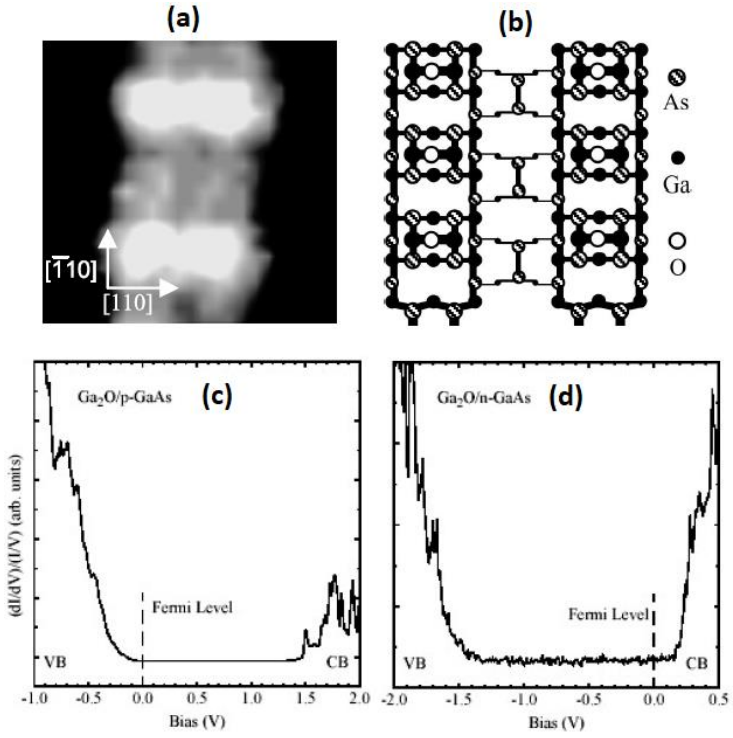
(a)
(b)
[1̄10]
[110]
As
Ga
O
Ga2O/p-GaAs
(c)
Fermi Level
VB
CB
(dI/dV)/(I/V) (arb. units)
Bias (V)
Ga2O/n-GaAs
(d)
Fermi Level
VB
CB
Bias (V)

FIG. 17.

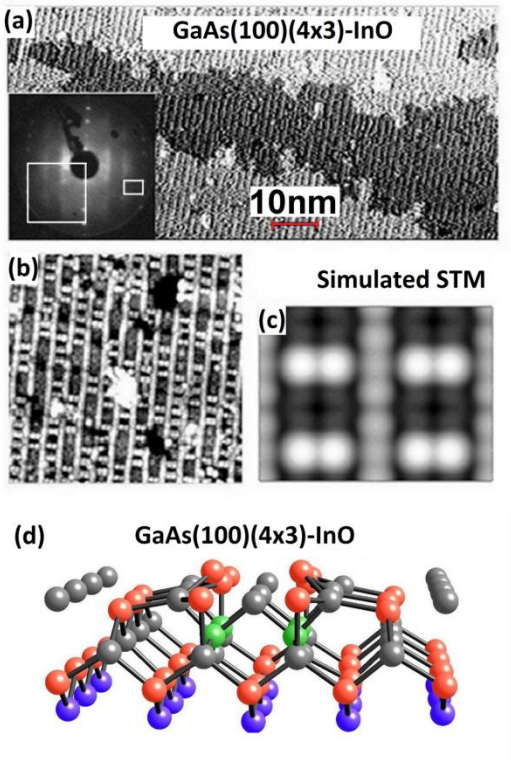

FIG. 18.

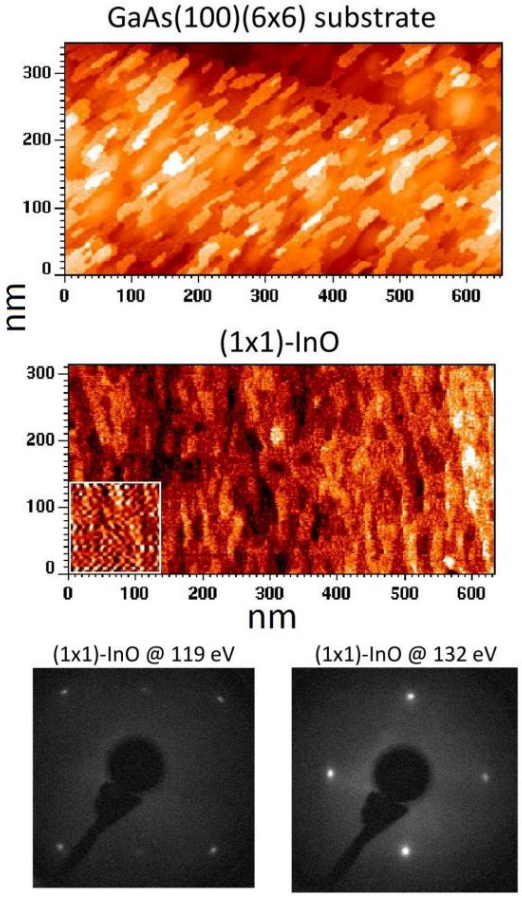
GaAs(100)(6x6) substrate
300
200
100
0
0
100
200
300
400
500
600
nm
(1x1)-InO
300
200
100
0
0
100
200
300
400
500
600
nm
(1x1)-InO @ 119 eV
(1x1)-InO @ 132 eV

FIG. 19.

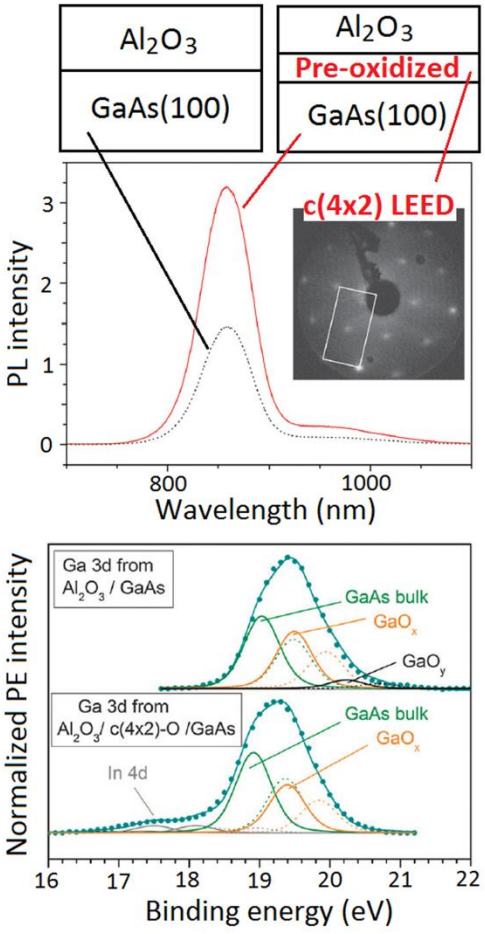
Al2O3
GaAs(100)
Al2O3
Pre-oxidized
GaAs(100)
c(4x2) LEED
PL intensity
0
1
2
3
800
1000
Wavelength (nm)
Ga 3d from
Al2O3 / GaAs
GaAs bulk
GaOx
GaOy
Ga 3d from
Al2O3/ c(4x2)-O /GaAs
GaAs bulk
GaOx
In 4d
Normalized PE intensity
16
17
18
19
20
21
22
Binding energy (eV)

FIG. 20.

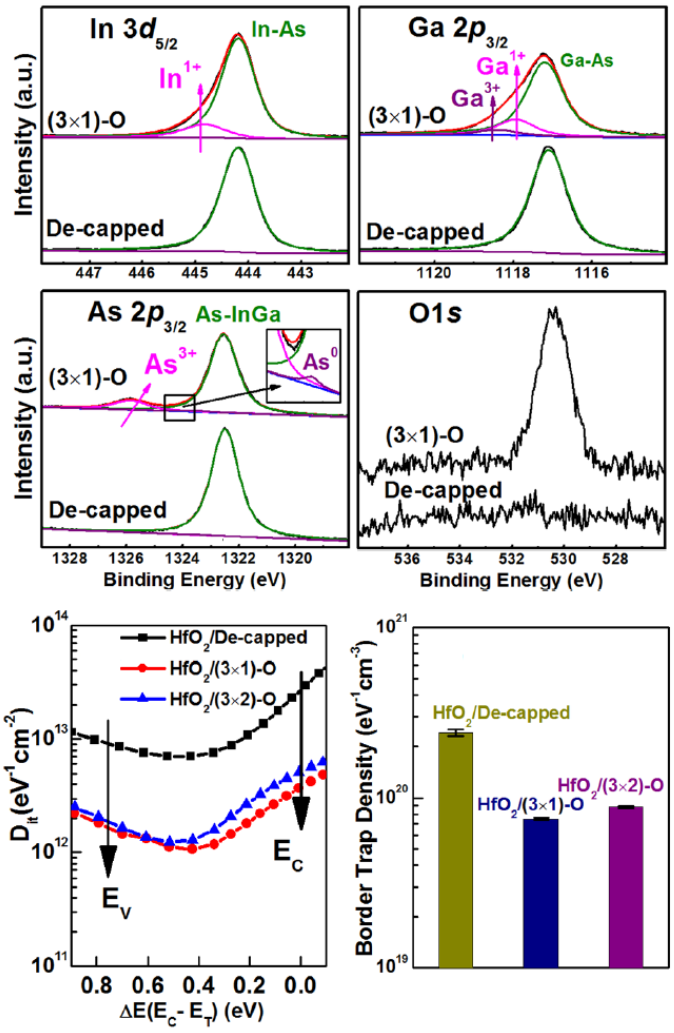
In 3d5/2
In-As
In1+
(3×1)-O
De-capped
Intensity (a.u.)
447 446 445 444 443
Ga 2p3/2
Ga1+
Ga-As
Ga3+
(3×1)-O
De-capped
1120 1118 1116
As 2p3/2
As-InGa
As3+
As0
(3×1)-O
De-capped
Intensity (a.u.)
1328 1326 1324 1322 1320
Binding Energy (eV)
O1s
(3×1)-O
De-capped
536 534 532 530 528
Binding Energy (eV)
HfO2/De-capped
HfO2/(3×1)-O
HfO2/(3×2)-O
Dit (eV-1cm-2)
EV
EC
0.8 0.6 0.4 0.2 0.0
ΔE(EC- ET) (eV)
Border Trap Density (eV-1cm-3)
HfO2/De-capped
HfO2/(3×1)-O
HfO2/(3×2)-O

FIG. 21.

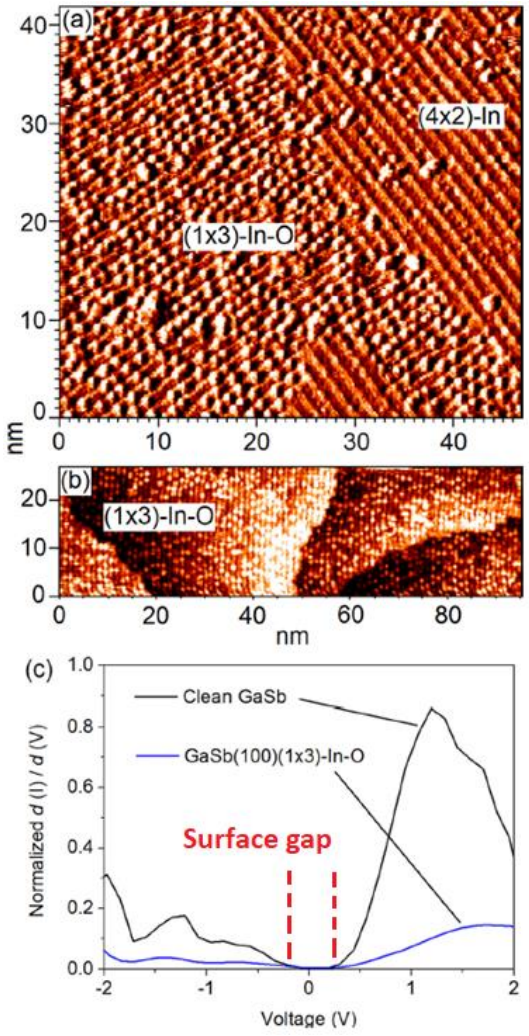
(a)
(4x2)-In
(1x3)-In-O
nm
(b)
(1x3)-In-O
nm
(c)
Clean GaSb
GaSb(100)(1x3)-In-O
Surface gap
Normalized d (I) / d (V)
Voltage (V)

FIG. 22.

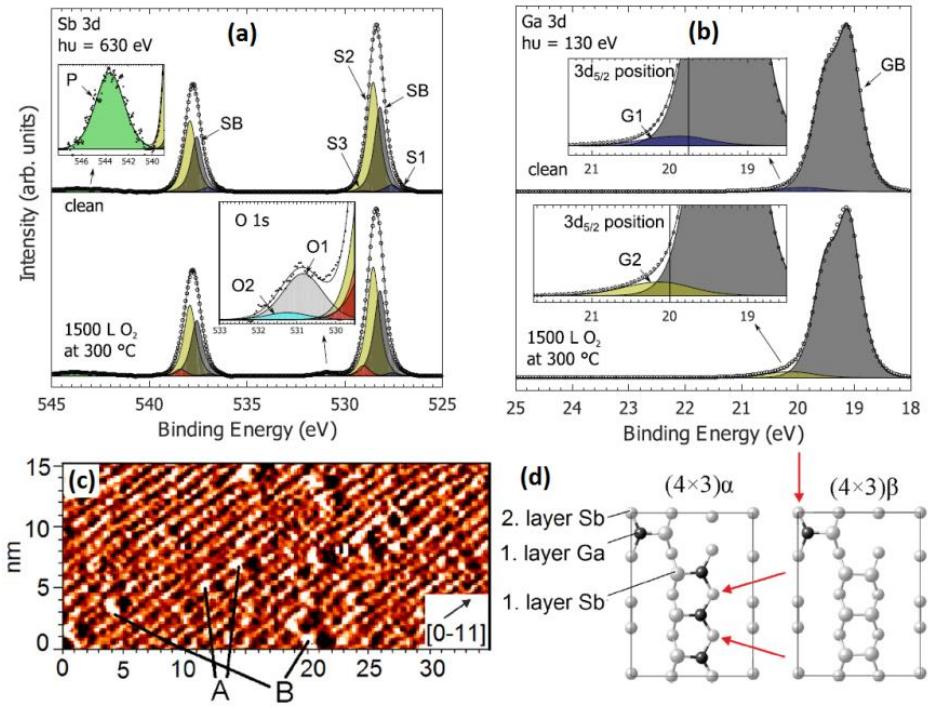
Sb 3d
hu = 630 eV
(a)
P
SB
S2
SB
S3
S1
clean
O 1s
O1
O2
1500 L O2
at 300 °C
Intensity (arb. units)
545 540 535 530 525
Binding Energy (eV)
Ga 3d
hu = 130 eV
(b)
3d5/2 position
G1
GB
clean
21 20 19
3d5/2 position
G2
21 20 19
1500 L O2
at 300 °C
25 24 23 22 21 20 19 18
Binding Energy (eV)
(c)
15
10
5
0
nm
0 5 10 15 20 25 30
A
B
[0-11]
(d)
(4×3)α
(4×3)β
2. layer Sb
1. layer Ga
1. layer Sb

FIG. 23.

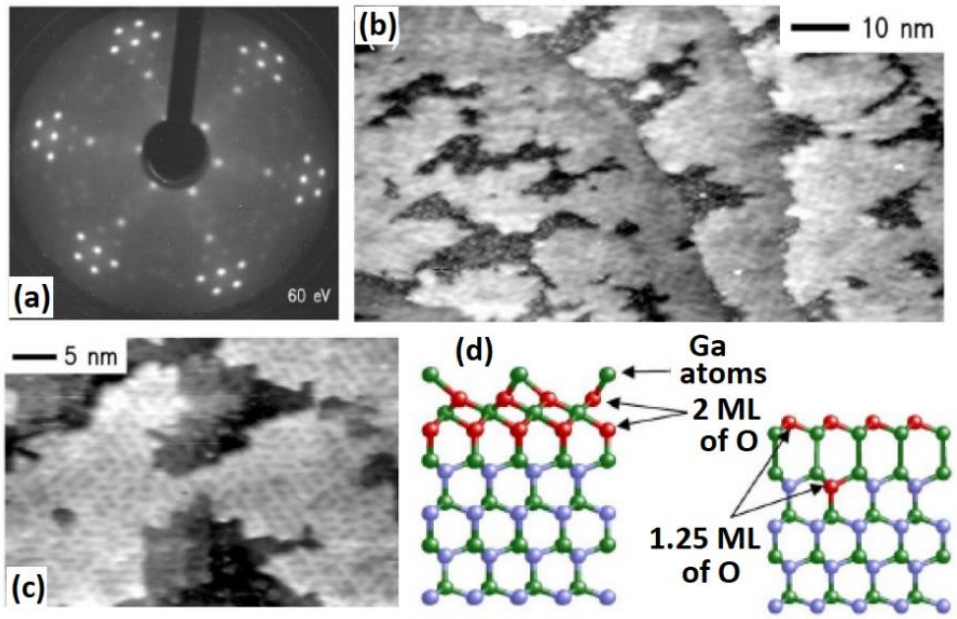

FIG. 24.

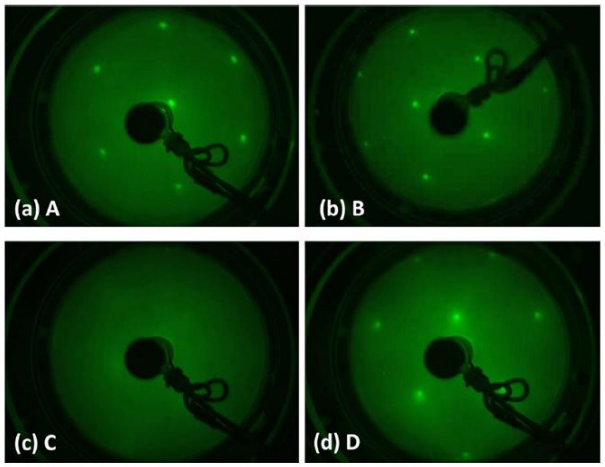

FIG. 25.

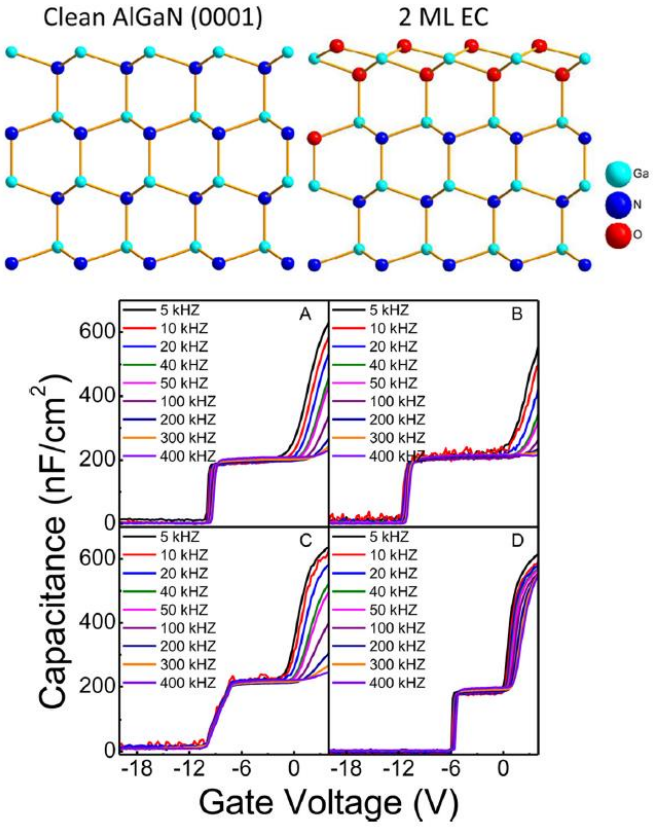
Clean AlGaN (0001)
2 ML EC
Ga
N
O
A
B
C
D
5 kHZ
10 kHZ
20 kHZ
40 kHZ
50 kHZ
100 kHZ
200 kHZ
300 kHZ
400 kHZ
Capacitance (nF/cm^2)
Gate Voltage (V)
0
200
400
600
-18
-12
-6
0

FIG. 26.

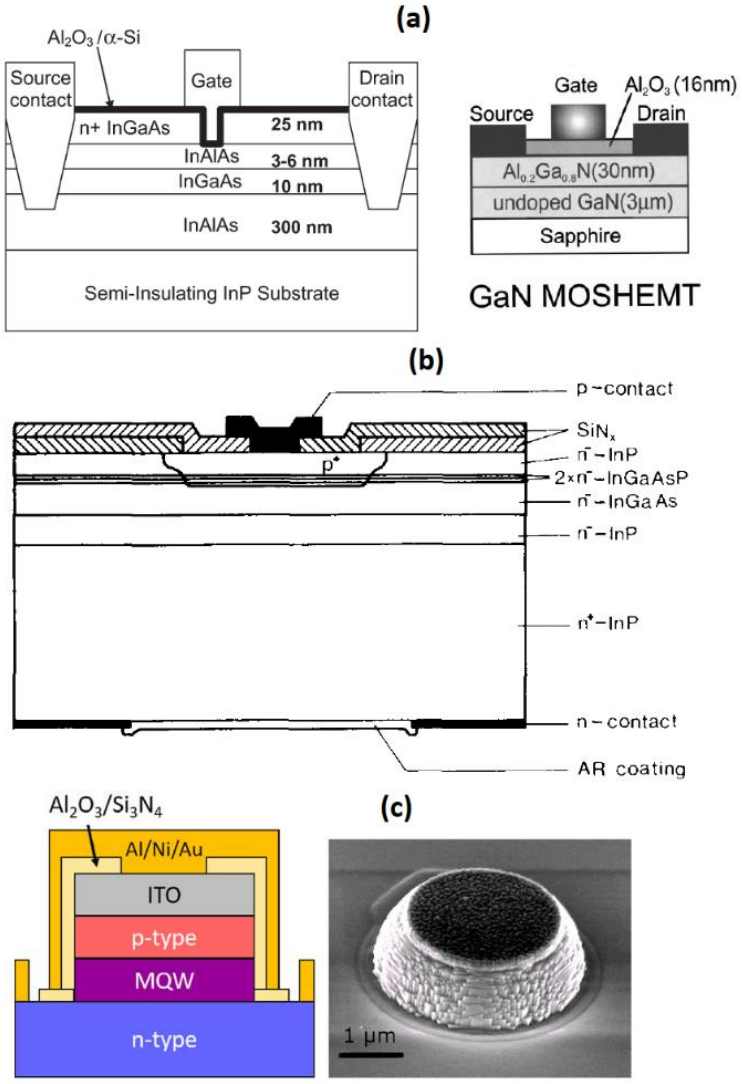
(a)
Al_2O_3 /α-Si
Source contact
Gate
Drain contact
n+ InGaAs
25 nm
InAlAs
3-6 nm
InGaAs
10 nm
InAlAs
300 nm
Semi-Insulating InP Substrate
Gate
Al_2O_3 (16nm)
Source
Drain
$Al_{0.2}Ga_{0.8}N$(30nm)
undoped GaN(3μm)
Sapphire
GaN MOSHEMT
(b)
p−contact
SiN_x
n⁻−InP
2×n⁻−InGaAsP
n⁻−InGaAs
n⁻−InP
p⁺
n⁺−InP
n−contact
AR coating
Al_2O_3/Si_3N_4
Al/Ni/Au
ITO
p-type
MQW
n-type
(c)
1 μm

FIG. 27.

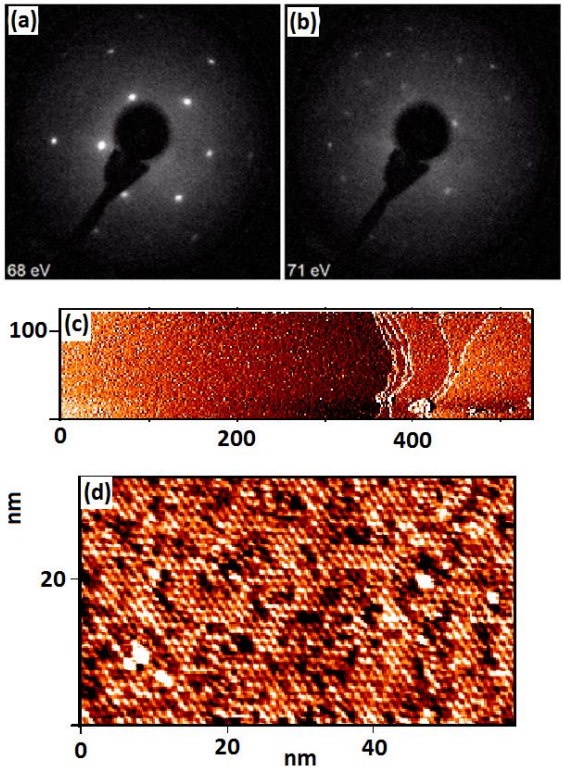

FIG. 28.