Design and Implementation of Selective Active EMI Filter with Digital Resonant Controller

*Hongwu Peng, Balaji Narayanasamy, Asif Imran Emon, Zhao Yuan, Mustafeez Ul Hassan, and Fang Luo
University of Arkansas, Fayetteville, AR, USA
*hp013@uark.edu

***Abstract*—In the power electronics equipment, passive EMI filters occupy up to 30% of system's volume and weight. In order to reduce the size of passive EMI filter in the power electronics system, active EMI filters (AEF) is introduced. With the AEF approaches, the size of the passive component within the EMI filter can be reduced by more than 50%. The higher attenuation achieved by AEFs, the more size reduction can be obtained through AEFs methodology. However, the performance of AEF with feedback control is limited to around 24 dB attenuation in the reported work. New methodology needs to be found to push forward the performance. In this study, a novel digital active EMI filter (DAEF) with the resonant controller, which provides ultra high-gain at frequencies of interest, is demonstrated for DM noise attenuation. The experimental test results show that the proposed EMI filter has 45 dB more attenuation at 150 kHz than the conventional passive EMI filter, which is also the highest attenuation reported in the AEF literature.**

***Index Terms*—Conducted emission, digital active EMI filter, resonant controller, Field Programmable Gate Array (FPGA)**

I. Introduction

In order to comply with certain conducted emission standard, the passive EMI filter is needed for the power electronics equipment [1]–[6]. In most of the power converter with semiconductor switches [7]–[11], the passive EMI filter occupies up to 30% of system's size [12]–[17]. Thus, AEF could be utilized to reduce the size of passives [18]–[25]. There are different approaches for the classification of AEFs: noise sensing methodology, noise cancellation circuits, and active circuits. AEFs with feedback [26]–[28] and feedforward [29], [30] have been evaluated in past works, which provides an attenuation of 20 to 30 dB. By combining feedback and feedforward implementation together [28], two-stage AEFs have pushed the attenuation of AEFs to more than 40 dB. However, two-stage AEFs adds to system complexity as well as volume of passive component. Owning to the growth of controller's computing speed, DAEFs [31]–[34] that use DSP/FPGAs have been demonstrated. This paper proposes a new implementation of single -stage AEF, which provides higher attenuation than any previous works.

The voltage-sensing current-cancellation (VSCC) feedback AEF with digital resonant controller is shown in Fig. 1aa. The system comprises of the noise sensing circuit, the Analog-to-Digital Converter (ADC), the DSP/FPGA, the Digital-to-Analog Converter (DAC), the active circuit, the main passives, and the compensation circuitry. The DSP/FPGA will not be present in an analog-only implementation. The main limitation to the performance of any AEF with feedback compensation is stability. The stability is mainly influenced by the phase shift introduced by the noise-sensing stage [27] and the noise-processing stage. Particularly, in converters with ac voltage, a second-order high-pass filter is required to separate the sensed noise from the fundamental voltage or current signal. This results in reduced attenuation of the AEF and additional compensation network. Some compensation networks require high-voltage capacitors, thus reducing the volumetric benefits of using an active EMI filter. This limitation is applicable to both analog and digital AEF. In [35] showed how the processing delay in digital AEF affects the attenuation. In [34], it was shown that the previous switching cycle noise could be used to compensate for noise in the next switching cycle to avoid the delay. However, attenuation of only 24 dB could be achieved in the process. This paper proposes an improved digital active EMI filter that uses the resonant controller, which achieves improved attenuation without increasing the volume overhead from additional high-voltage components.

Proportional resonant (PR) controller [36], [37] has been widely used in grid-connected inverters, which provides superior performance than conventional proportional-integral (PI) controller in tracking fixed frequency signals. Ideally, the resonant part of the PR controller provides infinite gain on the frequency of interest, while provides no gain and phase at other frequencies. Thus, the resonant controller will be perfectly suitable for the VSCC DAEF application. However, CISPR 22 [38] class B conducted noise limits, which is widely used in the residential environment, define EMI test frequency range from 150 kHz to 30 MHz. If the resonant controller is to be implemented in the DAEF system, the resonant frequency should be set to be a few 100s of kHz, while digital controller discretization frequency should be at least a few 10s of MHz for fulfilling the speed requirement. Thus, FPGA instead of DSP is to be used for the ultra-high frequency control. The structure of the resonant controller is shown in Fig. 1b, multiple resonant controllers are used in parallel at different frequencies for canceling EMI noise on different frequencies.

The contributions of this work are as follows. A novel digital AEF that utilizes both VSCC topology and the resonant controller is proposed, the stability design of the implementation is demonstrated. The discretization and modeling of the resonant controller based VSCC AEF are demonstrated, and the design methodology for proposed implementation is included. By utilizing the resonant controller in the FPGA control system,

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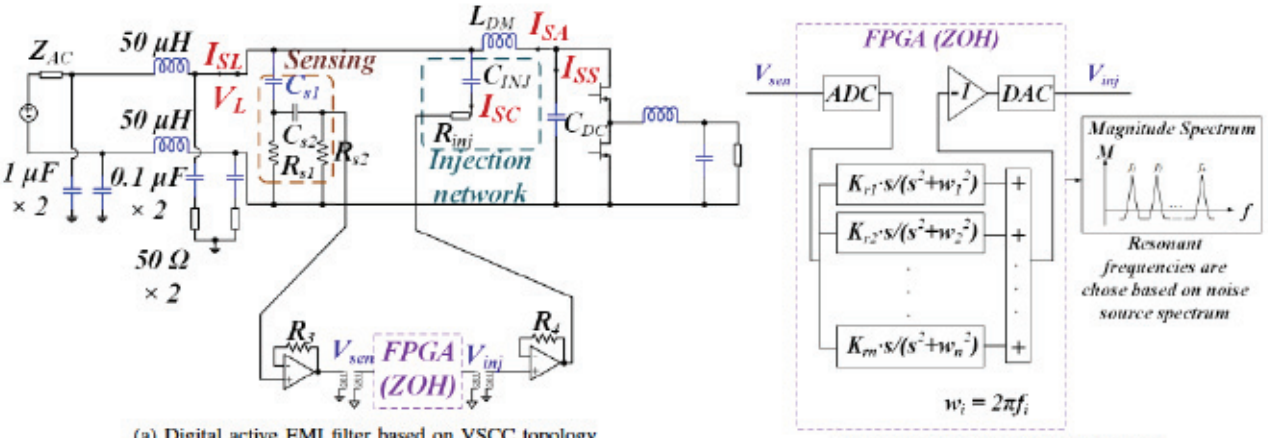


(a) Digital active EMI filter based on VSCC topology

(b) Resonant controller built in FPGA

Fig. 1: Proposed digital active EMI filter with the resonant controller

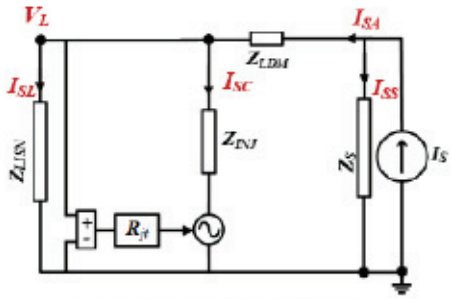
the proposed AEF achieves an attenuation of 46 dB at around 150 kHz which is 25 dB higher than conventional single-stage active EMI filter. This is the highest reported attenuation in the literature using single-stage digital or analog AEF.

The organization of the work is as follows. Section II describes the topology which is used in the implementation. Section III involves the theoretical modeling of proposed VSCC with the resonant controller. Section IV describes the design case for the proposed concept and frequency domain measurements using the VNA to verify the modeling. Section V describes the experimental test setup and discusses the small-signal and converter test results. Section VI presents the conclusion.

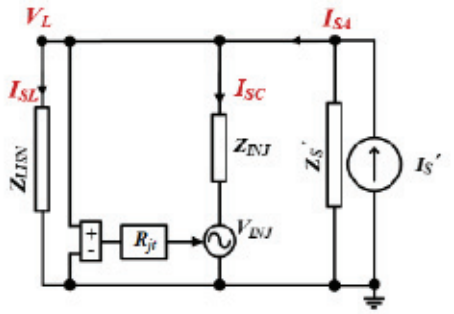
II. Active EMI filter Topology

Different AEF topologies use either current or voltage sensing and compensation. While for AEF topologies that utilize current-sensing or voltage compensation, current transformers (CTs) or voltage-injection transformers are needed. For DM noise, CTs and voltage-injection transformers can be bulky when the line current is high. Therefore, AEF topologies that do not have transformers are preferred. The voltage-sense current-cancellation topology requires high voltage capacitors and other low voltage circuitry for noise sensing and cancellation. In summary, VSCC topology will maximize the volume reduction for AEFs, which will be used in this paper. Previously, feedback control based voltage-sense current-cancellation topology was demonstrated in [27]. However, the attenuation of only 12 dB at around 150 kHz is obtained. This paper utilizes the resonant controller built in FPGA for the feedback loop of VSCC AEF, which achieves 46 dB attenuation at around 150 kHz and is the highest attenuation in reported literature.

The VSCC AEF topology is shown in Fig. 1. And the simplified version of VSCC topology is shown in Fig. 2a, where the feedback loop is collapsed into a transfer function R_{jt}. Through Norton and Thevenin equivalent circuit transformation, the equivalent circuit can be obtained as Fig. 2b. I_S



(a) Simplified VSCC AEF topology



(b) Equivalent circuit of VSCC AEF topology

Fig. 2: VSCC AEF topology

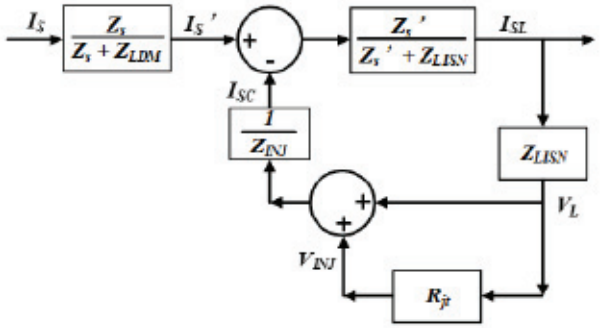
is the noise source current and I_S' represent equivalent noise source current considering the current sharing between the differential-mode noise source impedance (Z_S) and impedance of DM inductor. The new equivalent noise source (I_S') and noise source impedance (Z_S') is given by (1) and (2), respectively. The AEF cancellation current and noise current on the LISN are represented by I_{SC} and I_{SL}, respectively. The noise voltage on the LISN is represented by V_L.

$$I_S' = \frac{Z_S}{Z_S + Z_{DM}} I_S \tag{1}$$

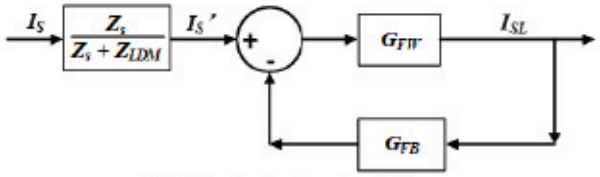
$$Z_S' = Z_S + Z_{DM} \tag{2}$$

III. Design and Modeling of the Active EMI Filter with Digital Resonant Controller

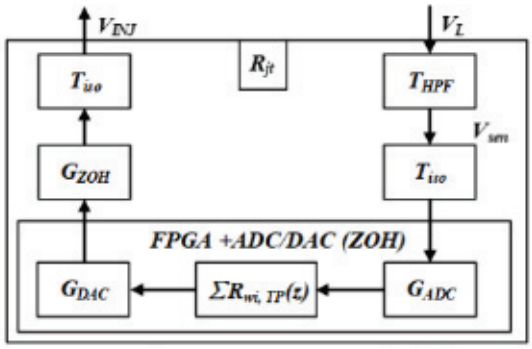
According to Fig. 1 and Fig. 2b, the block diagram of VSCC AEF system is shown in Fig. 3a. The equivalent feedforward and feedback loop equivalent block diagram is shown in Fig. 3b, where $G_{FW}(s)$ and $G_{FB}(s)$ donate transfer function of forward and backward loop. Sensing and FPGA processing are collapsed into R_{jt}. The open-loop current gain G_{FW} without the DAEF (R_{js} is disconnected) is given by (3). And the feedback loop transfer function is give by (4). Close-loop current gain G_{CL} with active EMI filter is give by (5). The insertion gain G_{IS}, which is defined as the ratio of current flowing through Z_{LISN} with and without active EMI filter, can be derived as (6). The open loop gain is given by (7), which will be used for defining stability margin.



(a) System block diagram (Sensing and FPGA processing stage are collapsed into R_{jt})



(b) Equivalent system block diagram



(c) Sensing and FPGA processing stage block diagram

Fig. 3: Block diagram of VSCC DAEF system

$$G_{FW} = \frac{I_{SL}}{I_S'} = \frac{Z_S' \cdot Z_{INJ}}{Z_{INJ} \cdot (Z_S' + Z_{LISN}) + Z_{LISN} \cdot Z_s'} \quad (3)$$

$$G_{FB} = \frac{I_{SC}}{I_{SL}} = R_{js} \frac{Z_{LISN}}{Z_{INJ}} \quad (4)$$

$$G_{CL} = \frac{I_{SL}}{I_S'} = \frac{G_{FW}}{1 + G_{FW} \cdot G_{FB}} \quad (5)$$

$$G_{IS} = \frac{G_{FW}}{G_{CL}} = \frac{1}{1 + G_{FW} \cdot G_{FB}} \quad (6)$$

$$T_{LG} = G_{FW} \cdot G_{FB} \quad (7)$$

The sensing and FPGA processing transfer function R_{jt} is shown In Fig. 3c. T_{HPF} denotes the transfer function of the high pass filter, T_{iso} denotes the RF transformer transfer function, G_{ADC} and G_{DAC} denotes the transfer function of ADC sampling stage, $R_{wi,Tp}(z)$ denotes the transfer function of digitized resonant controller, G_{ZOH} denotes the transfer function of transformation between continuous and discrete domain. Within FPGA, resonant controllers are built in parallel with each other, the transfer function of R_{js} is given by (8). The resonant controller provides high gain at frequencies which match with noise source spectrum, and provide high attenuation to the EMI noise at those frequencies. However, the delay introduced by ADC/DAC and the phase introduced by resonant controller will give rise the stability issue in feedback loop.

$$R_{js} = T_{HPF} \cdot T_{iso}^2 \cdot G_{ADC} \cdot G_{DAC} \cdot \sum_{w_i=w_1}^{w_i=w_n} R_{wi,TP}(z) \quad (8)$$

Discretization methods of resonant controller and detailed modeling of each component within VSCC DAEF system will be discussed in the next few sections, which will provide a guideline of the detailed resonant controller modeling strategy.

A. Gain Selection for Resonant Controller

The selection of gain at different resonant frequencies is dependant on the clock accuracy for pulse width modulation (PWM), the accuracy of resonant controller itself within FPGA, and the fundamental frequency of output current if the noise source is an inverter. Assuming resonant frequency of resonant controller is w_i, and the frequency variation caused by the PWM clock accuracy or calculation accuracy is Δw_i (either positive or negative). The amplitude of the resonant controller at $w = w_i + \Delta w_i$ frequency is given by (9). The lower limit of gain value selection is given by (10), where dB_{rsd} denotes the desired amplitude residue of the resonant controller at $w = w_i + \Delta w_i$ frequency. The higher limit of gain value is given by (11), which limits the bandwith of resonant within $w_i - 0.05w_i$ to $w_i + 0.05w_i$ to make sure that the resonant controller will not create stability issues when multiple resonant controllers are used in parallel.

$$|R_s(w_i + \Delta w_i)| = \left|\frac{K_{r,i}}{-2\Delta w_i + \frac{\Delta w_i^2}{w_i + \Delta w_i}}\right| \quad (9)$$

$$|R_s(w_i + \Delta w_i)| > 10^{\frac{dB_{rsd}}{20}} \quad (10)$$

$$|R_s(w_i \pm 0.05w_i)| \approx \frac{10K_{r,i}}{w_i} < 2 \quad (11)$$

B. modeling of The High Pass Filter

The converter that uses this filter could be fed from an ac or dc supply. Either way, the noise-sensing stage has to sufficiently attenuate any 60 Hz ac voltage and its harmonics, and the high-frequency currents due to rectifier operation or any other converters connected to the same node. Otherwise, any low frequency harmonic can easily saturate the output of the active circuits. Ideally, the output of the high pass filter should only include the switching frequency and its harmonics in the desired EMI frequency range (150 kHz to 30 MHz). The design of the sensing network requires careful consideration to ensure that it:

1. has the desired performance throughout the entire frequency range and
2. it does not add too much to the volume of the filter

It is not possible to get around high attenuation at 60 Hz with a 1^{st} order high pass filter. Therefore a 2^{nd} order high pass filter is used as the sensing network. The capacitor C_{s1} needs to be rated for the input voltage and needs to be safety rated (X1Y1 rated). The other components C_{s2}, R_{s1} and R_{s2} are low voltage and low power components. The capacitor C_{s2} is a 50 V rated X7R surface mount capacitor. The transfer function of the filter is given by (12) $\sim$ (14). The output of the high pass filter is buffered (op-amp configured as voltage follower) and fed to ADC. The selected op-amp is unity-gain stable with a gain-bandwidth of about 500 MHz. Therefore, the output of the buffer could be assumed to be the same as that of the high pass filter.

$$T_{HPF} = \frac{s^2}{s^2 + k_1 s + k_2} \tag{12}$$

$$k_1 = \left(\frac{1}{C_{s1}R_{s1}} + \frac{1}{C_{s1}R_{s2}} + \frac{1}{C_{s2}R_{s2}}\right) \tag{13}$$

$$k_2 = \frac{1}{C_{s1}C_{s2}R_{s1}R_{s2}} \tag{14}$$

C. modeling of the ADC and DAC Sampling System

According to [39], the RF transformer which is used in sampling system for matching the impedance on termination, the transfer function can be modelled as (15). The characteristic of the RF transformer is simply a band pass filter, which has the first corner frequency w_1 as around 20 kHz and the second corner w_2 as around 200 MHz.

$$T_{iso} = \frac{1}{(1 + w_1/s) \cdot (1 + s/w_2)} \tag{15}$$

[40] presented the model of discrete sampling system, transfer function of transformation between continuous and discrete domain is given in (16), where T_s represents the digitization step.

$$G_{ZOH} = \frac{1 - e^{-sT_s}}{sT_s} \tag{16}$$

For most of the off-shore ADC/DACs, there are clock latency which is around 5 to 15 clock cycles. Thus, the model of ADC and DAC are given in (17) and (18), where m and n denote the bit width of ADC and DAC, V_{ADC} and V_{DAC} denote the range of ADC and DAC, n_{ADC} and n_{DAC} donate the clock latency of ADC/DACs.

$$G_{ADC} = \frac{2^m}{V_{ADC}} \cdot z^{-n_{ADC}} \tag{17}$$

$$G_{DAC} = \frac{V_{DAC}}{2^n} \cdot z^{-n_{DAC}} \tag{18}$$

IV. System Level Modeling of the Configuration and Stability Analysis

In this section, the parameter of the AEF system will be given or derived based on previous sections, and then the open loop gain and close loop gain modeling and measurement will be conducted.

The noise source is a DC-DC converter, the output filter components' parameters are: $L = 70\mu H$ and $C = 5\mu F$. The switch frequency of DC-DC converter is 50 kHz, and it's realizing 12 to 5 V conversion. The inductance value of the DM inductor is $L_{DM} = 131\mu H$, and capacitance value of the DM capacitor is $C_{INJ} = 470nF$.

The gain for resonant controller ($K_{r,i}$) is selected based on (9) $\sim$ (11). For example, for an DC-DC converter which switching frequency is $50kHz$, and resonant controller at 150 kHz is to be designed for DAEF. Assuming the 150 kHz noise will have $\pm 300Hz$ variation. 30 dB amplitude residue (dB_{rsd}) at $150kHz \pm 300Hz$ is to be ensured. According to (10), the lower limit of gain K_i can be calculated as $1.9 \cdot 10^4$. And according to (11), the higher limit of K_i can be calculated as $3 \cdot 10^4$. So the value of resonant controller gain K_i should satisfy $1.9 \cdot 10^4 < K_i < 3 \cdot 10^4$.

For the second order high pass filter, the components' values are: $C_{s1} = 4.7\ nF$, $C_{s2} = 10\ nF$, $R_{s1} = 3.3\ k\Omega$ and $R_{s2} = 3.3\ k\Omega$. According to (12) $\sim$ (14), two corner frequencies of the high pass filter can be calculated as $700Hz$ and $7kHz$. The attenuation of $60Hz$ signal is around $35dB$, which will make sure that the line frequency voltage variation will not saturate the ADC sampling.

The proposed concept is implemented using Intel Cyclone IV FPGA in a Terasic DE2-115 demo board, and the operating frequency is set to 100 MHz, so the discretization time step is $T_s = 10ns$. In the configuration, the ADC AD9254 [41] has around 4 ns of propagation delay and 12 cycles of clock latency. Since the ADC is using FPGA's clock output as ADC clock in the design, the propagation delay can be ignored and totally 13 cycles of clock latency exists in ADC sampling. The same concept can be applied to DAC DAC5672 [42] model. In equation (17) and (18), the n_{ADC} and n_{DAC} values can be acquired as (19).

$$n_{ADC} = 14, \quad n_{DAC} = 5 \tag{19}$$

Based on (3) $\sim$ (8), the loop gain of the proposed configuration of AEF without resonant controller can be expressed as (20). The first round of loop gain and phase measurement

should be done by replacing resonant controller with unity gain transfer function, which is described as (7). The loop gain measured from the circuit under test as well as loop gain calculated from modeling is shown in Fig. 4. From 70 kHz to 20 MHz, the model matches pretty well with the measurement, the discrepancy of low frequency and high frequency gain/phase might be caused by the inaccuracy model of the RF transformer.

$$T_{LG,w/o\ res} = G_{FW} \cdot \frac{Z_{LISN}}{Z_{INJ}} \cdot T_{HPF} \cdot T_{iso}^2 \cdot G_{ADC} \cdot G_{DAC} \tag{20}$$

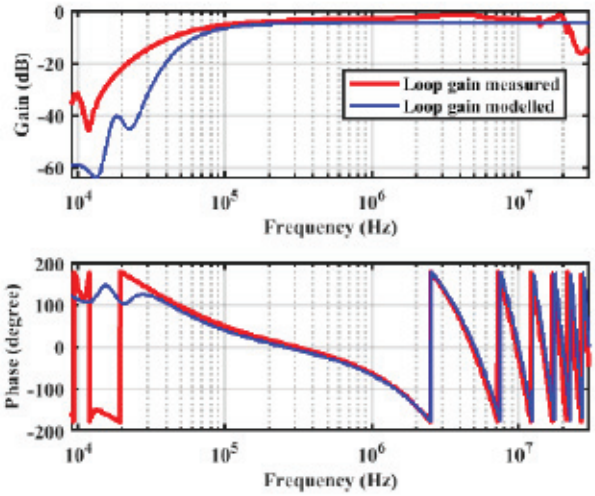


Fig. 4: Loop gain without resonant controller

Gain and phase of the loop gain without PR controller is of great significance in determining where digital PR controller can be implemented. The resonant controller will introduce 90° lead/lag. In order to make sure that the entire loop gain with the resonant controller implemented is stable, original phase of the loop gain without PR controller should be within ±90°, otherwise phase compensation should be implement together with the resonant controller. Remaining 25° phase margin, 65 kHz to 950 kHz frequency range is available for implementing resonant without any phase compensation.

Assuming the noise source is a converter/inverter operating at 50 kHz switching frequency, then the noise source will contain $k_i \cdot 50kHz$ noise and its harmonics. CISPR 22 defined the conducted emission limit from 150 kHz to 30 MHz, so the resonant controller's frequencies are selected as $i \cdot 50kHz$ where i ranges from 3 to 19. Gain selection for resonant controller is done by using (10) and (11). After carefully designing the resonant frequencies and gains, the loop gain incorporating resonant controller is obtained in Fig. 5. As it can be seen from the loop gain measurement, the phase margin at highest frequency is exactly 25°, which matches very well with previous analysis.

The insertion loss measurement result is shown in Fig. 6. From the figure it can be seen that the insertion loss at 150 kHz is enhanced by about 45 dB using the resonant controller. The insertion loss is high at harmonics of 50 kHz (n = 3, 4, ..., 19).

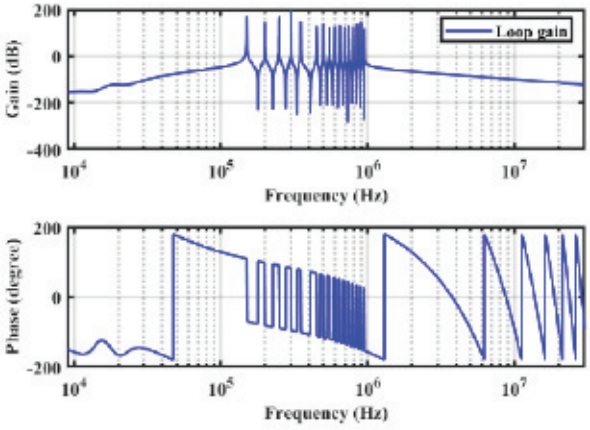


Fig. 5: Loop gain with the resonant controller

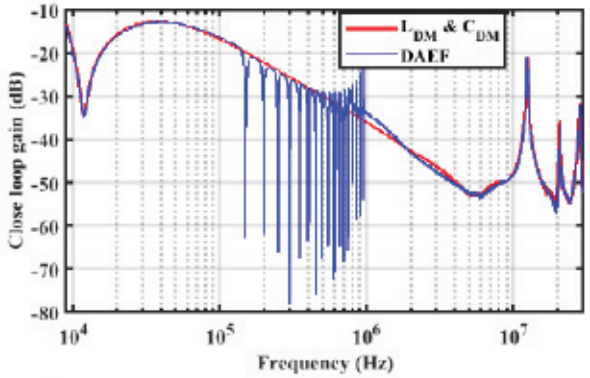
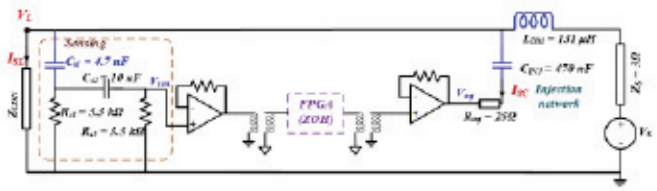


Fig. 6: Insertion loss measurement of DAEF implementation

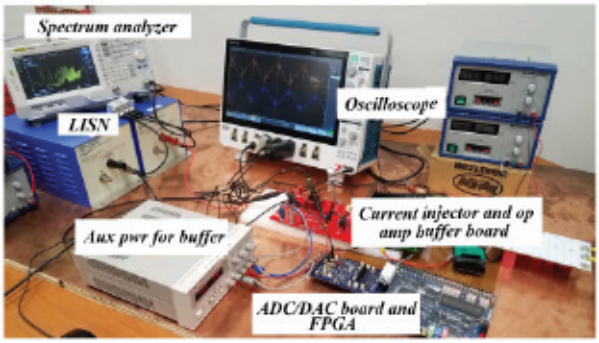
V. Experimental Results

The filter discussed in above is implemented in the experiment. The proposed resonant controller is implemented in the FPGA (Intel Cyclone IV FPGA in a Terasic DE2-115 demo board along with Terasic AD/DA daughter card with sample rate of 100 MHz). Apart from the filter, the noise is measured at the LISN using an EMI receiver.

In the small signal measurement, a function generator along with a buffer is used as the noise source, and D = 0.5 and D = 0.3 of noise source are implemented and test. The EMI receiver measurement is shown in Fig. 8a and the attenuation at 150 kHz with the active EMI filter is about 45 dB which is the highest attenuation reported in any active EMI filter literature, both analog and digital active EMI filters. As for D = 0.3 condition, harmonics of 50 kHz (n = 3, 4, ..., 19) is attenuated down to noise floor as well.

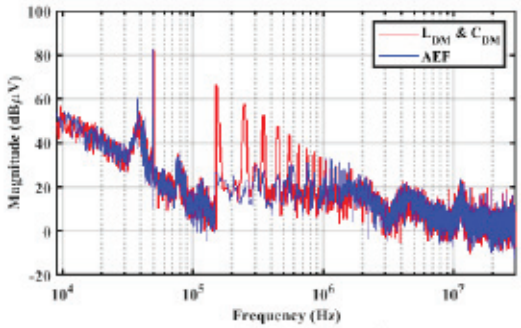


(a) Equivalent circuit for experiment setup

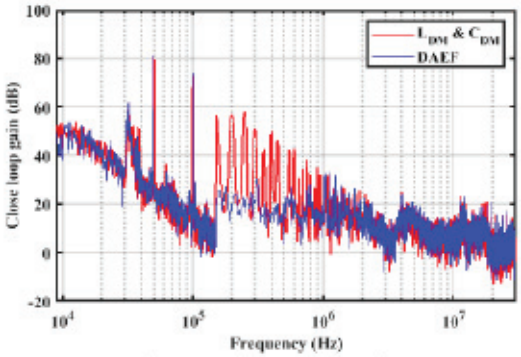


(b) Picture for experiment setup

Fig. 7: Experiment setup



(a) Test under D = 0.5 condition



(b) Test under D = 0.3 condition

Fig. 8: Small signal test of proposed DAEF under different noise source condition

Conclusion

The performance of conventional digital active EMI filters are limited by the delay introduced by the ADC/DAC. The best attenuation reported in the literature is 24 dB at 150 kHz. This paper proposes a new method to combine proportional resonant controller along with the digital active EMI filter to improve the attenuation by another 20 dB. Design and modeling of the proposed DAEF are discussed, small-signal experimental results as well as converter experimental results have confirmed the validity of the proposed method.

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