Optimal Ferroelectric Parameters for Negative Capacitance Field-Effect Transistors Based on Full-Chip Implementations—Part II: Scaling of the Supply Voltage

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***Abstract*— Negative capacitance field-effect transistors (NCFETs) with optimal ferroelectric parameters provide phenomenal power reduction as discussed in Part I. In this part, we explore the impact of operating voltage on power consumption at the device, gate, and full-chip levels. We first observe that high operating voltages applied to NCFET devices lead to an abrupt increase in both the drain current and the gate capacitance. Furthermore, negative capacitance is lost when the voltage is set too high. On the other hand, the gate capacitance increase still exists, although with smaller magnitude, even at low operating voltages. This helps reduce device delay and eventually full-chip delay. Furthermore, delay improvement at the full-chip level can be traded off to gain power reduction at the full-chip level. Finally, our experiments suggest that a sufficiently low supply voltage (=0.4 V out of [0.2 and 0.8 V] range in our study) is needed to maximize power and performance gain at full-chip level.**

***Index Terms*— CMOS technology, high performance, low-power, negative capacitance transistor.**

I. Introduction

IN THE first part of this article [1], we performed detailed analysis of the negative capacitance field-effect transistor (NCFET)-based transistor, inverter, and full-chip level at a fixed supply voltage of $V_{DD} = 0.4$ V. We presented the NCFET parameter space region that provides the highest power reduction at the specific voltage without any loss in performance. In traditional circuits, voltage scaling is an integral part of the low-power circuit design as it is directly related to power consumption. In this article, we investigate the impact of the voltage scaling in the NCFET parameter space and identify the important effects it has on the power, delay characteristics of the device. This is carried out at the inverter level using the inverter model of the FreePDK 15-nm Open Cell Library (OCL) [2] device model, and the full-chip level with the low-density parity-check (LDPC) circuit [3] as our benchmark and FreePDK 15-nm OCL as the technology. Using the framework for identifying, the optimal parameters from Part I, we find how V_{DD} impacts the optimal region. We show that varying the V_{DD} has a sometimes counter-intuitive impact on higher level parameters such as delay and power. We also analyze the power benefits of using NCFETs at the full-chip level. In this article, wherever we mention NCFET or NCFET-based devices, it means that the transistors in those implementations have the internal metal layer and ferroelectric layer in their gate-stack as seen in Part I. Across both the articles, we make the following assumptions about NCFETs: 1) the switching speed of NCFETs is higher than the device switching; 2) it is possible to find materials with low viscosity parameter that allow for the high NCFET switching shown; and 3) the multidomain and grain-size effects are ignored. As we perform a device and circuit co-design and optimization with combined effects of remnant polarization and coercive field, these assumptions help to focus on the considered parameters and their full-chip effects.

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II. Ferroelectric and Voltage Parameter Space

The ferroelectric parameters space under consideration remains the same from Part I [1]. The thickness of the ferroelectric layer is fixed at $t_F = 2.5$ nm [4]–[6]. The coercive field (E_C) and spontaneous polarization (P_O) of the ferroelectric layer are varied within the range 1 MV/cm $\leq E_C \leq$ 4 MV/cm and 10 μC/cm^2 $\leq P_O \leq$ 40 μC/cm^2 (refer to [1, Fig. 2(a)]). The design space is based on a literature survey from reported works on NCFETs, including, but not limited to, [7]–[13]. Based on the reported parameter space, we expanded it to include the different regions in the

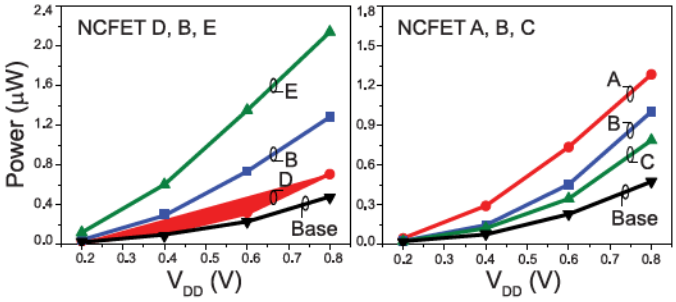

Fig. 1. Impact of V_{DD} on inverter (NCFET and BaseFET) power consumption.

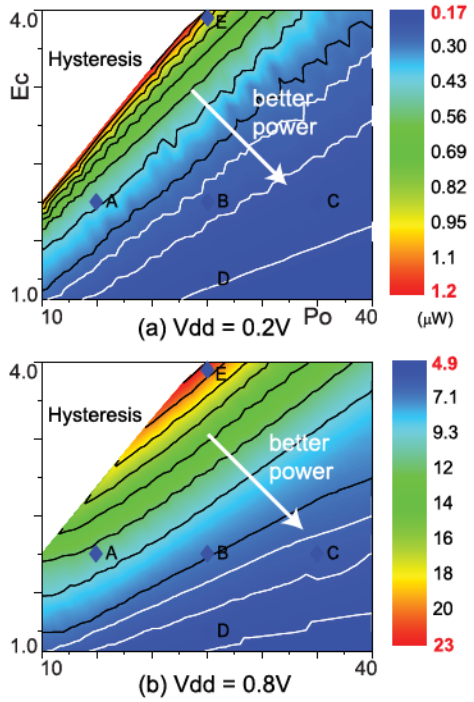

Fig. 2. NCFET inverter power phase plots at $V_{DD} = 0.2$ and 0.8 V. We omit 0.4 and 0.6 V due to space limit. However, they show the same trend except that the power consumption ranges for 0.4 and 0.6 V are [0.9, 6.5 μW] and [2.4, 14 μW], respectively.

design space, such as hysteresis and nonhysteresis regions, and to cover a wide-enough range of negative capacitance behaviors in the nonhysteresis. The points A, B, C, D, and E representing ferroelectric parameters of the NCFETs that we study in particular details in this article are the same from Part I.

Four different V_{DD} values of (0.2, 0.4, 0.6, and 0.8 V) are considered for the voltage space. The highest voltage point of 0.8 V is the nominal V_{DD} for the FreePDK 15-nm technology [2], and hence, we study the parameter space with $V_{DD} \leq 0.8$ V for the power reduction study.

III. NCFET Inverter Analysis

In this section, we study how the delay and power in NCFET-based inverters evolve as V_{DD} is scaled. To study this, our test-bench consists of a fan-out-1 inverter (a minimum-sized inverter driving another identical inverter as load). The inverter model includes the parasitic information of interconnects in the inverter layout, and these parasitics are external to a transistor. The device simulation is based on the

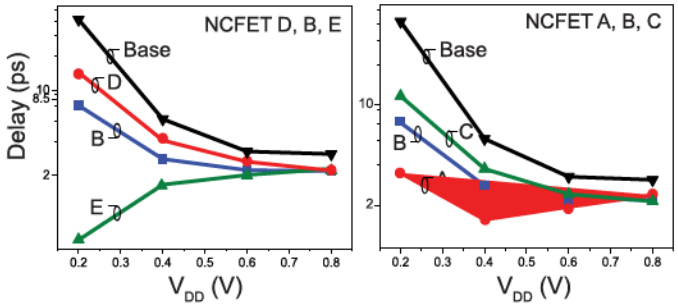

Fig. 3. Impact of V_{DD} on inverter (NCFET and BaseFET) delay.

Verilog-A model of the NCFETs [1], [14] that models the effect of negative-capacitance on the transistor characteristics.

A. NCFET Inverter Power as Function of V_{DD}

In Fig. 1(a) and (b), we present the power dissipated versus V_{DD} in the inverters based on NCFETs B, D, and E and A, B, and C, respectively. Power consumption of the BaseFET(no ferroelectric layer) is also included for comparison. The inverter power increases with V_{DD} in all NCFETs as would be expected due to the increase in current with increasing V_{DD}.

To show the overall evolution of the power at different voltages, the phase plots are shown in Fig. 2 for $V_{DD} = 0.2$, 0.8 V. At all V_{DD} levels, the power phase plot follows the same pattern—the power is maximum for devices near the hysteresis region and decreases as we move away. The total power is proportional to the total ON-current, which increases as the negative capacitance effect increases. This is the reason that the devices closer to the hysteresis boundary consume higher power, and the power decreases as we move further away from the boundary. The total power is dominated by short-circuit power component at all V_{DD} (as was explained in Part I) and resembles the phase map for the short-circuit current plotted in Fig. 3(i) of Part I [1].

B. NCFET Inverter Delay as Function of V_{DD}

The delay of the inverters based on NCFET B, D, and E and A, B, and C, respectively, are plotted with respect to the supply voltage and shown in Fig. 3. In both the plots, the BaseFET inverter delay is included for comparison. For an inverter consisting of standard MOSFETs (BaseFET inverter), the delay is expected to decrease with the increase of V_{DD}—the increase in ON-current with an increasing V_{DD} charges up the load capacitor quickly. However, in Fig. 3, it is observed that the evolution of delay with V_{DD} is not the same for all NCFET inverters. The inverters based on NCFET B,C, and D have delays monotonically decreasing with increase in V_{DD} (as expected). However, the delay of inverter with NCFET E is the lowest at $V_{DD} = 0.2$ V and increases with V_{DD}. The inverter delay of NCFET A decreases as V_{DD} decreases from 0.2 to 0.4 V, but increases as V_{DD} is increased from 0.4 to 0.8 V.

Depending on the shape of the delay versus V_{DD} plots, the NCFET parameter space is split into various regions, as shown in Fig. 4.

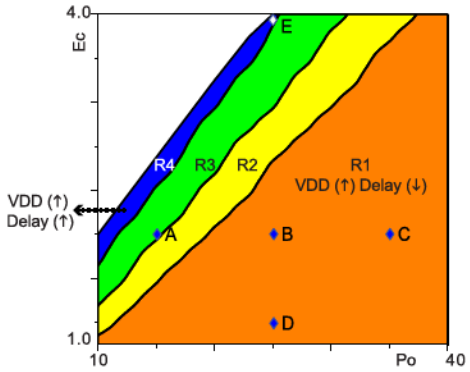

Fig. 4. Delay evolution versus V_{DD} in the parameter space. Based on the delay versus V_{DD} graphs, the nonhysteretic parameter space is divided into four regions R1–R4.

R1: The region where delay decreases monotonically with increase in V_{DD}. This is the traditional delay-V_{DD} trend observed in BaseFETs. Inverters with NCFETs B, C, and D fall in this region. This is a region with low negative capacitance effect from ferroelectrics.

R2: The region where the delay decreases as expected from 0.2 to 0.6 V, and increases from 0.6 to 0.8 V. This is where the negative capacitance effect becomes strong enough to overcome the effect of increasing voltage on the delay.

R3: The region in the parameter space where delay decreases only from 0.2 to 0.4 V, but then increases from 0.4 to 0.8 V. NCFET A falls in this region.

R4: The final nonhysteretic region where the delay increases monotonically from 0.2 to 0.8 V. The NCFETs closest to hysteresis form this region. NCFET E is one such example.

To understand the origin of different delay trends among different NCFETs, in Fig. 5 voltage transfer curves (VTCs) of the inverters based on NCFET A, C, and E are plotted. From the VTCs of A and E in Fig. 5, it is observed that at higher V_{DD}, the VTCs for NCFETs A and E, have significantly more diffused transitions compared with the VTCs of NCFET C and BaseFET (represented as a dotted line in all VTC plots). This is because the steep subthreshold slope in NCFETA and E coupled with the OFF-current adjustment leads to a low threshold voltage as can be seen in $I_D - V_{GS}$ beside the inverter VTCs. The left and right ends of the VTC slope (transition) correspond to the voltages where n-FET exits and p-FET enters the subthreshold region, respectively. This means that during an input rise transition of a cell, such as an inverter, the n-channel FET turns on faster and p-channel FET turns off slower. In the transient behavior, this leads to a wider region in the transition where both n-FET and p-FET consume current causing an increased internal current in the inverter (refer to [1, Fig. 3(c) and (d)]). This internal (short-circuit) current limits the current available to the load. In fact, for inverters A and E, with the increase in V_{DD}, the time spent in the short-circuit region and short-circuit current increases such that the available current to charge/discharge the load capacitor decreases. In other words, at higher values of V_{DD}, the short-circuit current (and power) constitutes a larger fraction of

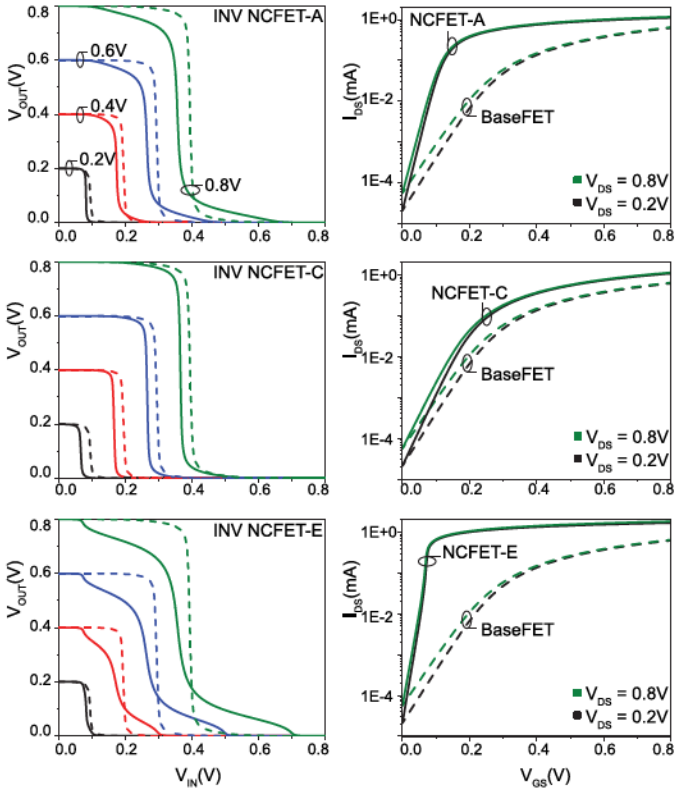

Fig. 5. **Left column:** VTCs for inverters based on NCFET A, C, and E for $V_{DD} = 0.2$, 0.4, 0.6, and 0.8 V. **Right column:** I_D–V_{GS} curves of nMOS based on NCFETs A, C, and E at the highest and lowest V_{DS}. The dotted lines in all the plots correspond to BaseFETs.

the current drawn from the power supply during switching, and hence, reduces the current that goes into charging and discharging the load. This results in the increase in the delay with increasing V_{DD} in NCFET inverters A and E. This signifies that a higher ON-current is not the only important parameter in choosing the best NCFET parameters. Along with higher ON-current the current supplied to the load is of higher importance. With varying V_{DD}, this internal current and current supplied to the load varies and changes the impact of NCFET parameters on delay characteristics. Note that supply voltage scaling does not have a huge impact on the I_D–V_{GS} curves of an n-channel or p-channel transistor but rather affects the higher level characteristics, such as the delay and power, of an inverter and full-chip level as we will see in Sections III and IV.

In Fig. 6, the phase plots of the inverter delay with respect to (P_O and E_C) at V_{DD}=0.2, 0.4, and 0.8 V are shown. The BaseFET inverter delay at nominal $V_{DD} = 0.8$ V, $t_D = 2.55$ ps is the target delay and NCFETs exhibiting delay less than 2.55 ps are marked with the blue–red phase in each of the phase plots. NCFETs with delay $t_D > 2.55$ ps constitute the gray region. In Fig. 6, we observe that with the increase in V_{DD} the minimum delay region of (P_O and E_C) moves away from the hysteresis boundary line toward the right direction. This shift in the minimum delay region with V_{DD} occurs due to the increased short-circuit current at higher V_{DD} in the inverters with steep switching characteristics near the hysteresis boundary—which also causes NCFETA- and E-based inverters to show unusual delay versus V_{DD} characteristics (as explained

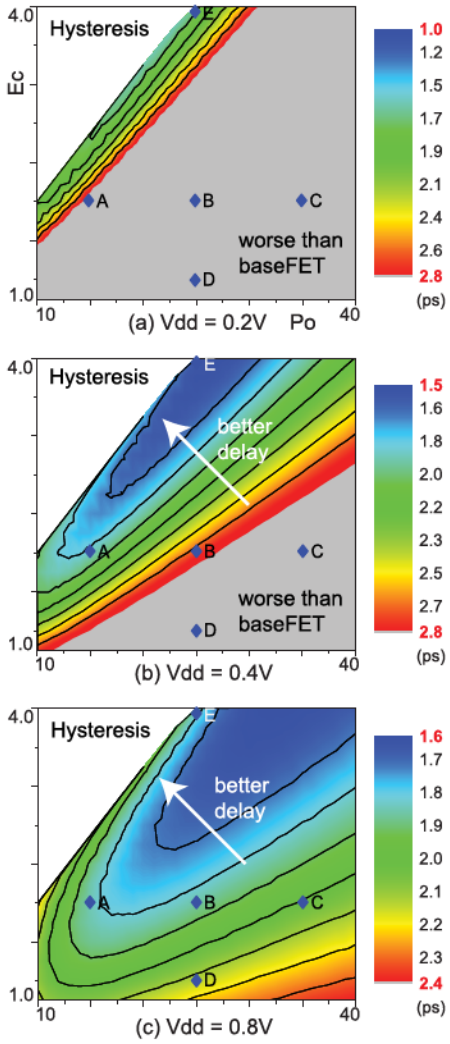

Fig. 6. NCFET inverter delay phase plots. $V_{DD} = 0.6$ V is omitted due to space limit, but it resembles 0.8 V. The gray region contains NCFETs that are slower than the BaseFET.

in the earlier paragraph). This shows that at a given voltage it is not always true that the fastest NCFETs are the ones with highest negative capacitance effect. The NCFET inverter has a minimum delay of 1.0 ps across all V_{DD}'s and parameter space. This is more than thrice the maximum intrinsic switching delay of the ferroelectrics of 270 fs shown in [15] and, therefore, neglecting the dynamic behavior of the ferroelectrics does not have a huge impact on the device characteristics.

C. Ferroelectric Parameters and V_{DD} Co-Optimization

Next, we study how the optimal ferroelectric parameters—the (P_O and E_C) combinations consume within 5% of the lowest power at each V_{DD} while meeting the target delay of 2.55 ps of nominal BaseFET—evolve as V_{DD} is scaled from 0.8 to 0.2 V. Fig. 7 plots the V_{DD} evolution of optimal ferroelectric parameter space. We observe in Fig. 7 that with the decrease in V_{DD}, the optimal (P_O and E_C) region moves closer to the hysteresis boundary. The lowest power consumption devices at a given V_{DD} are the ones that are farthest away from the hysteresis region. The additional delay target set by BaseFET devices acts as the limit to how farther away from the hysteresis region can we go without exceeding the target delay. And the power limit dictates how far the optimal

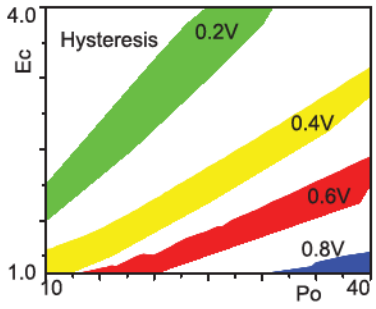

Fig. 7. Optimal NCFET inverter ferroelectric parameter space at different V_{DD}.

TABLE I
NCFET INVERTER POWER COMPARISON. WE REPORT THE BEST (P_0 AND E_C) AMONG 496 COMBINATIONS AT EACH V_{DD}. THE BASEFET CONSUMES 5.80 μW AT 0.8 V. IMPORTANT PARAMETERS OF THE N-TYPE TRANSISTOR ARE ALSO INCLUDED

	0.2 V	0.4 V	0.6 V	0.8 V
EC (MV/cm)	1.6	1.0	1.2	1.0
P0 (μC/cm^2)	10	10	35	29
Total Power (μW)	0.466	1.28	2.65	4.93
Power Saving over BaseFET (%)	91.98	78.02	54.38	15.00
V_{th} (V) of nFET	0.069	0.147	0.230	0.230
SS (mV/dec) of nFET	22.4	45.6	71.0	70.9
I_D (mA) of nFET	0.359	0.441	0.572	0.896

region can move toward higher power (power increases as we move toward the hysteresis boundary) in the direction of better delay without increasing power than the target of 5% from the minimum. Table I shows the combinations that lead to the lowest total inverter power of the NCFET devices. Note that multiple combinations of (P_O and E_C) lead to the same power reduction and we only report a single value. For example, in Fig. 2 all the (P_O and E_C) combinations lying on a fixed black line represent the devices with equal power consumption. The most important observation is that the ferroelectric parameters need to be optimized for each value of V_{DD}, and such V_{DD}-based optimization will lead to the maximum reduction of inverter power.

IV. Full-Chip Analysis

Finally, we explore the NCFET isoperformance power characteristics of the full-chip benchmarks based on LDPC. The maximum frequency of 2.5 GHz achieved by BaseFET implementations at nominal $V_{DD} = 0.8$ V is used as the target frequency similar to that described in Part I. Table II compares the full-chip implementations of NCFETs A–E at various voltages. The BaseFET implementation at $V_{DD} = 0.8$ V is also shown for reference. NCFETs A–D fail standard cell library implementation at $V_{DD} = 0.2$ V as the cells in the FreePDK 15-nm OCL used are designed to work at the nominal 0.8-V $\pm$ variance and the low voltage can cause some transistors to be in permanent OFF-state in the subthreshold. Therefore, these NCFETs are excluded from the comparison table.

A. NCFET Full-Chip Power as Function of V_{DD}

All NCFET implementations have increased power consumption as V_{DD} increases in keeping with the analysis thus

TABLE II
DETAILED POWER BREAKDOWN FOR NCFETLDPC FULL-CHIP DESIGNS. CAPACITANCE VALUES ARE REPORTED IN pF AND POWER IN mW. ALL DESIGNS RUN AT 2.5 GHz

	BaseFET	NCFET A			NCFET B			NCFET C			NCFET D			NCFET E			
V_{DD} (V)	0.8	0.4	0.6	0.8	0.4	0.6	0.8	0.4	0.6	0.8	0.4	0.6	0.8	0.2	0.4	0.6	0.8
V_{th} (V)	0.278	0.099			0.169			0.199			0.212			0.061			
Timing Slack (ps)	6	40	36	38	23	34	44	-65	28	44	-144	5	39	21	20	30	25
Net cap	201	186	177	183	197	180	176	200	193	174	304	201	180	193	189	193	202
Pin cap	260	346	300	272	298	287	287	291	237	267	278	223	229	846	600	498	400
Switching Power	274	77	156	264	74	153	268	70	141	253	84	139	236	33	113	221	349
Internal Power	210	85	311	651	44	122	312	54	94	222	62	89	203	30	534	1327	2086
Leakage Power	4.4	0.6	1.2	2.3	0.7	1.2	2.2	1.0	1.2	2.3	1.3	1.4	2.2	0.2	0.6	1.3	2.3
Total Power	488	162	468	917	118	276	582	125	236	477	147	229	441	64	648	1,549	2,437

far. NCFETs C and D with low current enhancement fail to meet the target frequency at $V_{DD} = 0.4$ V indicated by the negative timing slack value, whereas they satisfy the timing constraints at higher voltages. NCFETs A, B, and E with relatively higher current enhancement, successfully meet the frequency target at low voltages of $V_{DD} = 0.4$ V. The implementation of NCFET B characterized by low pin capacitance and short-circuit current, consumes the lowest power among $V_{DD} = 0.4$ V implementations of A–E. NCFET E with extremely high current enhancement meets the frequency target even at lowest V_{DD} of 0.2 V leading to the maximum power reduction.

In full-chip implementations, additional optimizations, such as the ability to upsize a gate to meet timing or to downsize, to improve the power add higher freedom of power/timing improvements compared with a single inverter. As a result of these additional sizing optimizations, the (P_O and E_C) that fail timing in inverter analysis can meet timing with the help of upsizing, and those that consume higher power with better delay can consume lower power with downsizing. The first of the effects (up-sizing for timing improvement) is observed by comparing the phase plots of inverter [Fig. 3(b)] and full-chip [Fig. 8(a)] at 0.4 V. The region where NCFETs do not meet timing target of BaseFET at 0.8 V is smaller in full-chip implementation which means that previously slower NCFETs for inverter comparison are now able to meet timing target at full-chiplevel. The second effect (downsizing for power improvement) can be seen from Table II. Here, the full-chip implementations of NCFETs C and D at 0.8 V consume lower power than the BaseFET design. However, the inverter design with the same NCFETs C and D consume higher power than BaseFET at 0.8 V as can be seen in Figs. 1 and 2(b). The minimum operating voltage of technology is dictated by interconnect characteristics and the threshold voltage of the NCFETs. The lowest voltage leads to NCFET implementations that consume the lowest power at the feasible minimum operating voltage provide the maximum power reduction. Therefore, the optimal NCFET parameters that maximize power reduction are also a function of operating voltage.

Fig. 8(a)–(c) plots the phase maps of %reduction in total power in the NCFET implementation of LDPC at $V_{DD} = 0.4$, 0.6, and 0.8 V. Here, we only consider the NCFET implementations that satisfy the isoperformance frequency target. The phase plot at $V_{DD} = 0.2$ V is omitted as only very few inverters from the 22 sampled inverters achieve the maximum frequency target.

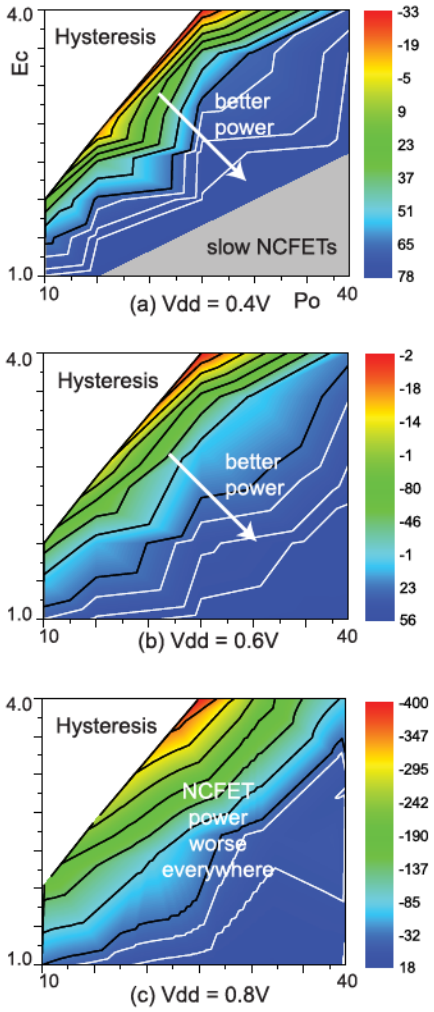

Fig. 8. LDPC full-chip isoperformance power saving over BaseFET at various V_{DD} levels. Negative means NCFET full-chip is worse than BaseFET. We omit 0.2 V because most NCFETs are slower than BaseFET, as shown in Fig. 6.

B. Ferroelectric Parameters and V_{DD} Co-Optimization

Fig. 9 is the optimal ferroelectric parameter space based on the NCFET implementation of LDPC benchmark at different V_{DD}. The definition of optimal parameters is the same as the one used for inverter trends. By comparing Figs. 9 and 7, we note that the evolution of optimal (P_O and E_C) combinations with V_{DD} are similar in both inverter and full-chip analysis. The main differences in the shapes are attributed to two main causes: 1) the discretization/sampling error created

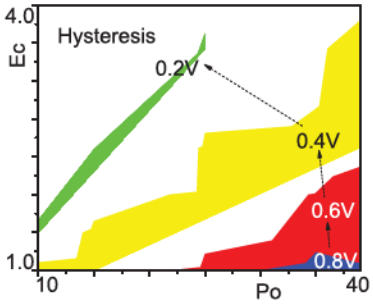

Fig. 9. Optimal NCFET full-chip LDPC ferroelectric parameter space at different V_{DD}.

TABLE III
NCFETLDPC FULL-CHIP POWER COMPARISON. WE REPORT THE BEST AMONG THE 19 COMBINATIONS USED FOR FULL CHIP ANALYSIS. THE BASEFET CONSUMES 488.0 mV AT 0.8 V

Voltage	0.2 V	0.4 V	0.6 V	0.8 V
EC (MV/cm)	1.6	1.2	1.2	1.2
P0 (μC/cm^2)	10	15	35	35
Total Power (mW)	34.4	107.8	215.2	408.1
Power Saving over BaseFET (%)	92.95	77.91	55.90	16.38
V_{th} (V) of nFET	0.069	0.147	0.230	0.230
SS (mV/dec) of nFET	22.4	53.3	71.0	71.0
I_D (mA) of nFET	0.359	0.452	0.572	0.905

by using only 22 points in the design space as opposed to 496 points for inverter study. 2) The upsizing and downsizing optimizations in the full-chip implementation lead to expanded regions where NCFETs meet timing and can achieve higher power reduction than the inverter analysis. An interesting observation is that the even with the extra optimizations in full-chip designs, the combinations of (P_O and E_C) in Table I representing the best power reduction in inverter analysis are close to the best parameters for full-chip power as seen in Table III leading to the conclusion that the sizing optimizations do not create a very large difference in optimal regions of NCFETs.

V. CONCLUSION

The operating voltage specific ferroelectric parameter space exploration and the optimal value framework proposed in this article can help device and circuit designers choose the best parameters for a given voltage and performance requirement. The differences between the gate-level and full-chip level optimizations are that: 1) the full-chip level optimization benefit from sizing optimizations by choosing from a wide range of cell-sizes and varieties that are fixed for the technology node; 2) different circuits have different types of logic and can have a small variance in optimization parameters. The variance due to the second effect would not be as drastic as the first effect. Therefore, it is recommended first to find the variance of optimality between gate level and full level (which in the 15-nm technology considered is pretty small) and then comparing the distribution of cell type.

Over both parts, we develop a multilevel framework and analysis of different aspects of the NCFET device and present the optimal parameter space of (E_c and P_o) can vary at both gate- and full-chip levels. We show the potential power benefits of using NCFETs in full-chip circuits and the voltage tuning required to achieve such benefits. We also show that in very steep-slope NCFETs, the delay versus V_{DD} trend inverts, and therefore, choosing the NCFET with steepest subthreshold slope is not always the best choice. As this is a simulation-based study targeting multiple levels of abstractions, several assumptions about an ideal NCFET and ideal power supply are made for simplicity. Viscosity parameter and switching speed can limit the NCFET parameter space. Grain size, orientation, and phase of the domains can reduce the potential benefits by introducing variability in the ferroelectric layer. Relaxation time can also introduce new constraints similar to hold time violations in the full-chip design. A high IR-drop due to the increased ON-current can limit the minimum supply voltage that can be supplied. Therefore, a detailed full-chip study is further needed as technology improves.

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