Solid State Electronics 172 (2020) 107881

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Electrical properties of MgO/GaN metal-oxide-semiconductor structures

Onoriode N. Ogidi-Ekoko[a,*], Justin C. Goodrich[a], Alexandra J. Howzen[b], Matthew R. Peart[a], Nicholas C. Strandwitz[b], Jonathan J. Wierer Jr.[a], Nelson Tansu[a]

[a] Center for Photonics and Nanoelectronics, Department of Electrical and Computer Engineering, Lehigh University, Bethlehem, PA 18015, USA
[b] Department of Materials Science and Engineering, Lehigh University, Bethlehem, PA 18015, USA

ARTICLE INFO

The review of this paper was arranged by "E. Calleja"

Keywords:
MgO
Al_2O_3
GaN
C-V characteristics
I-V characteristics
MOS capacitor

ABSTRACT

Electrical properties of metal-oxide semiconductor (MOS) capacitors were measured with MgO/Al_2O_3 gate dielectrics deposited by atomic layer deposition (ALD) on GaN. For an Al_2O_3 (1 nm)/MgO (20 nm) dielectric layer, a leakage current density of 0.25 mA/cm^2 at 1 V was measured for the MOS capacitor. A peak capacitance of ~0.1 μF/cm^2 was obtained from the C-V measurements with significant hysteresis observed. In addition, a 15-minute forming gas anneal at 450 °C resulted in an increased leakage current density of 1 A/cm^2 at 1 V while also increasing the peak capacitance by approximately 30%. To improve the performance, an Al_2O_3 (20 nm)/MgO (20 nm) dielectric stack was deposited that exhibited a leakage current density of ~1 × 10^{-5} mA/cm^2 at 1 V, which corresponds to ~4 orders of magnitude lower current density than that of the single layer dielectric. Additionally, a 3-layer Al_2O_3 (10 nm)/MgO (20 nm)/Al_2O_3 (10 nm) stack also shows a leakage current density reduction of ~4 orders of magnitude, and a reduced density of interface states while remaining a high-k dielectric. The density of interface states was estimated to be between 6.8 × 10^{11} eV^{-1} cm^{-2} and 1.5 × 10^{12} eV^{-1} cm^{-2} for the 3-layer stack using the photo-assisted C-V method.

1. Introduction

Conventional silicon technology widely used today for electrical power conversion has been developed over the years such that fundamental physical limits are now being reached [1,2]. Thus, consideration is currently being given to alternative materials like GaN. Along with its III-Nitride family of compounds, GaN has already been used for a wide range of applications including solid state lighting, lasers, thermoelectricity, photovoltaics, and sensors, [3–8] due, in part, to its wide bandgap (~3.4 eV) which results in high critical electric fields and breakdown voltages. This property also gives it high figures of merit for high power applications and makes it more attractive than silicon for high speed, power, and temperature applications [9]. However, challenges remain despite these benefits.

One such challenge is the difficulty of growing wide bandgap and high-k dielectrics on GaN with very good interface quality and low interface trap density which is a necessity for a number of high-power devices. Several dielectrics have already been examined including: SiO_2 [10], Ga_2O_3 (Gd_2O_3) [11], ZrO_2 [12], HfO_2 [12], Sc_2O_3 [13], BeO [14], MgO [15–17], and Al_2O_3 [18]. Among these, rock-salt MgO could be an excellent choice because not only does it have a similar lattice constant to wurtzite GaN (−6.5% strain), but it also has a wide bandgap of ~8 eV and a relatively high k-value of 9.8 [19]. The potential of MgO has motivated several studies. MgCaO, a ternary alloy of MgO and CaO, has been characterized in the work done by Lou et al [20]. Gila and coworkers have also reported on the electrical properties of MgO grown by MBE on GaN as well as some of its limitations [21]. A key limitation of MgO revealed in these studies is a low breakdown field which is unfavorable for high power applications.

In this work, we investigate the electrical properties of MgO grown by atomic layer deposition (ALD) on GaN. We show via current versus voltage (I-V) and capacitance versus voltage (C-V) measurements that MgO on GaN exhibits high levels of leakage current and a high density of interface states. However, by capping the MgO layer with a sufficiently thick Al_2O_3 layer, remarkable reductions in leakage current density (at 1 V) of ~4 orders of magnitude can be achieved. By using an Al_2O_3/MgO/Al_2O_3 dielectric stack, a similar reduction in leakage current density can be achieved while also reducing the density of interface states and preserving a high-k dielectric constant.

2. Experimental procedure

In order to investigate the electrical properties of MgO grown on GaN, MOS capacitors were fabricated using GaN/sapphire templates

* Corresponding author.
E-mail addresses: ono215@lehigh.edu (O.N. Ogidi-Ekoko), tansu@lehigh.edu (N. Tansu).

https://doi.org/10.1016/j.sse.2020.107881
Received 28 February 2020; Received in revised form 10 July 2020; Accepted 18 August 2020
Available online 27 August 2020

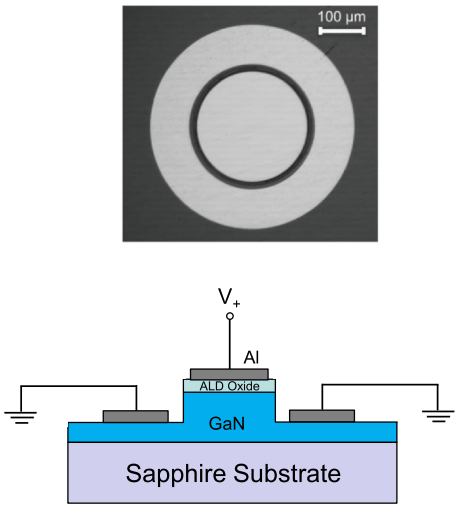

Fig. 1. (a) Microscope image showing top view of MOS capacitor with a gate diameter of 280 μm (b) Cross section of MOS capacitor with ALD-grown oxide.

grown by metal–organic chemical vapor deposition (MOCVD). The GaN epilayers used were doped n-type with Si at a background carrier density of n = ~7.5 × 10^{18} cm^{-3}. The GaN/sapphire templates were first cleaned using a 1:1 HCl:H_2O solution for 10 min followed by a deionized water rinse. Subsequent to the cleaning, the dielectrics were formed by ALD, which allows for conformal and very precisely controlled deposition down to the atomic level by self-limiting surface reactions [22]. Three different configurations of multilayer dielectric stacks were deposited on the GaN. The first case comprises a single 20 nm thick MgO layer that is capped with a 1 nm thick Al_2O_3 capping layer. In this instance, the capping layer was deposited solely for the purpose of protecting the MgO layer from degradation that occurs from exposure to normal atmospheric conditions [23]. The second case is comprised of a 20 nm or 40 nm thick MgO layer followed by a 20 nm or 40 nm thick Al_2O_3 layer. The third case consists of a 10 nm thick layer of Al_2O_3, followed by a 20 nm thick layer of MgO, capped with an additional 10 nm thick layer of Al_2O_3. The schematic of the fabricated MOS structure with the lateral metal contacts used in our study is shown in Fig. 1.

The ALD growth was done by loading samples into a growth chamber primed to a temperature of 200 °C. The precursors used for the MgO deposition were bis (ethylcyclopentadienyl) magnesium and water while trimethylaluminum (TMAl) and water precursors were used for the Al_2O_3 deposition. The oxide-coated samples were then patterned with circle-shaped photoresist by photolithography with diameters of 300 μm. Then the MgO and Al_2O_3 layers were etched using HCl and H_3PO_4 etchants respectively, in order to selectively expose the GaN. The exposed GaN was etched down by Cl-based inductively coupled plasma (ICP) etching to a depth of 1.5 μm to form circular mesas and a good contact layer. Aluminum ohmic contacts were formed on top of the dielectrics and as a ring around the mesa by electron beam evaporation and lift-off.

Three types of measurements were done on the MOS capacitors: current versus voltage (I-V), capacitance versus voltage (C-V), and conductance versus voltage (G-V) measurements. The G-V characteristic was measured simultaneously with the C-V characteristic in order to extract the phase angle of the impedance of the MOS capacitor and thus determine the actual nature of capacitive behavior at each data point. The I-V measurements were done using a Keithley 2450 sourcemeter while the C-V and G-V measurements were done using an HP 4194A impedance/gain-phase analyzer. In all cases, the semiconductor contact was grounded, and the measurements were done in the dark at room temperature.

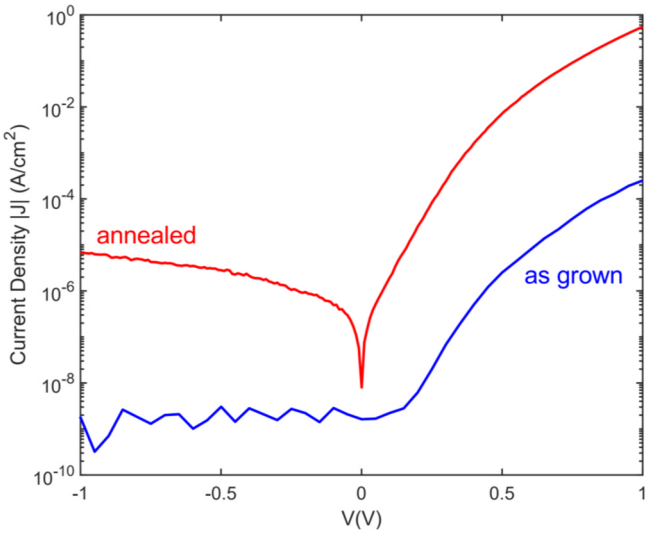

Fig. 2. J-V characteristics of an Al_2O_3 (1 nm)/MgO (20 nm) gate dielectric on GaN for as grown (blue) and after a forming gas anneal (red). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

3. Results and discussion

Fig. 2 shows representative J-V characteristics for a MOS capacitor with a 20 nm thick MgO layer capped with 1 nm of Al_2O_3 under two different conditions: as grown and after a 15-minute rapid thermal anneal (RTA) in forming gas ambient (95% N_2 + 5% H_2) at 450 °C. The voltage sweep started at −1 V and was stepped up to 1 V. The as-grown sample shows a leakage current density of 0.25 mA/cm^2 at 1 V and after annealing, a higher leakage current density of ~1 mA/cm^2 at the same voltage is measured. Extensive measurements of similar as-grown MOS capacitors showed leakage current densities in the range of 1 × 10^{-4} A/cm^2 to 1 A/cm^2 at 1 V. The high level of leakage current for the as-grown sample is comparable to reported values for MgO grown by MBE on GaN [21]. Although annealing with forming gas is often used to reduce the density of interface states and can sometimes help reduce the leakage current density [24,25], under these annealing conditions, a reduction in leakage current was not achieved.

The means of current conduction in insulators is typically tunneling through a bandgap barrier, either by direct tunneling or Fowler-Nordheim tunneling [24]. Given the wide bandgap of MgO (8 eV), its band offsets to GaN (ΔE_C = ~3.3 eV, ΔE_V = 8–1.06 eV) [26,27] and the relatively thick barrier of 20 nm, the high levels of leakage current exhibited by the MgO layer are unlikely to be due to either direct tunneling or Fowler-Nordheim tunneling as these are very sensitive to the barrier height and width [24]. Thus, the leakage current may be attributed to trap-assisted tunneling where defects in the MgO layer introduce trap states within the bandgap that effectively reduce the barrier heights for electron tunneling. In our previous work, x-ray diffraction (XRD) and electron backscatter diffraction (EBSD) data obtained for ALD MgO on MOCVD GaN (0002) template showed two highly-oriented (1 1 1) domains in the MgO crystal structure [28]. A possible explanation for the leakage current could thus be that it occurs primarily through the grain boundaries of these domains. The exact mechanism of this leakage needs to be further investigated as it presents a critical challenge that must be overcome if MgO is to be used as a gate dielectric for GaN-based power devices.

In order to mitigate the current leakage through MgO, a multilayer dielectric stack was considered. A (thicker) layer of Al_2O_3 was deposited over the MgO on GaN. Thus, the benefit of the MgO-GaN lattice structure compatibility was maintained while taking advantage of the insulating properties of the Al_2O_3 layer and what should be an overall

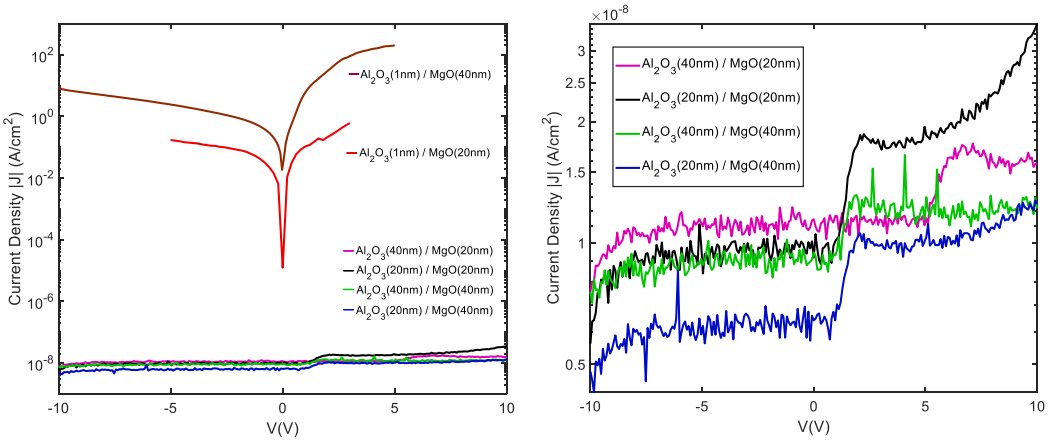

Fig. 3. (a) J-V characteristics comparing as-grown Al_2O_3/MgO stacked gate dielectrics with various thicknesses on GaN. (b) J-V characteristics of bilayer samples expanded for clarity.

high-k dielectric. Fig. 3 summarizes the results of I-V measurements of Al_2O_3/MgO stacks with four-layer thickness permutations of 20 and 40 nm. These are compared to thinner stacks of 1 nm thick Al_2O_3 on 20 nm or 40 nm thick MgO. The measurements are swept from negative voltages to positive. For the single-layer MgO MOS capacitors (the samples having a 1 nm Al_2O_3 cap), the 40 nm thick MgO layer exhibits higher leakage current than the 20 nm layer. This suggests that a high incidence of current conduction pathways exist in the MgO layer, such that the MgO layer remains very leaky even at double the dielectric thickness. In all 4 cases of the thicker bilayer dielectrics, there is a remarkable reduction of the leakage current through the dielectric stack by over 4 orders of magnitude (at a gate voltage of 1 V) relative to the Al_2O_3 (1 nm)/MgO (20 nm or 40 nm) dielectric. For the dielectric stacks with 20 nm thick MgO, the leakage current decreases with increasing thickness of the Al_2O_3 layer, despite its lower bandgap relative to MgO, suggesting that the Al_2O_3 layer itself has better insulating properties than MgO. A similar trend is observed for the 40 nm thick MgO devices. It is worth noting that the improvement in the insulating properties of the dielectric stack varies only slightly when changing the thickness of the capping layer (Al_2O_3) at these lower voltages. These improvements may be further enhanced by the utilization of an alternative dielectric because Al_2O_3 films are limited to suppressing gate leakage in MOS structures due to their susceptibility to trap-assisted tunneling [29].

Fig. 4(a) and (b) show C-V hysteresis curves for Al_2O_3 (1 nm)/MgO (20 nm) and Al_2O_3 (20 nm)/MgO (20 nm) measured at 100 kHz before and after annealing the MOS capacitor for 15 min in forming gas ambient (95% N_2 + 5% H_2) at 450 °C. In both cases, the first sweep direction was from depletion towards the accumulation region and the second was from accumulation towards the depletion region. For the as-grown Al_2O_3 (1 nm)/MgO (20 nm) structure, the C-V characteristics show a capacitance value of about 0.1 μF/cm^2 at ~3 V. For the annealed case, the C-V curve shows an early roll-off at 3 V (less than in the as-grown case) which indicates that the gate dielectric is lossy. A negative shift in the flatband voltage dielectric indicates a reduction in fixed oxide charges after annealing. The multilayer Al_2O_3 (20 nm)/MgO (20 nm) sample, on the other hand, shows a slight reduction in hysteresis after annealing, implying a slight decrease in oxide trapped charge.

To ascertain the phase angle of the equivalent impedance represented by the MOS Capacitor, we measured the G-V characteristics of the MOS capacitors. In the ideal case, the impedance of a MOS capacitor would be a pure capacitive reactance with a phase angle of −90°. However, in practice, losses are present which increase the phase angle. These losses can be modeled as a resistor in parallel with the MOS capacitor and needs to be taken into account for the analysis. For the annealed Al_2O_3 (1 nm)/MgO (20 nm) MOS capacitor, at 3 V, the phase angle was found to be −6.61°, based on the concurrently measured G-V characteristics, confirming that the MOS capacitor is not ideally capacitive but lossy. Thus, an extracted value of the dielectric constant that can be obtained from the maximum capacitance value using the C = ϵA/d relation is inaccurate.

In contrast, the annealed Al_2O_3 (20 nm) / MgO (20 nm) dielectric had a phase angle of −89.2° at 15 V, which is closer to the –90° of an ideal capacitor. A wide hysteresis loop was observed in both cases, indicative of an increase in the density of oxide trapped charge. The equation C′ = ϵ/d is used to extract the dielectric constant, ϵ (where C' is the normalized capacitance and d is the thickness of the dielectric). For these samples, we determined the actual dielectric thicknesses of 24 nm and 22 nm for MgO and Al_2O_3 respectively by ellipsometry, and the extracted effective dielectric constant is 4.52ϵ_0 (where ϵ_0 is the free space dielectric constant). The MOS capacitor is then modeled as a series combination of a 24 nm-thick MgO MOS capacitor and a 22 nm-thick Al_2O_3 MOS capacitor $\left(\frac{1}{C'_{eff}} = \frac{1}{C'_{Al_2O_3}} + \frac{1}{C'_{MgO}}\right)$. The C-V characteristics of a 20 nm-thick Al_2O_3 MOS capacitor were measured and these are presented in Fig. 4(d). Note that we use the actual ellipsometry-measured thicknesses for all calculations. From the accumulation capacitance, the dielectric constant of our ALD Al_2O_3 is extracted as 8.56ϵ_0. Using this dielectric constant (or accumulation capacitance) for Al_2O_3 and using a measured accumulation capacitance estimate of less than 0.095 μF/cm^2 for the overall bilayer MOS capacitor, the dielectric constant of the MgO layer is measured to be ~3.56ϵ_0, which is much lower than the widely accepted value of 9.8 for bulk MgO [19]. This discrepancy is explained by the high resistive losses of the MgO layer. Fig. 4(c) compares C-V curves for 4 different combinations of 20 nm and 40 nm thicknesses of Al_2O_3/MgO. The thickest dielectric combination (Al_2O_3 (40 nm)/MgO (40 nm)) appears to have the least accumulation capacitance, as is to be expected, given the C′ = ϵ/d relationship (where C' is the normalized capacitance, ϵ is the effective permittivity of the dielectric and d is the overall thickness). Keeping the bottom oxide layer thickness the same, the trend shows a positive shift in flatband voltage as the top layer thickness is increased. This can be explained by an increase in the fixed oxide charge with the increased top layer oxide thickness.

Due to the leakage characteristics of the MgO dielectric layer, a different approach was needed to extract the dielectric constant of MgO. The approach taken was to grow a 20 nm thick MgO layer sandwiched between two 10 nm thick Al_2O_3 layers. This dielectric stack provides two insulating layers on either side of the MgO and ensures that the lossy MgO layer is electrically isolated by the Al_2O_3 layers, allowing for a more accurate value of the MgO dielectric constant to be extracted. The results are presented in Figs. 5 and 6. Fig. 5 shows the J-

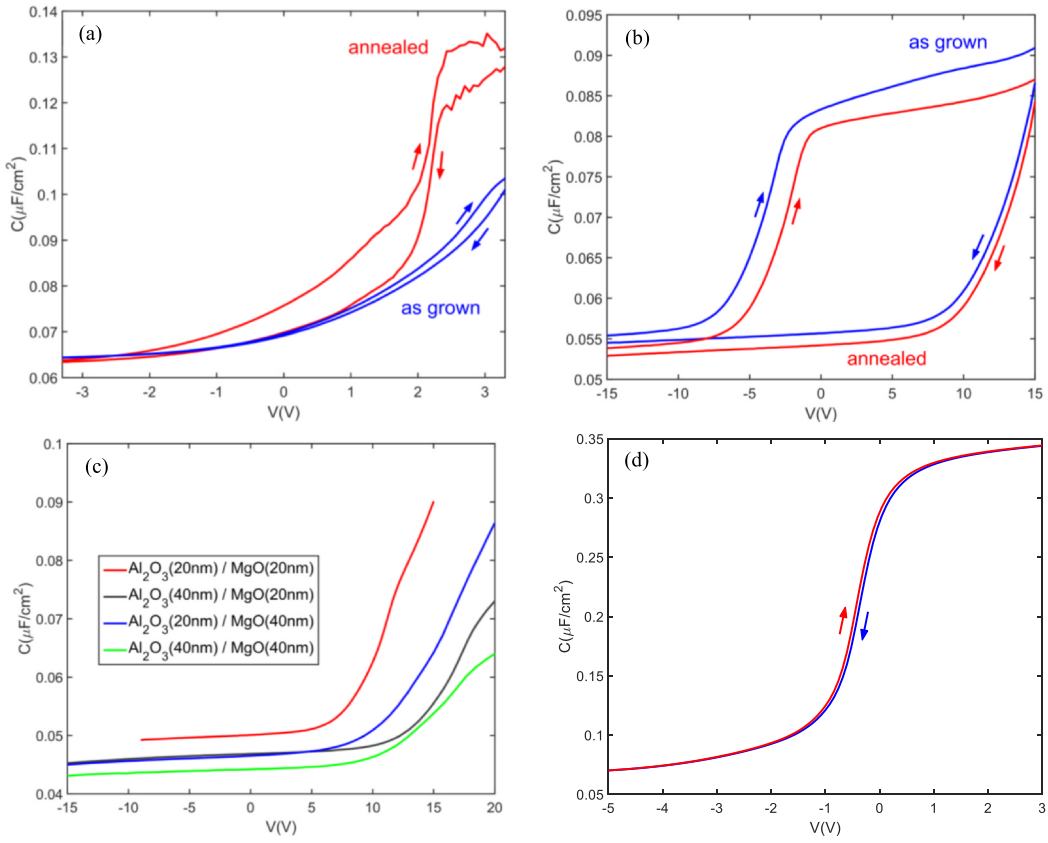

Fig. 4. C-V characteristics for (a) Al_2O_3 (1 nm)/MgO (20 nm) MOS capacitor as grown (blue lines) and after a forming gas anneal (red lines) (b) Al_2O_3 (20 nm)/MgO (20 nm) MOS capacitor as grown (blue lines) and after a forming gas anneal (red lines) (c) gate stack MOS capacitors on GaN/Sapphire, sweeping from negative voltages to positive. (d) Al_2O_3 (20 nm) on GaN / Sapphire showing low hysteresis. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

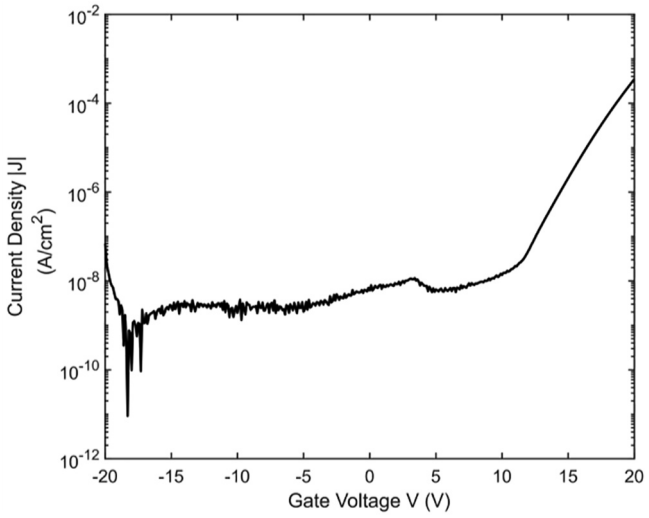

Fig. 5. J-V Characteristics of Al_2O_3(10 nm)/MgO (20 nm)/Al_2O_3 (10 nm)/GaN MOS capacitor.

V characteristics of the MOS capacitor. The leakage current density of 1×10^{-8} A/cm^2 at 1 V is largely comparable to that of the Al_2O_3 (20 nm)/MgO (20 nm) case discussed earlier. The charging effect that causes a shift in the J-V curve is also present in this stack. The switch in the direction of current flow occurs at about −18 V rather than at 0 V. This shift indicates that there are stored charges in the oxide layer(s) and interface traps.

The C-V characteristics of the 3-layer dielectric, Al_2O_3 (10 nm)/MgO (20 nm)/Al_2O_3 (10 nm), are summarized in Fig. 6. Fig. 6(a) shows a hysteresis plot with the first sweep from depletion to accumulation and the second sweep in the reverse direction. The plot qualitatively shows a noticeably smaller hysteresis loop than either the double layer dielectric stacks considered earlier, which is a strong indication of a much-reduced oxide trapped charge density. The frequency dispersion curve in Fig. 6(b) is for the same sample with ac frequencies from 21.5 kHz to 1 MHz and with sweep direction from depletion to accumulation. These plots represent a significantly reduced frequency dispersion and hysteresis from the other dielectric stacks considered and is indicative of a reduction in the densities of interface states and oxide trapped charge. From the accumulation capacitance, the dielectric constant of MgO is obtained by modeling the dielectric as a series combination of 3 capacitors i.e. 2 equally thick Al_2O_3 layers (11 nm each as measured by ellipsometry) and an MgO dielectric capacitor of 24 nm thickness (as measured by ellipsometry). By using the relations $C' = \epsilon/d$ and $1/C' = 1/C_1' + 1/C_2' + 1/C_3'$, where C' is the measured normalized accumulation capacitance and C_1', C_2', and C_3' are the normalized capacitances of the 3 different layers, the extracted value of the MgO dielectric constant was found to be 8.92 which is closer to the known value of 9.8 [19]. For the extraction of ϵ_{MgO} using the above relations, the dielectric constant of Al_2O_3 was assumed to be $8.56\epsilon_0$ as determined from the accumulation capacitance of Fig. 4(d) and the thicknesses used were those obtained from ellipsometry measurements (24 nm for MgO and 11 nm for each Al_2O_3 layer). Fig. 6(c) shows a phase angle plot obtained from conductance measurements of the triple layer dielectric. The phase angle of −89.5° obtained in accumulation confirms that the loss through the MgO layer has been reduced by the Al_2O_3 barrier layer adjacent to the GaN surface.

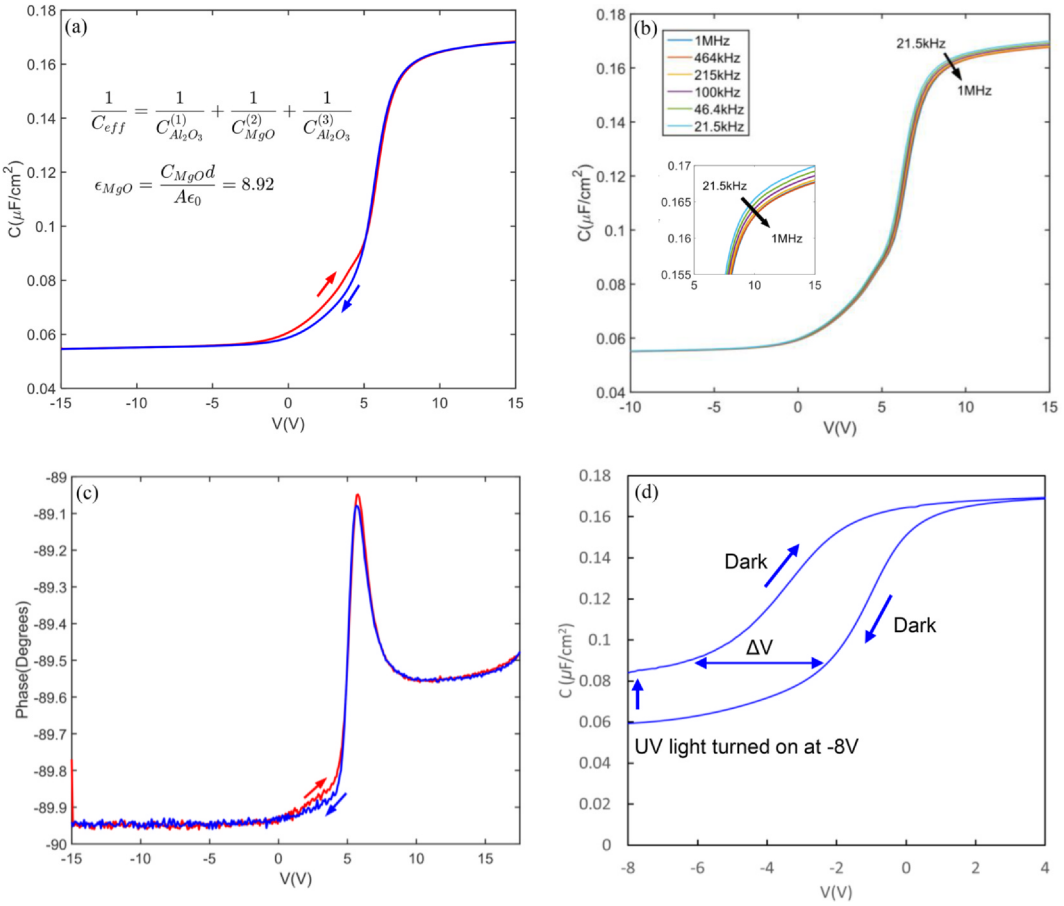

Fig. 6. C-V characteristics of Al_2O_3 (10 nm)/MgO (20 nm)/Al_2O_3 (10 nm) MOS capacitor. (a) Hysteresis plot at 100 kHz (b) Frequency dispersion plot. Measurements were done from negative to positive voltages and from low to high frequencies (c) Phase-V plot at 100 kHz (d) Photo-assisted C-V plot for D_{it} measurement. First sweep was done from accumulation towards inversion in the dark, UV light was turned on and then swept back towards accumulation in the dark.

The interface trap density is also of interest in this work. The total number of interface states across the band gap can be estimated by the photo-CV technique, also used in previous reports for estimating the average interface trap density, D_{it}, for GaN [30–33]. To apply this technique, the gate voltage was swept from accumulation to inversion (positive to negative) while dark. While holding the bias constant in inversion, a UV source (266 nm laser) was used to increase the carrier generation rate and populate the inversion layer. Once the inversion layer was formed, the UV source was turned off and the sample was swept back towards accumulation. While dark, electrons captured in the deep-level states cannot emit into the conduction band due to unfavorably long emission times that increase exponentially with energy separation [24,33]. When the UV light is turned on, minority carriers are generated and an inversion layer is formed, leading to an increase in capacitance. Fig. 6(d) shows the results obtained from our measurement. The shift between the pre-illumination and post-illumination C-V curves, ΔV, reflects the differences in charging of deep level states with and without illumination. Using the ΔV shift, the average D_{it} can be calculated by $D_{it} = C_{ox}\Delta V/qE_g$, where C_{ox} is the oxide capacitance per unit area, E_g is the GaN bandgap and q is the electron charge [30]. Based on this equation, we estimate the average interface trap density of the Al_2O_3 (10 nm)/MgO (20 nm)/Al_2O_3 (10 nm) sample to be between 6.8 × 10^{11} eV^{-1} cm^{-2} and 1.5 × 10^{12} eV^{-1} cm^{-2}. Finally, Table 1 summarizes key findings obtained from representative samples of the MOS capacitors considered in this work.

Table 1
Measured and extracted Parameters for select dielectric stacks.

Dielectric Stack	ϵ_{MgO}	Phase Angle	Current density at 1 V
Al_2O_3 (1 nm) MgO (20 nm)		−6.61°	~2.5 × 10^{-4} A/cm²
Al_2O_3 (20 nm)/MgO (20 nm)	3.56	−89.2°	~1 × 10^{-8} A/cm²
Al_2O_3 (10 nm)/MgO (20 nm)/ Al_2O_3 (10 nm)	8.92	−89.5°	~1 × 10^{-8} A/cm²

The dielectric constant of Al_2O_3 was set at 8.56 for the ϵ_{MgO} value obtained from the Al_2O_3 C-V curve. An accurate value of ϵ_{MgO} cannot be extracted in the first two cases due to the lossy MgO layer.

4. Conclusion

MgO, though apparently promising as a gate dielectric for GaN-based devices, presents certain critical challenges for its usage, especially the low dielectric breakdown voltage and high density of interface state and oxide traps as observed from current versus voltage and capacitance versus voltage measurements. High leakage current densities of ~2.5 × 10^{-4} A/cm² were observed for a 20 nm thick MgO layer at a gate voltage of 1 V. Annealing tests performed did not improve performance in this respect with increases in the leakage current density of over 3 orders of magnitude and a significant increase in interface state density observed. However, by incorporating MgO into a gate stack dielectric that includes Al_2O_3 layers, significant improvements in overall dielectric quality were seen. A high effective dielectric constant of 8.8 was obtained, while reducing the leakage current density by over 4 orders of magnitude and significantly reducing the interface state density. Phase angle calculations based on conductance versus voltage measurements confirm that the degradation in device quality occurs primarily within the MgO layer and at the MgO/GaN

interface. A further study is required to understand the mechanism by which the leakage current occurs in MgO and additional ways by which it may be reduced.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

The authors would like to acknowledge the support from U. S. Department of Education GAANN (Graduate Assistance in Areas of National Need) Fellowship [JCG], U. S. National Science Foundation (DMR 1505122, DMR 1708227, DMR 1752956, and ECCS 1935295), and Daniel E. '39 and Patricia M. Smith Endowed Chair Professorship Fund. The work is also supported via the Accelerator Program by the Office of the Vice President for Research at Lehigh.

References

[1] Flack TJ, Pushpakaran BN, Bayne SB. GaN technology for power electronic applications: a review. J Electron Mater 2016;45(6):2673–82.
[2] Baliga BJ. Power semiconductor device figure of merit for high-frequency applications. IEEE Electron Device Lett 1989;10(10):455–7.
[3] Tansu N, Zhao H, Liu G, Li XH, Zhang J, Tong H, et al. III-nitride photonics. IEEE Photonics J 2010;2(2):241–8.
[4] Wierer JJ, Tsao JY, Sizov DS. The potential of III-nitride laser diodes for solid-state lighting. Phys Status Solidi (c) 2014;11(3–4):674–677.
[5] Stutzmann M, et al. GaN-based heterostructures for sensor applications. Diam Relat Mater 2002;11(3–6):886–91.
[6] Nakamura S. InGaN-based blue/green LEDs and laser diodes. Adv Mater 1996;8(8):689–92.
[7] Yamaguchi S, Izaki R, Kaiwa N, Yamamoto A. Thermoelectric properties of and devices based on free-standing GaN. Appl Phys Lett 2005;86(25):252102.
[8] Lu N, Ferguson I. III-nitrides for energy production: photovoltaic and thermoelectric applications. Semicond Sci Technol 2013;28(7):074023.
[9] Baliga BJ. Gallium nitride devices for power electronic applications. Semicond Sci Technol 2013;28(7):074011.
[10] Matocha K, Tilak V, Dunne G. Comparison of metal-oxide-semiconductor capacitors on c- and m-plane gallium nitride. Appl Phys Lett 2007;90(12):123511.
[11] Chang YC, Lee YJ, Chiu YN, Lin TD, Wu SY, Chiu HC, et al. MBE grown high κ dielectrics $Ga_2O_3(Gd_2O_3)$ on GaN. J Cryst Growth 2007;301–302:390–3.
[12] Bothe KM, von Hauff PA, Afshar A, Foroughi-Abari A, Cadien KC, Barlage DW. Electrical comparison of HfO_2 and ZrO_2 gate dielectrics on GaN. IEEE Trans Electron Devices 2013;60(12):4119–24.
[13] Gila BP, Johnson JW, Mehandru R, Luo B, Onstine AH, Krishnamoorthy V, Bates S, Abernathy CR, Ren F, Pearton SJ. Gadolinium oxide and scandium oxide: gate dielectrics for GaN MOSFETs. Phys Status Solidi (a) 2001;188(1):239–242.
[14] Lee SM, Yum JH, Yoon S, Larsen ES, Lee WC, Kim SK, et al. Atomic-layer deposition of single-crystalline BeO epitaxially grown on GaN substrates. ACS Appl Mater Interfaces 2017;9(48):41973–9.
[15] Craft HS, Ihlefeld JF, Losego MD, Collazo R, Sitar Z, Maria J-P. MgO epitaxy on GaN (0002) surfaces by molecular beam epitaxy. Appl Phys Lett 2006;88(21):212906.
[16] Gila BP, Ren F, Abernathy CR. Novel insulators for gate dielectrics and surface passivation of GaN-based electronic devices. Mater Sci Eng: R: Rep 2004;44(6):151–84.
[17] Suzuki R, Kawaharazuka A, Horikoshi Y. MBE growth of GaN on MgO substrate. J Cryst Growth 2007;301–302(SPEC. ISS.):478–481.
[18] Gu S, Chagarov EA, Min J, Madisetti S, Novak S, Oktyabrsky S, et al. Characterization of interface and border traps in ALD Al_2O_3/GaN MOS capacitors with two-step surface pretreatments on Ga-polar GaN. Appl Surf Sci 2014;317:1022–7.
[19] Daude N, Jouanin C, Gout C. Electronic band structure of magnesium and calcium oxides. Phys Rev B 1977;15(4):2399–405.
[20] Lou X, Zhou H, Kim SB, Alghamdi S, Gong X, Feng J, et al. Epitaxial growth of $Mg_xCa_{1-x}O$ on GaN by atomic layer deposition. Nano Lett 2016;16(12):7650–4.
[21] Gila BP, Kim J, Luo B, Onstine A, Johnson W, Ren F, et al. Advantages and limitations of MgO as a dielectric for GaN. Solid-State Electron Dec. 2003;47(12):2139–42.
[22] George SM. Atomic layer deposition: an overview. Chem Rev 2010;110(1):111–31.
[23] Herrero AM, Gila BP, Gerger A, Scheuermann A, Davies R, Abernathy CR, et al. Environmental stability of candidate dielectrics for GaN-based device applications. J Appl Phys 2009;106(7):074105.
[24] Schroder DK. Semiconductor material and device characterization. 3rd ed. Hoboken, New Jersey: John Wiley & Sons Inc; 2006.
[25] Kar S. High permittivity gate dielectric materials. Berlin Heidelberg, Germany: Springer-Verlag; 2013.
[26] Craft HS, Collazo R, Losego MD, Mita S, Sitar Z, Maria J-P. Band offsets and growth mode of molecular beam epitaxy grown MgO (111) on GaN (0002) by x-ray photoelectron spectroscopy. J Appl Phys Oct. 2007;102(7):074104.
[27] Chen J-J, Gila BP, Hlad M, Gerger A. Determination of MgO/GaN heterojunction band offsets by x-ray photoelectron spectroscopy. Appl Phys Lett 2006;88(4):042113.
[28] Goodrich JC, et al. Surface pretreatment and deposition temperature dependence of MgO Epitaxy on GaN by thermal atomic layer deposition. J Cryst Growth 2020;536:125568.
[29] Lee H-P, Bayram C. Investigation of annealed, thin(~2.6 nm)-Al_2O_3/AlGaN/GaN metal-insulator-semiconductor heterostructures on Si(111) via capacitance-voltage and current-voltage studies. Mater Res Express 2019;6(10):105904.
[30] Tan J, Das MK, Cooper JA, Melloch MR. Metal–oxide–semiconductor capacitors formed by oxidation of polycrystalline silicon on SiC. Appl Phys Lett 1997;70(17):2280–1.
[31] Wu YQ, Shen T, Ye PD, Wilk GD. Photo-assisted capacitance-voltage characterization of high-quality atomic-layer-deposited Al_2O_3/GaN metal-oxide-semiconductor structures. Appl Phys Lett 2007;90(14):143504.
[32] Swenson BL, Mishra UK. Photoassisted high-frequency capacitance-voltage characterization of the Si_3N_4/GaN interface. J Appl Phys 2009;106(6):064902.
[33] Hashizume T, Alekseev E, Pavlidis D, Boutros KS, Redwing J. Capacitance–voltage characterization of AlN/GaN metal–insulator–semiconductor structures grown on sapphire substrate by metalorganic chemical vapor deposition. J Appl Phys 2000;88(4):1983–6.

Onoriode N. Ogidi-Ekoko received a B.S. degree and M.S. degree in electrical engineering from Lehigh University, Bethlehem, PA, USA in 2015 and 2016 respectively and is currently pursuing a PhD in electrical engineering at the same university. His research interests include III-Nitride applications for power devices and VCSEL technology.

Justin C. Goodrich received B.S. degrees in physics (2013) and electrical engineering (2014) from Lehigh University, Bethlehem, PA, USA. He worked for two years at POWER Engineers in Mount Laurel, NJ, USA before returning to Lehigh in 2016 to pursue his PhD in electrical engineering at Lehigh's Center for Photonics and Nanoelectronics (CPN). His research interests include III-Nitride materials for optoelectronic and power applications.

Alexandra J. Howzen received the B.S. degree in Materials Science and Engineering from The Pennsylvania State University, State College, PA, USA, in 2018 working on the impact of treatment and relative humidity on the structure and properties of aluminosilicate glasses. Currently she is pursuing her Ph.D. degree at Lehigh University, Bethlehem, PA, USA with Dr. Nicholas C. Strandwitz. Her current research involves designing and building an atomic layer deposition (ALD) chamber with *in situ* electron diffraction capabilities for investigating the amorphous to crystalline transition of metal oxide films. She is also investigating the impact of surface species, substrate, and ambient environment on the resulting structure of epitaxial films.

Matthew R. Peart received the B.S. degree in electrical engineering from Villanova University, Villanova, PA, USA, and the M.S. degree in electrical engineering from Lehigh University, Bethlehem, PA, USA, where he is currently pursuing the Ph.D. degree. He held research and development positions with Intel, Hillsboro, OR, USA, and Broadcom Limited, Breinigsville, PA, USA. His current research interests include III-nitride device physics and numerical simulation.

Nicholas C. Strandwitz received the B.S. degree in engineering science from Pennsylvania State University, State College, PA, USA, in 2004, and the Ph.D. degree from the Materials Department, University of California, Santa Barbara, CA, USA, with Prof. Galen D. Stucky. His current research interests include new chemistries and techniques in atomic layer deposition and interfacial electronic properties between semiconductors and metal oxides.

Jonathan J. Wierer, Jr. (M'95–SM'12) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana–Champaign, IL, USA, in 1994, 1995, and 1999, respectively. He was with Philips-Lumileds, San Jose, CA, USA, and Sandia National Laboratories, Albuquerque, NM, USA. He is currently an Associate Professor with Lehigh University, Bethlehem, PA, USA. He has authored or co-authored over 150 publications and conference publications, and holds 37 patents.

Nelson Tansu is the Daniel E. '39 and Patricia M. Smith Endowed Chair Professor in the Department of Electrical and Computer Engineering (ECE) and Center for Photonics and Nanoelectronics (CPN) at Lehigh University. He had made advances to the invention and innovation, fundamental sciences, and device technologies of III-V and III-Nitride semiconductors. He has authored 146+ refereed journals and 300+ conference publications. He holds over 18 US patents. Tansu is an elected Fellow of the National Academy of Inventors (NAI) and ISI/Clarivate Analytics Highly Cited Researcher. Tansu received the Libsch Research Award (2008, 2019), Lehigh University's highest faculty research award. His life story as a professor was published in the best-selling children's book "Nelson the Boy who Loved to Read".