Reflective Parametric Frequency-Selective Limiters With Sub-dB Loss and μWatts Power Thresholds

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***Abstract*— This article describes the design methodology to achieve reflective diode-based parametric frequency-selective limiters (pFSLs) with low-power thresholds (P_{th}) and sub-dB insertion-loss values ($IL^{s.s}$) for driving power levels (P_{in}) lower than P_{th}. In addition, we present the measured performance of a reflective pFSL designed through the discussed methodology and assembled on an FR-4 printed circuit board (PCB). Due to its optimally engineered dynamics, the built pFSL can operate around ∼2.1 GHz while exhibiting record-low P_{th} (−3.4 dBm) and $IL^{s.s}$ (0.94 dB) values. Furthermore, while the pFSL can selectively attenuate undesired signals with power ranging from −3.4 to 13 dBm, it provides a strong suppression level (IS > 12.0 dB) even when driven by much higher P_{in} values approaching 28 dBm. Such measured performance metrics demonstrate how the unique nonlinear dynamics of parametric-based FSLs can be leveraged through components and systems compatible with conventional chip-scale manufacturing processes in order to increase the resilience to electromagnetic interference (EMI) and even of wireless radios designed for low-power consumption and, consequently, characterized by a narrow dynamic range.**

***Index Terms*— Auxiliary generators, frequency-selective limiters (FSLs), interference suppression (IS), nonlinear dynamics, parametric components.**

I. Introduction

THE growing Internet of Things (IoT) is challenging the sharing of the available spectrum by an increasing number of wireless devices that interfere with each other. As a result, the performance of the existing radios keeps being affected more and more heavily by strong electromagnetic interference (EMI), lowering the capability to receive useful information and threatening the integrity of any receivers (RXs), especially when designed for low-power consumption. For this reason, adaptive RXs with interference filtering capabilities have received growing attention in recent research efforts. In particular, radio frequency (RF) power-sensitive components known as frequency-selective limiters (FSLs) [1] have recently been researched to provide low-power RXs with the unique ability to instinctually suppress received EMI without affecting the capability to simultaneously receive the desired lower power useful information. Due to their power-sensitive electrical response, FSLs can address key operational needs, such as a higher resilience to EMI in modern radars or the protection of any critical communication systems from high-power microwave attacks or jamming. Two main classes of FSLs have been previously discussed. One class relies on ferrite-based components [2]–[12], exploiting different types of nonlinear mechanisms in thin-film magnetic materials. While ferrite-based FSLs employing different technologies have been explored, the intrinsic losses associated with any usable thin-film magnetic materials render these FSLs prone to high insertion-loss values for small signals ($IL^{s.s}$ up to 10 dB). In addition, since the magnetic materials used by ferrite-based components cannot be manufactured through fabrication processes compatible with the ones used for complementary–metal–oxide semiconductor (CMOS) integrated circuits (ICs), ferrite-based FSLs cannot be monolithically integrated with the other active and passive components forming the receive and transmit modules of commercial radios.

Alternatively, diode-based FSLs [13]–[19] have been investigated. Such components rely on the electrostatic nonlinearities of solid-state devices and systems to achieve compact FSLs that can be integrated with the other components of commercial and military RF chains to ensure the highest degree of miniaturization. Yet, the fully passive diode-based FSLs reported to date exhibit much higher power thresholds than those attained by the state-of-the-art (SoA) ferrite-based counterparts [9], thus not being adequate to protect the majority of the integrated front ends used by IoT systems. Just recently, a diode-based FSL relying on an active feedback loop, using a board-level power detection and an electromechanically tunable cavity resonator, has been reported [20]. Yet, due to the required intense operations allowing it to reconfigure its transmission characteristics and regardless of its exceptionally low threshold granted by the use of a sensitive power detector, this reported FSL is not ideal when miniaturized radios with a low-power consumption are needed.

Driven by the need of developing a new class of passive open-loop phase noise cleaners, known as parametric filters [21], [22], our group has recently investigated the stability of large-signal periodic regimes in diode-based 2:1 parametric frequency dividers (PFDs [23]), even describing

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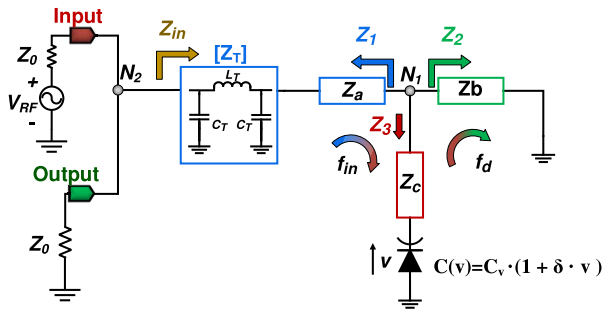

Fig. 1. Simplified schematic of a reflective pFSL including three complex impedances (Z_a, Z_b, and Z_c), a quarter-wave transformer ($[Z_T]$), a dc-biased diode and a real termination (Z_0) for both its input and output ports. The impedances (Z_1, Z_2, and Z_3) seen from node N_1 toward Z_a, Z_b, and Z_c, respectively, are also indicated along with the impedance (Z_{in}) seen from the node N_2 toward N_1. In favor of an easier visualization, no dc-biasing network is shown here.

a new design methodology to achieve exceptionally low parametric power thresholds (P_{th}) in lumped or distributed onboard PFD implementations. By further exploiting the outcomes of this investigation, we recently developed a new battery-less, chip-less, and harvester-free sensor tag [24], referred to as subharmonic tag (SubHT), utilizing an 860-MHz diode-based parametric circuit made of lumped off-the-shelf components assembled on a printed substrate. Through the SubHT, we demonstrated that the proper engineering of the dynamics of diode-based parametric circuits permits to achieve extraordinarily low P_{th} values (-18 dBm for an input frequency of 860 MHz) approaching the power threshold attainable by SoA ferrite-based FSLs, even when relying on low quality factor (<80) components and on packaged diodes with junction capacitance in the pF-range. Furthermore, the demonstration of the SubHT allowed us to unveil a unique dynamical characteristic for parametric circuits. Such circuits, in fact, can exhibit a much lower conversion loss (CL) from an ultralow-power ($\ll$1mW) input signal to a subharmonic output signal than the minimum CL obtained by any frequency doubling counterparts relying on the same nonlinear reactance and on the same circuit topology. This powerful feature has been leveraged in this work to achieve a tunable diode-based parametric FSL (pFSL) that can exhibit record-low P_{th} (-3.4 dBm for an input frequency close to 2.1 GHz) and $IL^{s.s}$ (as low as 0.94 dB) values, along with a significant interference suppression (IS) reaching 5.4 dB for driving power levels (P_{in}) lower than 13 dBm, even exceeding 12.0 dB for $P_{in} > 28$ dBm. In the following, we will first present the main design criteria and tradeoffs to consider in order to achieve pFSLs with low P_{th} and low $IL^{s.s}$. Later, we will discuss the perturbation-based circuit simulation approach that can be followed to predict and optimize the IS value achieved by pFSLs directly from the steady-state circuit simulated electrical response. Finally, we will showcase the measured performance of a $\sim$2.1 GHz diode-based pFSL that we designed and built on an FR-4 printed circuit board (PCB) in this work.

II. Reflective pFSLs—Design Methodology

A pFSL is a nonlinear circuit able to instinctually suppress the power flow between its ports when driven by strong RF signals with power (P_{in}) exceeding a certain threshold (i.e., P_{th}). In order to do so, pFSLs rely on the nonlinear dynamics of diode-based parametric circuits to trigger a period-doubling mechanism leading to abrupt changes in the pFSLs' electrical responses for P_{in} values exceeding P_{th}. For low-power RF front ends, in particular, pFSLs are well-suited to enhance resilience to interference, especially when combined with circuit-level linearity improvement methods, such as those discussed in [25]–[27]. Two main types of pFSLs can be designed, namely, the absorptive and the reflective pFSLs. Absorptive pFSLs rely on directional couplers with output and coupled ports terminated on two parametric networks, including one or more diodes. The reliance on such a circuit topology renders absorptive pFSLs capable to absorb strong RF signals with power exceeding their P_{th} value. Yet, absorptive pFSLs are characterized by significant IS values only within a narrow range of input power levels centered around an optimal value (P_{opt}) that dynamically minimizes the return loss (RL) at the input of their parametric networks. Consequently, absorptive pFSLs exhibit just negligible IS levels for P_{in} largely exceeding P_{opt}. Hence, they are challenging to use in the presence of continuously varying interference power levels, such as the ones frequently captured by mobile radios in practical electromagnetic (EM) scenarios, since they leave cascaded components exposed to severe risks of being damaged by EMI with power higher than P_{opt}. On the contrary, reflective pFSLs exploit the dynamics of diode-based passive circuits to trigger sudden and large increases of RL (at both the pFSLs' input and output ports) in the presence of P_{in} values exceeding their P_{th}. Reflective pFSLs also exhibit the highest frequency selectivity around an optimal P_{in} value, which depends on the maximum voltage that can be applied across the diode before triggering any periodic transitions between the diode's reverse and forward conductions. Nevertheless, due to their design characteristics, reflective pFSLs can exhibit a high IS even in the presence of much stronger interference signals, thus lowering the chances that any RXs can be damaged by EMI of extraordinary high power. However, up to date, a consolidated and systematic design flow for reflective pFSLs is still missing. Such a lack of information, along with the complexity of adapting the *ad hoc* simulation techniques developed for parametric circuits to the algorithms used by commercial circuit simulators [28]–[32], has inhibited the design of reflective pFSLs simultaneously achieving low P_{th} and $IL^{s.s}$ values.

In the most simplistic representation, a reflective pFSL can be seen as a two-port passive network, including one diode characterized by a biased capacitance C_v and a corresponding tuning range δ (see Fig. 1), together with a set of components forming a stabilization network for the large signal periodic regimes excited in the circuit by P_{in}. Without any loss of generality, we can assume any reflective pFSLs to be representable through a T-network topology, including the adopted diode, three one-port complex impedances (Z_a, Z_b, and Z_c), and a quarter-wave transformer (labeled as $[Z_T]$) with bandwidth (BW) centered around the value (f_{in}^{opt}) of the input frequency (f_{in}, corresponding to a natural frequency labeled as ω_{in}) at which the minimum P_{th} is desired. While

the transformation stage can be implemented through any existing lumped or distributed circuit topologies, a third-order lumped implementation is assumed here in favor of a simpler analytical treatment. Also, such a two-port network, uniquely identified by an inductance (L_T) and a capacitance (C_T) setting the equivalent characteristic impedance ($Z_{\text{tx}} = (L_T/C_T)^{1/2}$), plays a key role to simultaneously achieve the lowest possible P_{th} and $\text{IL}^{\text{s.s}}$ values in pFSLs. Furthermore, to match the most frequent operational scenario, the same termination (Z_0, equal to 50 Ω) can be considered for the input and output ports. As P_{th} exhibited by pFSLs needs to be as low as possible to ensure that even low-power RXs characterized by a small dynamic range can be protected from EMI, it is crucial to find the optimal design specifications for $[Z_T]$, Z_a, Z_b, and Z_c (from now on, labeled together as $Z_{T,a,b,c}$), allowing to minimize the achievable P_{th}. By relying on the same analytical methodology used to find the P_{th} of PFDs in our recent theoretical investigation [23], P_{th} of the reflective pFSL shown in Fig. 1 can be found as

$$P_{\text{th}} = \frac{|V_{\text{th}}|^2}{8Z_0} = \frac{C_v^4}{2Z_0\delta^2}\left|\frac{G_{\text{eq}}^{(\omega_d)}G_{\text{eq}}^{(\omega_{\text{in}})}\omega_{\text{in}}^2}{\left(Z_1^{(\omega_d)}+Z_2^{(\omega_d)}\right)Z_2^{(\omega_{\text{in}})}}\right|^2. \tag{1}$$

In (1), V_{th} is the voltage level of the input generator with characteristic impedance equal to Z_0 and power available equal to P_{th}. Also, $Z_1^{\omega_d}$ and $Z_2^{\omega_d}$ represent the equivalent impedances seen at the half of the driving frequency (f_d, equal to $f_{\text{in}}/2$ and corresponding to a natural frequency labeled as ω_d) from node N_1 (see Fig. 1) toward Z_a and Z_b, respectively, whereas $Z_2^{\omega_{\text{in}}}$ is the equivalent impedance at f_{in} seen from N_1 toward Z_b. Furthermore, $G_{\text{eq}}^{\omega_{\text{in}}}$ and $G_{\text{eq}}^{\omega_d}$ [see (2) and (3)] are complex functions of $Z_1^{\omega_{\text{in}}}$, $Z_2^{\omega_{\text{in}}}$, and $Z_3^{\omega_{\text{in}}}$ and the impedances $Z_1^{\omega_d}$, $Z_2^{\omega_d}$, and $Z_3^{\omega_d}$, where $Z_1^{\omega_{\text{in}}}$, $Z_2^{\omega_{\text{in}}}$, and $Z_3^{\omega_d}$ are the impedances seen at f_{in} and f_d from N_1 toward Z_a, Z_b, and Z_c

$$G_{\text{eq}}^{(\omega_{\text{in}})} = Z_2^{(\omega_{\text{in}})}Z_3^{(\omega_{\text{in}})} + Z_1^{(\omega_{\text{in}})}\left(Z_2^{(\omega_{\text{in}})}+Z_3^{(\omega_{\text{in}})}\right) \tag{2}$$

$$G_{\text{eq}}^{(\omega_d)} = Z_2^{(\omega_d)}Z_3^{(\omega_d)} + Z_1^{(\omega_d)}\left(Z_2^{(\omega_d)}+Z_3^{(\omega_d)}\right). \tag{3}$$

By replacing (2) and (3) in (1), it is straightforward to notice that the resulting P_{th} expression is a function of all the impedances in the circuit (i.e., $Z_{T,a,b,c}$, Z_0, and the diode impedance) and of the first two coefficients of the linearized capacitance versus voltage characteristic of the biased diode (see Fig. 1). Moreover, since all the impedances in (1)–(3) can be extracted through linear algorithms in any circuit simulators, their synthesis can be numerically tackled aiming at the minimization of P_{th} without running time-consuming nonlinear perturbation-based simulations, such as the ones available to investigate the steady-state large-signal operation of parametric circuits. Nevertheless, similar to what we showed for PFDs in [23], the inspection of (1) after simplifying $G_{\text{eq}}^{\omega_{\text{in}}}$ and $G_{\text{eq}}^{\omega_d}$ with their corresponding expressions in (2) and (3) permits to realize that the minimum P_{th} at $f_{\text{in}}^{\text{opt}}$ can be attained by ensuring that four resonant conditions are satisfied: 1) $Z_1^{(\omega_{\text{in}})}+Z_3^{(\omega_{\text{in}})}$ must be in series resonance at $f_{\text{in}}^{\text{opt}}$ with the lowest real part possible (R_p); 2) $Z_2^{(\omega_d)}+Z_3^{(\omega_d)}$ must be in series resonance at $f_{\text{in}}^{\text{opt}}/2$ with the lowest real part possible (R_d); 3) $Z_2^{(\omega_{\text{in}})}$ must be in parallel resonance at $f_{\text{in}}^{\text{opt}}$ with the highest real part possible; and 4) $Z_1^{(\omega_d)}$ must be in parallel resonance at $f_{\text{in}}^{\text{opt}}/2$ with the highest real part possible. In order to satisfy these resonance conditions through the use of a minimum number of lumped components, both Z_a and Z_b can be synthesized with parallel LC resonators, resonating at $f_{\text{in}}^{\text{opt}}/2$ and $f_{\text{in}}^{\text{opt}}$ and relying on inductors (capacitors) with inductance (capacitance) L_a (C_a) and L_b (C_b), respectively. Furthermore, Z_c can be synthesized with one inductor whose inductance (L_c) is strategically selected to ensure the simultaneous validity of the first two resonant conditions, given the selected L_a and L_b values. Thus, when the resonant conditions mentioned above are satisfied, (1) can be simplified as

$$P_{\text{th}} = \frac{C_v^4}{2Z_0\delta^2}\left(R_pR_d\omega_{\text{in,opt}}^2\right)^2 \tag{4}$$

where $\omega_{\text{in,opt}}$ is equal to $2\pi f_{\text{in}}^{\text{opt}}$ and R_p can be expressed in terms of Z_{tx} [see (5)] when assuming for simplicity $[Z_T]$ to be lossless

$$R_p = R_s + \frac{2Z_{\text{tx}}^2}{Z_0}. \tag{5}$$

In (5), R_s captures the ohmic losses of both Z_a and Z_c along with the ones of the diode. Also, in the derivation of (4), we neglected the impact of $Z_2^{\omega_{\text{in}}}$ and $Z_1^{\omega_d}$ in favor of a simplified analytical treatment and an easier visualization of the main features determining P_{th} in reflective pFSLs. The validity of this approximation is granted by the fact that these two impedances, which are synthesized by two notches, just allow to isolate the signals at $f_{\text{in}}^{\text{opt}}/2$ and $f_{\text{in}}^{\text{opt}}$ in dedicated meshes of the circuit. From (4) and (5), it is evident how the transformation stage plays a key role in lowering R_p with respect to the value that it would have (i.e., $R_s + Z_0/2$) if the resonant conditions were satisfied without using such a transformation stage. Therefore, the adoption of $[Z_T]$ introduces fundamental means to reduce the lowest P_{th} that can be attained by reflective pFSLs. It is useful to simplify (4) by expressing R_s and R_d in terms of the quality factor of the diode (Q_v, relative to an f_{in} value equal to $f_{\text{in}}^{\text{opt}}$) and the ones ($Q_1$ and Q_2), respectively, exhibited at $f_{\text{in}}^{\text{opt}}$ and $f_{\text{in}}^{\text{opt}}/2$ by $Z_1^{\omega_{\text{in}}}+Z_3^{\omega_{\text{in}}}$ and $Z_2^{\omega_d}+Z_3^{\omega_d}$. Also, for pFSLs operating in the ultrahigh-frequency (UHF) range, such as the prototype demonstrated in this work, we can assume Q_1 to be equal to Q_2 (i.e., $Q_{1,2} = Q_l$, being Q_l dependent on the technology of the adopted passive components) and to be significantly higher than Q_v. This simplification is particularly valid when relying on diodes with wide tuning ranges, such as any available hyperabrupt varactors [33]. Consequently, R_s can be considered equal to R_d and can be simplified as follows:

$$R_s = R_d = \frac{1}{\omega_{\text{in,opt}}C_v}\left(\frac{1}{Q_l}+\frac{1}{Q_v}\right) \approx \frac{1}{\omega_{\text{in,opt}}C_vQ_v}. \tag{6}$$

By using (6) in (4), P_{th} can then be rewritten as

$$P_{\text{th}} = \frac{\left(Z_0 + 2C_vQ_vZ_{\text{tx}}^2\omega_{\text{in,opt}}\right)^2}{2Q_v^4Z_0^3\delta^2}. \tag{7}$$

Equation (7) gives us the opportunity to estimate the minimum P_{th} value that can be attained by reflective pFSLs for any given $f_{\text{in}}^{\text{opt}}$ of interest and for a chosen diode's characteristics.

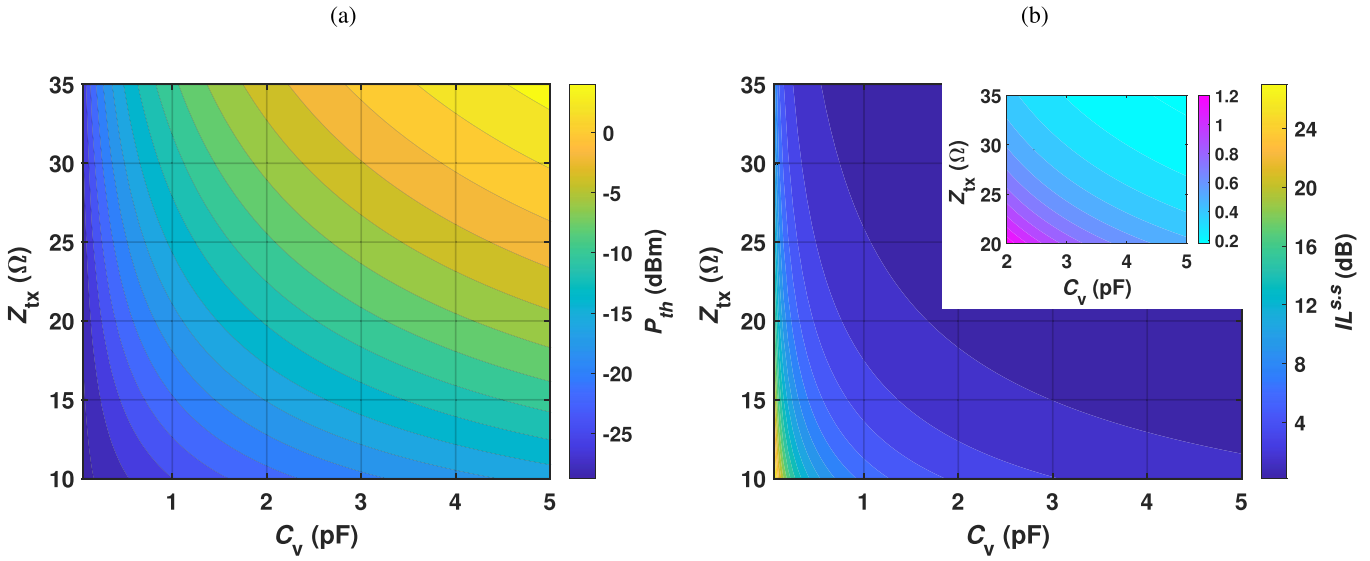

Fig. 2. Minimum P_{th} value (in dBm) computed through (7) in (a) and minimum $\text{IL}^{\text{s.s}}$ value (in dB) computed through (11) in (b) attainable by the reflective pFSL shown in Fig. 1 versus C_v and Z_{tx}. For both (a) and (b), we assumed $Z_0 = 50\ \Omega$, $f_{\text{in}}^{\text{opt}} = 2.1$ GHz, $Q_v = 15$, $\delta = 0.4$, and the validity of the resonant conditions minimizing P_{th}.

As an example, we report a contour-plot capturing P_{th} versus Z_{tx} and C_v [see (7)] in Fig. 2(a), which was analytically derived when assuming: 1) the use of a hyperabrupt varactor (i.e., $\delta \sim 0.4$ and $Q_v \sim 15$) with C_v ranging from 50 fF to 5 pF and 2) $f_{\text{in}}^{\text{opt}}$ of 2.1 GHz (in line with our experimental demonstration).

As evident from Fig. 2(a), reflective pFSLs can achieve low P_{th} values ($\ll$0 dBm) through the strategic adoption of diodes with wide tuning range and low capacitance, along with $\lambda/4$ transformation stages characterized by the minimum realizable characteristic impedance. Nevertheless, since pFSLs also need to exhibit the lowest possible insertion loss for power levels that are lower than P_{th}, the selection of $Z_{T,a,b,c}$ must also be made to ensure a minimum $\text{IL}^{\text{s.s}}$. In order to estimate the $\text{IL}^{\text{s.s}}$ value of the pFSL shown in Fig. 1, we can extract the small-signal scattering parameter (S_{21}) for the transmission at $f_{\text{in}}^{\text{opt}}$ from the pFSL's input port to the pFSL's output port, after linearizing the capacitance versus voltage characteristic of the diode around V_{dc}. The expression of $\text{IL}^{\text{s.s}}$ in dB is provided as follows:

$$\text{IL}^{s.s.} = -20\log_{10}(S_{21}) = -20\log_{10}\left|\frac{Z_{\text{in}}^{(\omega_{\text{in,opt}})}}{Z_{\text{in}}^{(\omega_{\text{in,opt}})} + \frac{Z_0}{2}}\right|. \quad (8)$$

In (8), $Z_{\text{in}}^{\omega_{\text{in,opt}}}$ is the impedance seen at $f_{\text{in}}^{\text{opt}}$ from the circuit node N_2 (see Fig. 1) toward N_1, and its value is almost independent of P_{in} for $P_{\text{in}} < P_{\text{th}}$. Upon validity of the same resonance conditions that minimize P_{th} and $Z_{\text{in}}^{(\omega_{\text{in,opt}})}$, it can be found that

$$Z_{\text{in}}^{(\omega_{\text{in,opt}})} = \frac{Z_{\text{tx}}^2}{R_s}. \quad (9)$$

Equation (9) allows to simplify $\text{IL}^{\text{s.s}}$ [see (8)] as follows:

$$\text{IL}^{s.s.} = -20\log_{10}\left|\frac{2Z_{\text{tx}}^2}{R_s Z_0 + 2Z_{\text{tx}}^2}\right|. \quad (10)$$

By replacing (6) in (10), $\text{IL}^{\text{s.s}}$ can be finally rewritten, as shown in the following equation:

$$\text{IL}^{s.s.} = -20\log_{10}\left|1 - \frac{Z_0}{Z_0 + 2C_v Q_v Z_{\text{tx}}^2 \omega_{\text{in,opt}}}\right|. \quad (11)$$

Equation (11) enables us to assess the minimum $\text{IL}^{\text{s.s}}$ value that can be attained by reflective pFSLs, given a selected $f_{\text{in}}^{\text{opt}}$ value and based on the dc-biased capacitance of the selected diode. As an example, a contour-plot capturing $\text{IL}^{\text{s.s}}$ versus Z_{tx} and C_v is displayed in Fig. 2(b), which was derived analytically while assuming the same δ, C_v, $f_{\text{in}}^{\text{opt}}$, and Z_0 values used during the derivation of Fig. 2(a). By comparing (11) with (7) and Fig. 2(a) with (b), an important design tradeoff between the desired P_{th} and $\text{IL}^{\text{s.s}}$ values can be identified. While relying on high-Z_{tx} values allows to reduce $\text{IL}^{\text{s.s}}$, it also determines an increase of P_{th} that can be unacceptable unless C_v values in the fF-range were used. Since any board-level pFSLs, such as the one that we designed and built in this work, can only leverage C_v values close to 1 pF or higher, there exists a fundamental limit for the minimum P_{th} that can be obtained while preserving a low $\text{IL}^{\text{s.s}}$. Furthermore, Z_{tx} cannot be made arbitrarily large without rendering $[Z_T]$ severely affected by electrical loading, thus also degrading $\text{IL}^{\text{s.s}}$. This inevitably restraints the pool of usable diodes as it limits the maximum acceptable R_s and, consequently, the minimum Q_v based on the maximum $\text{IL}^{\text{s.s}}$ that can be tolerated. Therefore, the strategic selection of the diode and the other components forming Z_a and Z_c is critical to make sure that the lowest $\text{IL}^{\text{s.s}}$ can be attained without requiring a large Z_{tx} that would compromise the achievable P_{th} value. Moreover, Fig. 2 provides useful means to assess the performance that would be achieved if pFSLs were designed and built directly on-chip through any available CMOS technologies. In such a scenario, due to the availability of both capacitors and diodes with capacitance in the fF-range, any integrated reflective

pFSLs would be able to simultaneously rely on extraordinarily low C_v and high Z_{tx} values (>1 kΩ), thus enabling much lower P_{th} values (<−20 dBm) than possible with board-level counterparts given a targeted $IL^{s.s}$ value.

A. Evaluation of the Maximum P_{in} Value for a Preserved Frequency Selectivity

While the achievement of low P_{th} and $IL^{s.s}$ values is certainly crucial, another metric to consider during the design of any pFSLs is the maximum P_{in} value ($P_{max} = (8Z_0\ V_{max})^{1/2}$, where V_{max} is the corresponding peak voltage at f_{in}^{opt}) at which a frequency-selective attenuation at f_{in}^{opt} is preserved. In particular, with regards to reflective pFSLs, the existence of a finite P_{max} is due to periodic transitions from reverse to forward conduction that any diodes undergo when the voltage across their terminals exceeds the sum of the diode's dc bias and built-in (V_{bi}) voltages. Due to these transitions, the diode's resistance (R_v) undergoes a sudden increase as P_{in} is made larger than P_{max}, leading to a progressive reduction of the parametrically generated negative resistance at f_d responsible for the rising of the subharmonic oscillation in the circuit and, consequently, to a degradation of the pFSL performance at f_{in}^{opt}. As a first-order of approximation, P_{max} can be found through a straightforward analysis of the circuit shown in Fig. 1 based on transmission matrices [see (12)] when assuming that Z_a, Z_b, and Z_c satisfy the resonant conditions minimizing P_{th} and when neglecting (for simplicity) any quadratic or cubic nonlinearities of the diode

$$P_{max} \approx \frac{(V_{dc} + V_{bi})^2 \left(2C_v Q_v \omega_{in,opt} Z_{tx}^2 + Z_0\right)^2}{8(Q_v)^2 Z_0 Z_{tx}^2}. \qquad (12)$$

Equation (12) aids the selection of the diode by identifying the minimum V_{dc}, allowing to preserve a frequency-selective limiting behavior for P_{in} values ranging from P_{th} to any desired P_{max} value, given any targeted C_v and Z_{tx} values. As an example, Fig. 3 shows a contour-plot capturing the analytically derived P_{max} versus Z_{tx} and V_{dc} [see (12)], assuming the same δ, f_{in}, and Z_0 values used during the derivation of Fig. 2, a V_{bi} arbitrary set to 0.7 V (i.e., the built-in voltage for silicon diodes), and a C_v value of 2.0 pF [i.e., the same used in our experimental demonstration when considering the additional parasitic capacitance (∼0.4 pF) associated with the diode's package]. As evident from both (12) and Fig. 3, P_{max} values lower than 0 dBm and fairly insensitive to Z_{tx} are obtained with low-capacitance diodes requiring the use of low V_{dc} values to operate. Nevertheless, significantly higher P_{max} values can still be achieved by selecting larger diodes biased with higher dc voltages. By comparing (12) with (7), it can be noticed that V_{dc} represents the most important design parameter to ensure that high P_{max} and low P_{th} values can be achieved simultaneously. Furthermore, contrary to any reported absorptive counterparts, reflective pFSLs are able to protect the integrity of any cascaded electronic components even for $P_{in} > P_{max}$. Yet, within such high-power operative scenario, reflective pFSLs progressively lose their frequency selectivity as P_{in} is increased, thus ultimately showing strong attenuations across significant portions of their original BW.

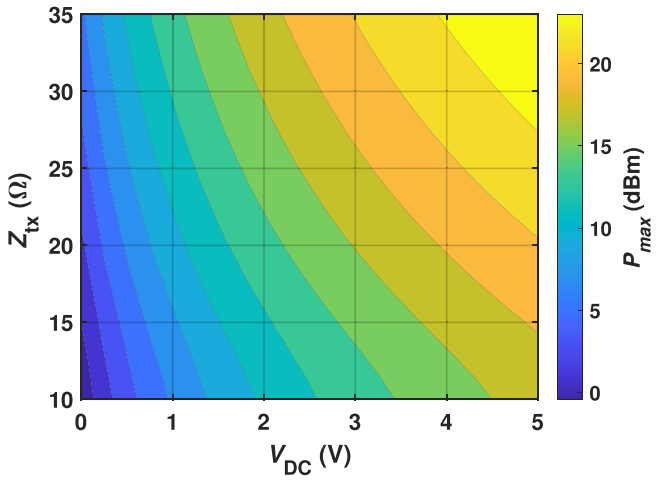

Fig. 3. P_{max} value (in dBm) versus Z_{tx} and V_{dc} for the reflective pFSL in Fig. 1, computed through (12) after assuming $Z_0 = 50\ \Omega$, $f_{in}^{opt} = 2.1$ GHz, $Q_v = 15$, $V_{bi} = 0.7$ V, $C_v = 2.0$ pF, and upon validity of the resonance conditions minimizing P_{th}.

III. Designing pFSLs in Commercial Circuit Simulators

In Section II, it has been shown how the achievement of the minimum P_{th} and $IL^{s.s}$ values in reflective pFSLs can be ensured for any input frequencies of interest by satisfying four resonant conditions and by minimizing $IL^{s.s}$ [see (11)]. Therefore, regardless of the nonlinear characteristics exhibited by pFSLs, the synthesis of the passive impedances [i.e., $[Z_T]$, Z_a, Z_b, and Z_c (see Fig. 1)] forming any board-level reflective pFSLs can be accomplished through linear simulation and optimization techniques, after selecting an available diode with the lowest possible C_v and the highest possible Q_v, given the minimum tolerated P_{max} value. It is worth pointing out that the capability to synthesize the different components of pFSLs through linear methods enables the reliance on conventional algorithms during the optimization of both the pFSLs' circuit and layout. Consequently, the optimal design conditions for any pFSLs, including those operating at high frequency and, consequently, more impacted by layout parasitics, can be identified more reliably and more easily than what is possible when only relying on perturbation-based techniques. Nevertheless, such techniques are still required to assess the behavior of pFSLs for $P_{in} > P_{th}$ and, thus, in the operative regime where the evolution of the circuit parameters strongly depends on the nonlinearities of the diode. Among the existing perturbation-based techniques, the power auxiliary generator (pAG) [28] technique provides unique means to extract the steady-state response of any parametric circuits without having to numerically enforce the validity of the nonperturbation condition [34] due to the adoption of an auxiliary generator in the circuit. A pAG consists of a continuous-wave (CW) voltage generator operating at f_d and delivering a small nonperturbative power through a generator impedance (Z_G). When a pAG is used to simulate the response of a pFSL through a commercial harmonic balance (HB) circuit simulator, the pFSL's output termination (i.e., Z_0 in

the circuit in Fig. 1) must be replaced by a pAG with Z_G also equal to Z_0. This allows us to insert f_d in the vector of frequencies that HB processors use to evaluate the response of driven RF circuits. In addition, by ensuring that Z_G matches Z_0, the adoption of the pAG does not cause variations of the impedance seen by the diode at f_d or at multiples of f_d, thus preventing any undesired changes in the dynamics of the circuit, which would lead to unreliable predictions of the circuit's response. The extraction of the steady-state response of pFSLs can be achieved by sweeping P_{in} from a much lower power than P_{th} up to the maximum power level of interest while configuring the values of the computed current and voltage phasors for any evaluated power level as initial conditions for the same circuit parameters prior the computation of the following data point to assess. Through this *ad hoc* sweeping strategy, it is possible to extract IS by evaluating the trend of the pFSLs' insertion loss for power levels exceeding P_{th}. This also provides the means to fine-tune some of the component values synthesized in the earlier design stage toward the achievement of the highest IS value. In order to do so, it is convenient to look at $Z_{\text{in}}^{\omega_{\text{in}}}$ (see Fig. 1) while varying some strategically selected circuit components to let the magnitude of this impedance be as small as possible for P_{in} exceeding P_{th}. During this design phase, the components synthesizing Z_b are the most adequate to be fine-tuned as they do not affect $\text{IL}^{\text{s.s}}$ while only slightly altering P_{th}. It is also important to point out that the ability to accurately predict IS in any pFSLs is heavily influenced by the reliability of the available nonlinear circuit model for the adopted diode.

IV. Experimental Results

In order to demonstrate the capability of reflective pFSLs to simultaneously exhibit low $\text{IL}^{\text{s.s}}$, low P_{th}, and high IS values, we designed an FR-4 PCB implementation of a ~2.1 GHz reflective pFSL (i.e., $f_{\text{in}}^{\text{opt}} \sim 2.1$ GHz) using a commercial off-the-shelf hyperabrupt varactor (Skyworks SMV1231) as a diode. The assembled pFSL relies on a hybrid implementation of the circuit topology shown in Fig. 1, including a set of lumped components strategically selected together with the optimal geometrical layout characteristics (i.e., the length and width of all interconnecting lines, the shape and foot-print of the selected surface-mount connectors, and the radius of each circular via). This allows to achieve a small form factor (2.2 cm^2 of board area) and the lowest possible P_{th} given an $\text{IL}^{\text{s.s}}$ lower than a maximum tolerated value (here set to 1 dB). In particular, Z_a and Z_b were synthesized through two LC parallel resonators with inductors L_a and L_b and capacitors C_a and C_b, whereas Z_c was synthesized through an inductor (L_c) in series with the selected varactor. Also, a dc-blocking capacitor ($C_{\text{blk}} = 12$ pF) was introduced in series with L_b to permit the dc-biasing of the selected diode through a bias-tee (Inmet 8800SMF3-06) at the input port, even allowing analog reconfigurability of P_{th} and $f_{\text{in}}^{\text{opt}}$, as will be discussed later. The transformation stage at $f_{\text{in}}^{\text{opt}}$ was designed to exhibit a Z_{tx} value close to 31 Ω when relying on two lumped capacitors (C_{tx} and C_{in}) and two distributed inductors made of short lines. Such a Z_{tx} value was chosen to ensure P_{th} and $\text{IL}^{\text{s.s}}$ values lower than −3 dBm and 1 dB, respectively (see Fig. 2) based on the C_v (2.0 pF) and Q_v (≈15) values exhibited by the varactor when V_{dc} is set to 1.1 V. Also, the adoption of distributed components in the transformation stage represents the most convenient design solution to ensure that the performance is not degraded by the capacitive coupling between the connectors' footprints and the rest of the circuit while preserving the lowest possible form factor. The designed pFSL is visualized in Fig. 4 together with a photograph of its built implementation, where the values and the model numbers of the selected lumped components are listed in the caption. After assembling the pFSL, we proceeded with its electrical characterization by extracting its S-parameters through the experimental setup described in Fig. 5. The measured electrical response of the reported pFSL was first characterized through the extraction of its S-parameters for driving power levels (e.g., −30 dBm) much lower than the expected limiting threshold and, thus, in the operative regime where a linear operation can be assumed. Fig. 6 shows the resulting measured and closely matching simulated plots of the pFSL's S_{21} and S_{11} versus f_{in}. Evidently, the reported pFSL exhibits a bandpass characteristic with a measured 3-dB fractional BW of 17%. Also, a minimum $\text{IL}^{\text{s.s}}$ of 0.94 dB was measured for a frequency (2.06 GHz) close to the targeted $f_{\text{in}}^{\text{opt}}$. Such a record-low $\text{IL}^{\text{s.s}}$ value closely matches both the corresponding circuit simulated one (0.9 dB) and our analytically derived expectation [0.6 dB; see Fig. 2(b)].

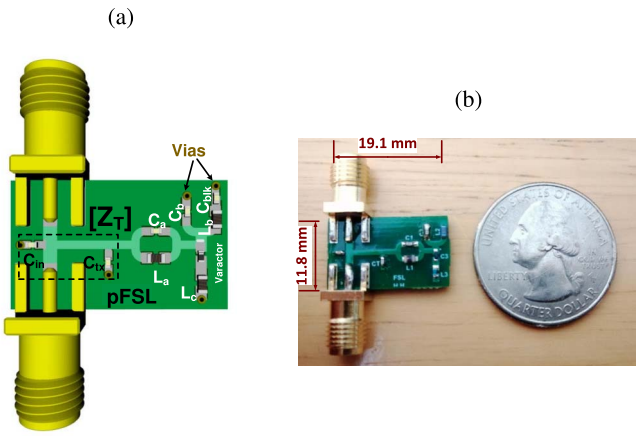

Fig. 4. (a) 3-D view of the designed pFSL showing $[Z_T]$ and the area dedicated to each adopted lumped component. (b) Top-view photograph of the built pFSL circuit. The model numbers for the adopted lumped components are: 1) 0402DC-11NXGRW for L_a; 2) 0603HP-6N8XGLU for L_b; 3) GJM1555C1H1R4WB01D for C_a; 4) GJM1555C1HR30WB01D for C_b; 5) 0402DC-1N0XJRW for L_c; 6) Skyworks SMV1231 for the diode; 7) GJM1555C1H1R5WB01D for C_{tx}; 8) GJM1555C1H1R0WB01D for C_{in}, and 9) GJM1555C1H120FB01 for C_{blk}.

Later, we characterized the pFSL response for P_{in} approaching and exceeding P_{th}. In order to most reliably extract P_{th}, we found the minimum P_{in} value around 2.1 GHz, triggering a 2:1 subharmonic oscillation in the circuit. In order to do so, we identified the power level at which a bifurcation triggering a 2:1 frequency division occurs from the measured output power (P_{sub}; see Fig. 7) at half of any explored driving frequencies. It is worth emphasizing that P_{sub} is not trivial

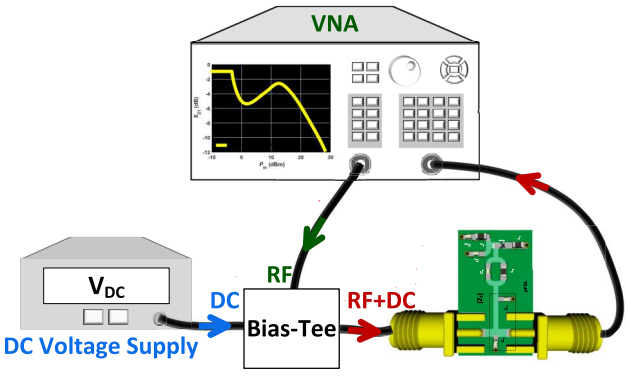

Fig. 5. Schematic of the experimental setup used for the extraction of the S-parameters of the fabricated pFSL. The circuit was connected to a network analyzer (Keysight N5221A) through an off-the-shelf bias-Tee (Inmet 8800SMF3-06).

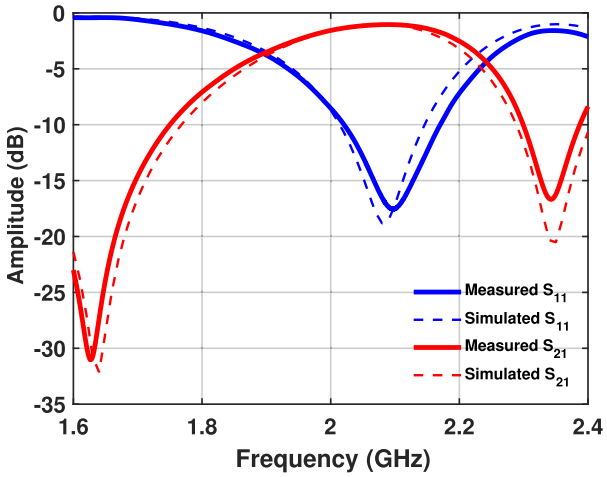

Fig. 6. Measured (continuous lines) and simulated (dotted lines) S_{11} and S_{21} of the reported pFSL for frequencies included within the pFSL's BW and when considering an input power level (−30 dBm) during the frequency sweep much lower than the expected P_{th}. The V_{dc} value (see Fig. 5) used during the extraction of these reported curves is 1.1 V.

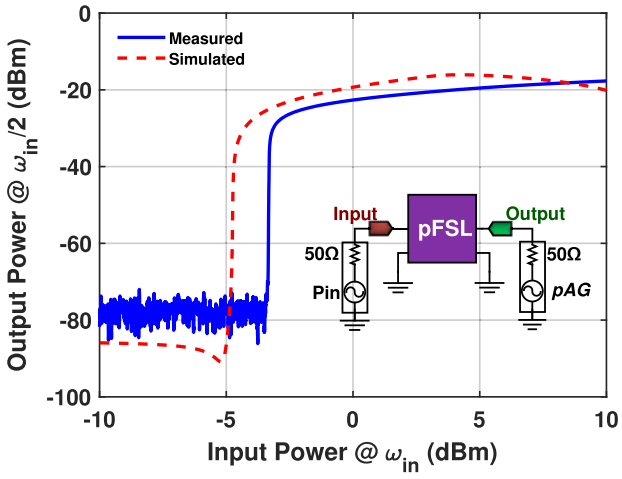

Fig. 7. Measured (in blue) and simulated (in red) trends of P_{sub} versus P_{in}. A simplified schematic is also shown in the inset, describing how we used a pAG erogating a nonperturbative power (−90 dBm) at 1.03 GHz in order to extract the simulated data. The V_{dc} value (see Fig. 5) used during the extraction of these reported curves is 1.1 V.

only for P_{in} exceeding P_{th}. As shown in Fig. 7, the measured pFSL exhibits a minimum P_{th} of −3.4 dBm at 2.06 GHz (i.e., the same frequency minimizing $IL^{s.s}$; see Fig. 6). Such a measured P_{th} value matches closely the predicted one found from the circuit simulated trend of P_{sub} versus P_{in} (see the dotted line in Fig. 7). This simulated trend was obtained by utilizing the pAG technique and the extracted EM model of the designed board, together with the S-parameters of the selected lumped components. The measured P_{th} is also close to its analytically predicted value [−4.8 dBm; see Fig. 2(a)], given the capacitance of the selected diode and the value chosen for Z_{tx}. The IS value of the built pFSL at 2.06 GHz was assessed as well. This was done by extracting the corresponding S_{21} for P_{in} values ranging from −10 to 28 dBm [the maximum available power level in our experiment; see Fig. 8(a)]. As evident, significant IS values up to 5.4 dB were found for $P_{in} > P_{th}$ and lower than 13 dBm. Within this power range, the designed pFSL shows a trend of the large-signal S_{21} versus f_{in} that realizes a frequency-selective notch centered around 2.06 GHz, clearly indicating the activation of a frequency-selective attenuation as P_{in} is increased above P_{th} [see the inset of Fig. 8(a)]. Furthermore, despite its less frequency-selective limiting behavior for $P_{in} > P_{max}$, the measured pFSL shows high IS values even for P_{in} higher than 13 dBm ($IS > 12.0$ dB for P_{in} approaching 28 dBm). It is worth emphasizing that the achievement of such high IS value is granted by a parametrically triggered nonlinear mechanism causing the RL at the two pFSL's ports to significantly increase as P_{in} is made larger than P_{th} [see Fig. 8(b)].

Nevertheless, both the measured S_{21} and S_{11} trends versus P_{in} (see Fig. 8) do not show a fully monotonic behavior, as also expected from the corresponding simulated trends (see the dotted lines in Fig. 8). This is due to changes in the diode's dynamics becoming more and more significant as the input power approaches P_{max}. In particular, through our circuit simulations, we found that the P_{in} value associated with the local maximum (minimum) of S_{21} (S_{11}) for $P_{in} > P_{th}$ corresponds to a peak voltage level across the adopted diode equal to $V_{bi} + V_{dc}$. This finding provided us with simple means to identify the P_{max} value [13 dBm, close to its estimated analytical value (14 dBm; see Fig. 3)] of the built pFSL by extracting the P_{in} level at which the same phenomenological change occurs in both the measured S_{21} and S_{11} trends. Finally, we evaluated the performance of the built pFSL when simultaneously driven by a 2.06-GHz signal and by a much lower power (−30 dBm) in-band tone. In order to do so, we relied on a conventional two-tone harmonic test where two RF signals, combined through an external power combiner (Mini-Circuits ZFRSC-42-S+), were simultaneously injected into the circuit from the pFSL's input port. In particular, the signal at 2.06 GHz, with power labeled as P_1, emulated the presence of a strong EMI at the pFSL's input port, whereas the second much lower power signal (with −30 dBm), detuned from

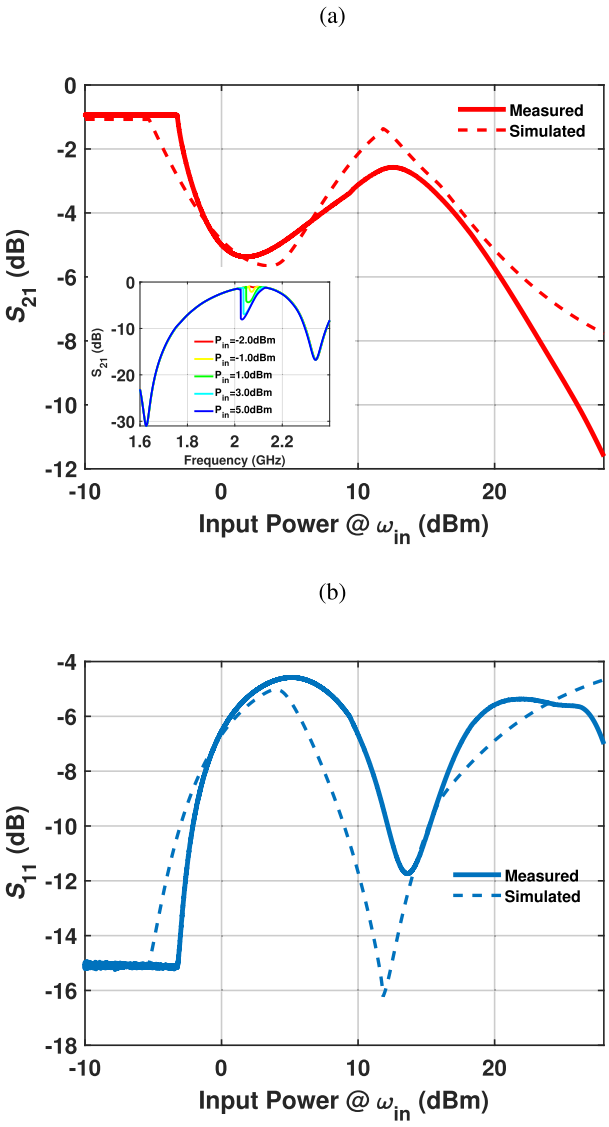

Fig. 8. Measured (continuous lines) and simulated (dotted lines) (a) S_{21} and (b) S_{11} at 2.06 GHz for P_{in} values ranging from -10 to 28 dBm. The measured trend of the S_{21} versus f_{in} for different input power levels used during the sweep, ranging from P_{th} to P_{max}, is also shown in the inset of (a) to highlight the frequency selectivity of the parametrically triggered limiting mechanism exploited by the reported pFSL for $P_{in} < P_{max}$. The V_{dc} value (see Fig. 5) used during the extraction of these reported curves is 1.1 V.

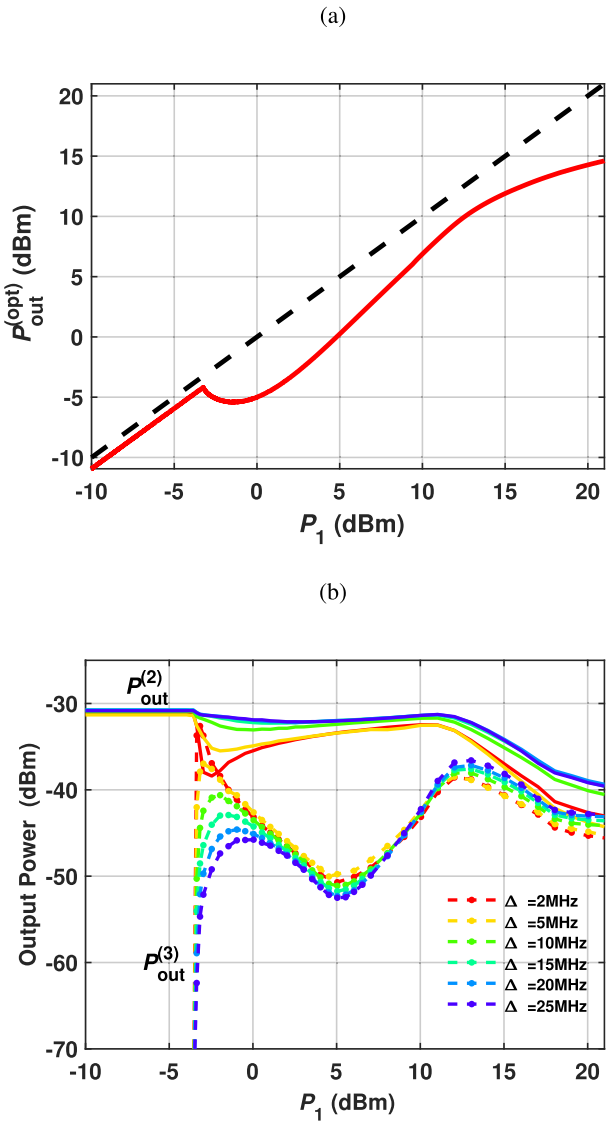

Fig. 9. (a) Comparison of the measured trend of P_{out}^{opt} versus P_1 (solid red line) with the corresponding trend expected from a linear and lossless two-port networks (black dashed line). (b) Measured trends of $P_{out}^{(2)}$ (solid lines) and $P_{out}^{(3)}$ (dashed lines) versus P_1 for Δ values ranging from 2 to 25 MHz. The V_{dc} value (see Fig. 5) used during the extraction of these reported curves is 1.1 V.

2.06 GHz by an amount labeled as Δ (i.e., $f_2 = 2.06$ GHz $+ \Delta$), was used to emulate the presence of a simultaneously received low-power signal carrying useful information. The output power levels at 2.06 GHz (P_{out}^{opt}) at f_2 ($P_{out}^{(2)}$) and the one ($P_{out}^{(3)}$) at the strongest 3rd-order intermodulation product ($f_3 = 4.12$ GHz-f_2) were measured for P_1 levels ranging from -10 to 21 dBm. It is crucial to emphasize that achieving low $P_{out}^{(3)}$ values is particularly important in applications where contiguous in-band channels with small frequency separations can be simultaneously received. The measured trends of P_{out}^{opt}, $P_{out}^{(2)}$ and $P_{out}^{(3)}$ versus P_1 are reported in Fig. 9(a) and (b) for Δ values varying between 2 and 25 MHz. It can be seen that the parametric mechanism responsible for the suppression of P_{out}^{opt} also causes an undesired attenuation (α) of $P_{out}^{(2)}$ that is higher for small values of Δ [see Fig 9(b)]. Yet, α values not exceeding 2 and 4 dB were attained for Δ values of 10 and 5 MHz, thus demonstrating a good frequency selectivity in the limiting operation generated by the circuit. Also, $P_{out}^{(3)}$ values below -40 dBm were measured for P_{in} values lower than P_{max} and for Δ higher than 10 MHz. It is key to point out that the ability to achieve such low $P_{out}^{(3)}$ values, regardless of the active parametrically triggered power limiting behavior, is due to the low impact exerted by the varactor's quadratic nonlinearities on the circuit dynamics for power levels that are lower than P_{max}. Nevertheless, for P_{in} larger than P_{max}, the compressing and nonfrequency-selective diode's electrical response determines a saturation in the power level at all frequencies in the circuit, causing the observed behavior for $P_1 > 13$ dBm. Ultimately, while the observation of P_{sub} has

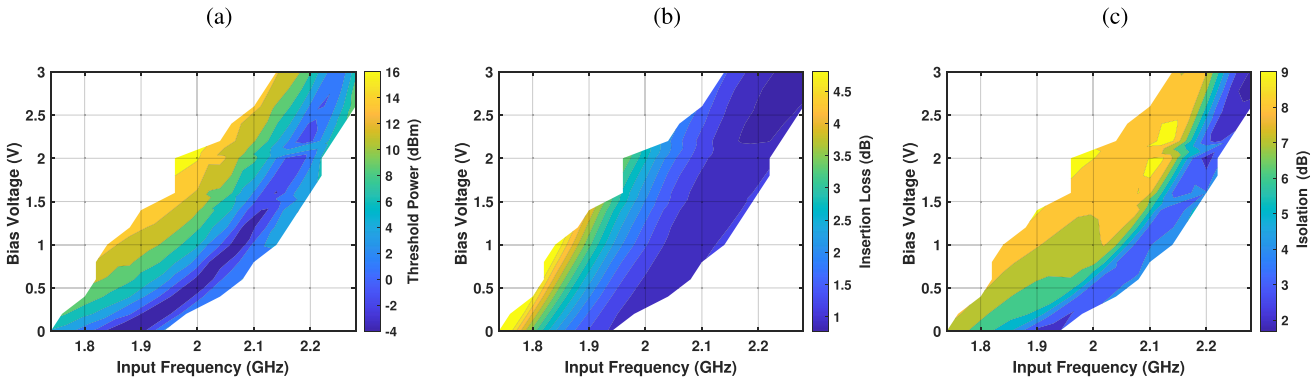

Fig. 10. Contour-plots capturing (a) measured P_{th}, (b) $\text{IL}^{\text{s.s}}$, and (c) $\text{IS}_{\text{max}}^{<P_{\text{max}}}$ values versus V_{dc} and f_{in}.

TABLE I
PERFORMANCE COMPARISON BETWEEN THE REPORTED pFSL AND OTHER PREVIOUSLY REPORTED DIODE-BASED PROTOTYPES

	Tech.	P_{th} (dBm)	$IL^{s.s.}$ (dB)	f_{in} (MHz)	$IS_{max}^{<P_{max}}$ (dB)	IS^{28dBm} (dB)	Component Area (cm^2)
[13]	Parametric	3	2	850	9	n/a	n/a
[16]	Parametric	10	1	2030	n/a	20	n/a
[15]	Parametric	3	2.5	2382	16	n/a	~9
[14]	BSF	3	2	2400	18	n/a	~37
[19]	BPF	24	2	1150	10	10	378
[18]	Coupler	6	1.5	2000	13	12	~3.5
This work	Parametric	-3.4	0.94	2060	5.4	12.0	2.2

provided us with reliable means to quantify P_{th}, the corresponding parametrically generated subharmonic signal, even if small, can also slightly degrade the signal-to-noise ratio (SNR) at the pFSL's output. Nevertheless, due to the large frequency separation between the pFSL's main operational frequency and its subharmonic one, a strong attenuation of P_{sub} can still be achieved through the adoption of a proper filtering stage at the pFSL output, without altering the circuit dynamics.

A. Threshold and Frequency Reconfigurability

After characterizing the operation of the built pFSL at the V_{dc} value (1.1 V) resulting in the lowest P_{th} around 2.1 GHz, we investigated the possibility to leverage different biasing conditions for the diode to reconfigure P_{th} and the frequency at which the highest IS value is desired. Yet, to ensure that the built pFSL can be practically used to suppress EMI with different frequencies or power levels from the originally targeted value, we measured P_{th}, $\text{IL}^{\text{s.s}}$, and the maximum IS for $P_{\text{in}} < P_{\text{max}}$ ($\text{IS}_{\text{max}}^{<P_{\text{max}}}$) for a broad range of V_{dc} and f_{in} values. This allowed us to construct three corresponding contour plots (see Fig. 10) capturing the value of each performance metric for the analyzed f_{in} and V_{dc} values. As evident, through the strategic adoption of V_{dc}, the measured pFSL can simultaneously achieve P_{th} and $\text{IL}^{\text{s.s}}$ values lower than 2 dBm and 2 dB, respectively, $\text{IS}_{\text{max}}^{<P_{\text{max}}}$ values up to 7 dB, and a tunable operational frequency ranging from 1.85 to 2.1 GHz. It is worth emphasizing that, due to the quadratic nonlinearities characterizing the response of the diode, especially under low V_{dc} values, any changes of the adopted dc bias to tune the frequency at which the maximum isolation can be attained will also result in variations of P_{max} and will influence the linearity of the circuit.

B. Comparison With the State of the Art

To benchmark the performance attained by our pFSL prototype with those attained by other passive diode-based FSLs, we compared (see Table I) P_{th}, $\text{IL}^{\text{s.s}}$, $f_{\text{in}}^{\text{opt}}$, and $\text{IS}_{\text{max}}^{<P_{\text{max}}}$ of our built pFSL when V_{dc} is chosen to minimize P_{th} with the corresponding values exhibited by the most recent demonstrated counterparts. Also, the IS value ($\text{IS}^{28\,\text{dBm}}$) of the reported pFSL for a much larger P_{in} value (28 dBm) than P_{th} was also compared to those of the other counterparts listed in Table I to assess the capability to protect any cascaded electronic components even from exceptionally strong EMI. As evident from Table I, the pFSL reported in this work exhibits the lowest P_{th} and $\text{IL}^{\text{s.s}}$ values among all the previously demonstrated diode-based passive FSLs even though it is operating at one of the highest frequencies. In particular, the P_{th} value attained by our reported pFSL is nearly five times lower than what was achieved by the previously reported SoA pFSL counterparts operating within the same frequency range. Nevertheless, when V_{dc} is selected to minimize P_{th}, $\text{IS}_{\text{max}}^{<P_{\text{max}}}$ is lower than what shown by the other previously reported diode-based FSLs. Yet, as shown in Fig. 10, $\text{IS}_{\text{max}}^{<P_{\text{max}}}$ can be increased up to 7 dB by relying on slightly different V_{dc} values, at the cost of higher P_{th} (still lower than 2 dBm) and $\text{IL}^{\text{s.s}}$ (still lower than 2 dB). Furthermore, it is important to point out that, different from other listed prototypes, the reported pFSL exhibits a large $\text{IS}^{28\,\text{dBm}}$ exceeding 12.0 dB, limiting the maximum output power delivered to any cascaded components to 13 dBm even in those scenarios when strong EMI with

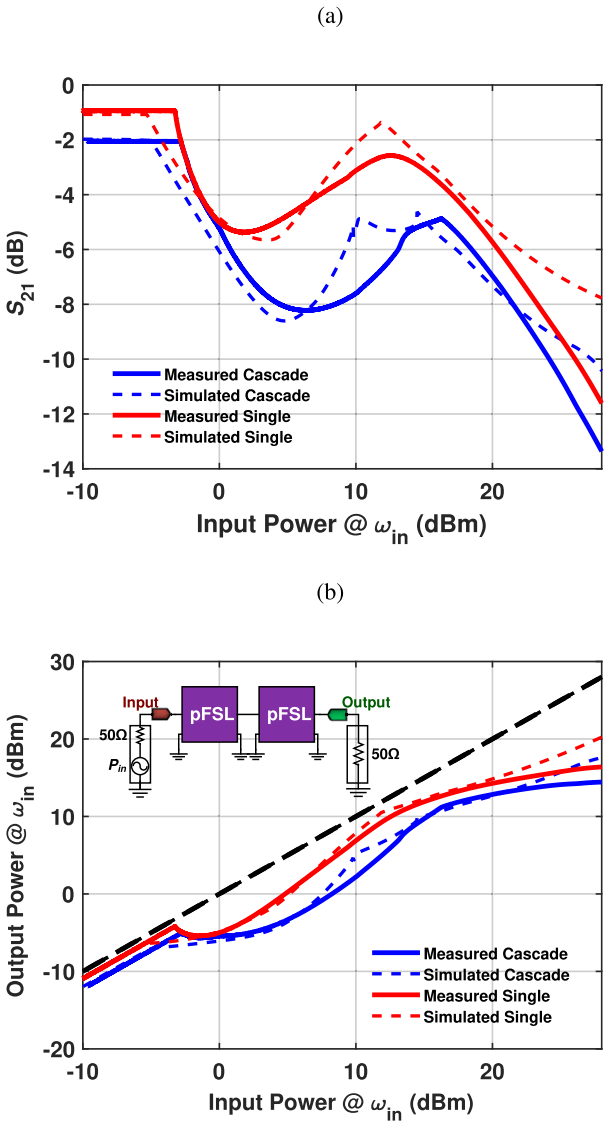

Fig. 11. Measured (continuous lines) and simulated (dotted lines) trends of (a) S_{21} and (b) output power for P_{in} values ranging from -10 to 28 dBm and when using only one pFSL (i.e., $M = 1$, in red) or two identical pFSLs (i.e., $M = 2$, in blue). A schematic representation of the connection between the pFSLs for $M = 2$ is shown in the inset. The V_{dc} value (see Fig. 5) used during the extraction of these reported curves is 1.1 V.

power approaching 30 dBm is received. Finally, by looking at the reported area of all the FSLs listed in Table I, it is easy to notice that our reported pFSL shows the highest degree of miniaturization.

In Section IV-C, an alternative approach not relying on changes of V_{dc} is introduced and experimentally validated to enhance both $IS_{max}^{<P_{max}}$ and $IS^{28\,dBm}$ without significantly degrading P_{th} and while preserving record-low $IL^{s.s}$ values (<2 dB).

C. Increasing IS Through Multiple pFSL Stages

Similar to what was previously shown for absorptive pFSLs [13], cascading multiple reflective pFSLs provides useful means to increase $IS_{max}^{<P_{max}}$, augmenting the maximum achievable suppression at f_{in}^{opt}. Nevertheless, this technique can be practically leveraged only when absorptive or reflective pFSLs with low $IL^{s.s}$ are available, such as the one that we designed and built in this work. In fact, since the insertion loss of a chain of pFSLs ($IL_{chain}^{s.s}$) grows proportionally with the number of cascaded stages (M), there exists an inevitable tradeoff between the maximum exploitable M and the highest tolerated $IL_{chain}^{s.s}$. Also, different from any chains of absorptive pFSLs whose design and operation inevitably lead to P_{th} values increasing proportionally to M, the high Z_{in} (see Fig. 1) value exhibited by reflective pFSLs for $P_{in} < P_{th}$ renders the voltage at f_{in}^{opt} across all the adopted diodes almost independent of M, especially when Z_{tx} is chosen to be much higher than R_s in order to minimize $IL^{s.s}$. This key operational feature allows to preserve low P_{th} values even when multiple reflective pFSL stages are used to enable higher $IS_{max}^{<P_{max}}$. Moreover, contrary to absorptive pFSLs, the adoption of multiple reflective pFSL stages permits to increase even the IS values attained for much higher P_{in} values than P_{max}.

In order to demonstrate the capability to achieve higher $IS_{max}^{<P_{max}}$ values through the adoption of multiple pFSL stages, we built a copy of the pFSL discussed in the previous section. The two pFSLs were then connected to each other, and the modified trends of the S_{21} versus P_{in} were extracted [see Fig. 11(a)], along with the corresponding trend of the output power versus P_{in} at 2.06 GHz (i.e., the f_{in} value giving the lowest threshold for a single-stage pFSL). As evident from Fig. 11, the chain formed by the two built pFSL stages allows to significantly enhance the maximum $IS_{max}^{<P_{max}}$ value attained by just one stage while causing negligible (<1 dB) increases of P_{th} and $IL^{s.s}$.

V. Conclusion

In this article, we discussed the design criteria and measured the performance of a ~2.1 GHz diode-based reflective pFSL built on an FR-4 PCB and using commercial off-the-shelf components. Due to its engineered dynamics, the reported pFSL prototype can exhibit record-low insertion loss for low-power signals ($IL^{s.s}$, as low as 0.94 dB), record-low-power threshold (P_{th}, as low as -3.4 dBm), and a significant suppression (up to 5.4 dB) for input power levels lower than the one forcing the diode to operate in its forward conduction. Furthermore, due to its unique design characteristics and regardless of the inevitable reduction in frequency selectivity, the built pFSL ensures good protection even from much stronger interference signals with power approaching 28 dBm. In addition, by strategically tuning the dc-biasing voltage of the diode, the reported pFSL allows to reconfigure the frequency at which the maximum IS is obtained by nearly 250 MHz (corresponding to a tuning range of ~0.12) while simultaneously preserving low P_{th} (<2 dBm) and $IL^{s.s}$ (<2 dB) values. Finally, by connecting two copies of the same pFSL designed and built in this work, we demonstrated that a significantly larger suppression value (>8 dB) for high-power signals can be attained while preserving low P_{th} (<−2.5 dBm) and low $IL^{s.s}$ (<2 dB).

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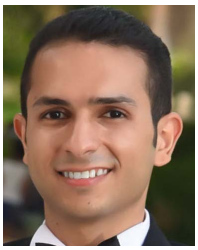

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