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Solution-Processed Organic and ZnO Field-Effect Transistors in Complementary Circuits

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Abstract: The use of high κ dielectrics lowers the operating voltage in organic field-effect transistors (FETs). Polymer ferroelectrics open the path not just for high κ values but allow processing of the dielectric films via electrical poling. Poled ferroelectric dielectrics in p-type organic FETs was seen to improve carrier mobility and reduce leakage current when compared to unpoled devices using the same dielectric. For n-type FETs, solution-processed ZnO films provide a viable low-cost option. UV–ozone-treated ZnO films was seen to improve the FET performance due to the filling of oxygen vacancies. P-type FETs were fabricated using the ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene) (PVDF-TrFE) as the dielectric along with a donor–acceptor polymer based on diketopyrrolopyrrole (DPP-DTT) as the semiconductor layer. The DPP-DTT FETs yield carrier mobilities upwards of 0.4 cm^2/Vs and high on/off ratios when the PVDF-TrFE layer is electrically poled. For n-type FETs, UV–ozone-treated sol–gel ZnO films on SiO_2 yield carrier mobilities of 10^{-2} cm^2/Vs. DPP-DTT-based p- and ZnO-based n-type FETs were used in a complementary voltage inverter circuit, showing promising characteristic gain. A basic inverter model was used to simulate the inverter characteristics, using parameters from the individual FET characteristics.

Keywords: field-effect transistor; conjugated polymer; ZnO; complementary circuit; ferroelectric polymer

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1. Introduction

The air-stability of n-type organic field-effect transistors (FETs) still remains a challenge. The intrinsic n-type behavior of ZnO provides an alternate path towards low-cost and air-stable FETs, and when integrated with p-type organic FETs, allows the realization of a basic digital circuit. As known from complementary metal oxide semiconductor (CMOS) technology, the fundamental element of a digital static circuit is a CMOS inverter, which connects an n-metal oxide semiconductor FET (MOSFET) and a p-MOSFET to achieve simple logic functions. The area of digital circuits based on solution-processed semiconducting films thus requires robust n- and p-type FETs. The non-toxicity and low-cost sol–gel processing conditions for depositing ZnO makes it attractive for the development of n-FETs. As such, several methods such as atomic layer deposition [1], pulsed laser deposition [2,3], spray pyrolysis [4], hydrothermal deposition [5], and chemical and other physical vapor deposition methods [6] have been used to deposit hierarchical architectures of ZnO in addition to sol–gel processes [7,8].

Naturally occurring oxygen vacancies in ZnO films may lead to trap sites that are detrimental to device performance. Several groups, including ours, have found that a UV–ozone treatment after film growth is an effective means of filling the vacancies [9–11]. This is seen to dramatically improve the performance of hybrid (with p-type organic semiconductors) photodiodes [12] and thin film transistors [13]. Electron energy loss spectroscopy suggests that oxygen vacancy sites are passivated within the bulk of the film to at least 90 nm upon UV–ozone treatment [12]. This is beneficial for bottom-gate ZnO FETs because film thicknesses are

typically less than 90 nm, ensuring that trap sites due to oxygen vacancies at the ZnO–dielectric interface are minimized.

In the area of p-type solution processable FETs, diketopyrrolopyrrole (DPP)-based copolymers have proven to be air-stable, robust, and demonstrate high carrier mobilities [14–16]. The tuning of the donor–acceptor (D–A) moieties in DPP copolymers not only lowers the band-gap energies but renders them chemically stable. The enhanced intermolecular interactions between the D–A units result in molecular packing with increased electronic bandwidths, which is favorable for charge transport [17]. A DPP copolymer, with the donor moiety of dithienylthieno[3,2-b]thiophene (DTT) and an acceptor moiety of n-alkyl (DPP-DTT), has shown p-type carrier mobilities >5 cm^2/Vs in FET architectures with modified SiO_2 dielectrics [18], and upon modifying the copolymer in a polystyrene matrix using self-assembly phenomena [19].

DPP copolymers with SiO_2 and divinyltetramethylsiloxane bisbenzocyclobutene (BCB) dielectrics in bottom-gate FET configurations [16,18] or low κ dielectrics, such as CYTOP in top-gate FET architectures [20], show relatively high operating voltages. Organic FETs mainly operate in the accumulation region; therefore, a practical approach towards lowering the operating voltage is to increase the capacitance of the dielectric, which may be achieved by using a high κ dielectric and/or decreasing the thickness of the dielectric film. Decreasing the thickness of the dielectric layer below a critical value is usually problematic with polymer dielectrics due to pin-hole effects.

Polymeric high κ ferroelectric dielectrics such as copolymers of polyvinylidene fluoride (PVDF) with trifluoroethylene (PVDF-TrFE) are advantageous in lowering the operating voltage as well as enhancing the performance of organic FETs [21–24]. Such ferroelectric dielectrics are particularly attractive for non-volatile memory applications and in sensing [25,26]. However, PVDF-based dielectrics could have a detrimental impact on the carrier mobilities in FETs. This is mainly due to a polarization fluctuation-driven transport and dynamic coupling of the charge carriers to the electronic polarization at the semiconductor–dielectric interface [27,28]. Such an interaction results in an increase in the effective mass of the carriers, and thus a decrease in carrier mobilities [29]. In a prior work, we have shown that electrical poling of the PVDF-TrFE layer is an effective means of enhancing carrier mobilities and other transport properties in FETs [24]. These poling methods can be divided into three categories: vertical poling, lateral poling, and texture-poling. In vertical poling, an electric field is applied perpendicular to the surface of the PVDF-TrFE layer, resulting in the alignment of the dipoles throughout the depth of the layer. The field is oriented in such a way that operation of the FET will not act to reorient the dipoles. In lateral poling, an electric field is applied parallel to the surface of the PVDF-TrFE layer. This poling acts on the top surface of the layer, which in the bottom-gate top-contact FET architecture used is the surface which is in contact with the semiconducting layer. Texture-poling makes use of both types of poling to further enhance the transport properties of our FETs. Vertical poling of the PVDF-TrFE layer or texture-poling, involving a judicious combination of lateral poling approximately the bottom one-third of the dielectric closer to the gate along with vertical poling, were seen to significantly improve the properties of 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) FETs. Lateral poling, on the other hand, was seen to be detrimental in the prior work, resulting in a positive shift of the threshold voltage and a reduction in the on/off ratio of the devices. These poling methods are reversible, and thus introduce a tunable parameter for FET performance.

Here, we extend the work of electrical poling of the PVDF-TrFE layer to DPP-DTT copolymer-based FETs. These p-type bottom-gate, top-contact FETs operate well below the 60 V range seen with SiO_2 and other dielectrics. The texture-poled DPP-DTT FETs show an order of magnitude higher carrier mobilities compared to vertically poled (V-poled) devices. For n-type FETs, sol–gel-processed UV–ozone-treated ZnO is used as the semiconductor. Due to the elevated temperature annealing of sol–gel ZnO films, we used SiO_2 as the gate dielectric in bottom-gate architectures. The DPP-DTT and ZnO FETs were used in a voltage inverter circuit, showing a maximum gain of 28.

Using the parameters obtained from the experimental transfer characteristics of FETs, we fitted the output characteristics using a script written in an open-source program (Python). The fitting parameters obtained from the individual p- and n-type FETs were then used to model a voltage inverter using an analytical model. We further discuss strategies for improving the performance of ZnO FETs and subsequent inverter operations.

2. Materials and Methods

2.1. Fabrication and Characterization of FET Devices

Heavily doped silicon wafers with a 200 nm oxide layer were obtained from Silicon Quest International Inc. (Santa Clara, CA, USA). Glass microscope slides were obtained from Fisher Scientific (Waltham, MA, USA). The dielectric copolymer poly(vinylidene fluoride trifluoroethylene) (PVDF-TrFE) (75:25) was procured from Measurement Specialties Inc. (Hampton, VA, USA). Zinc acetate dihydrate ($C_4H_6O_4Zn$ $2H_2O$, ACS Reagent $\geq$98%) and solvents: ethanolamine (C_2H_7NO, ACS Reagent $\geq$ 99.0%), 2-methyoxyethanol ($C_3H_8O_2$, anhydrous 99.8%), N-N Dimethyformamide (DMF), chloroform (HPLC grade) and 1,2-Dichlorobenzene (anhydrous 98%) were obtained from Sigma Aldrich (St. Louis, MO, USA). The DPP-DTT copolymer was procured through 1-Material Inc. (Dorval, Quebec, Cananda). The aluminum wire (Ag wire, 99.99% pure) and gold wire (Au wire, 99.99% pure) used for thermal evaporation of the electrodes were obtained from Kurt J. Lesker Inc. (Jefferson Hills, PA, USA).

For the n-type FET, silicon wafers were cut into 1 $\times$ 1 inch squares using a diamond-tipped pen. The substrates were cleaned using an organic cleaning method of rinsing with acetone, followed by 10 min sonication in an acetone bath, then rinsed with isopropanol, followed by 10 min sonication in an isopropanol bath, then finally rinsed with DI water and dried. Substrates were then baked in a 100 °C oven for 10 min to remove any residual moisture.

The ZnO precursor solution was made by combining 270 µL of ethanolamine with 10 mL of 2-methoxyethanol and then adding 1 g of zinc acetate dihydrate. A magnetic stirrer was added to the solution vial, and the solution was allowed to stir for >12 h at room temperature.

The solution was then filtered with a 0.22 µm PTFE filter. Then, 0.5 mL of ZnO solution was dropped and spincoated onto SiO_2/Si++ under ambient conditions at 2000 rpm for 60 s. The ZnO films were annealed in an oven set to 100 °C for 10 min and then placed into the chamber of a plasma cleaner (Harrick Plasma PDC-32G, Ithaca, NY, USA). A UV–ozone treatment was performed on the ZnO film at an O_2 pressure of 300 mTorr for 60 s. The duration was selected to ensure the filling of oxygen vacancies throughout the bulk of the ZnO film, without exposing it long enough to introduce interstitial oxygen [13]. Following this treatment, the film was further annealed for 50 min on a hotplate set to 275 °C followed by annealing in an oven at 220 °C for 24 h. Aluminum contacts (source/drain) of ~60 nm were thermally evaporated onto the ZnO film, which were patterned with a mask for a channel length of 1000 µm and a channel width of 50 µm.

For the p-type FET, glass microscope slides (1 mm thickness) were cut into 1 $\times$ 1 inch substrates using a diamond-tipped pen. These substrates were organically cleaned, and 60 nm Al gate electrodes were thermally evaporated onto the surface of the glass.

PVDF-TrFE was combined with DMF which was allowed to stir at room temperature overnight (>12 h). For comparing the effects of poling, the film was formed using solution with a 100 mg/mL concentration. Later, for devices used in the inverter circuit, the solution was made with a 50 mg/mL concentration to make the film thinner. Reducing the thickness of the dielectric layer enhances its capacitance and charge accumulation in the FET channel. Under nitrogen atmosphere, the solution was dropped onto the substrate and then spun at 1600 rpm for 60 s. The substrate was then annealed in a nitrogen atmosphere at 70 °C for 10 min. The PVDF-TrFE film was then removed from the glovebox for poling.

Electrical poling in the vertical direction of the ferroelectric PVDF-TrFE film was performed on a hotplate using the bottom aluminum gate and an external aluminum electrode (evaporated onto a separate glass slide) to apply a field on the order of magnitude

of 100 MV/m vertically across the thin film, as shown in Figure 1a. The film was poled at 135 °C for 30 min and at room temperature for 30 min. The temperature for annealing the film was chosen because it is just above the ferroelectric–paraelectric transition temperature of PVDF-TrFE [24]. The field was such that a negative bias was applied to the evaporated bottom-gate to ensure that the gate voltage during FET operation would not act to reorient the dipoles.

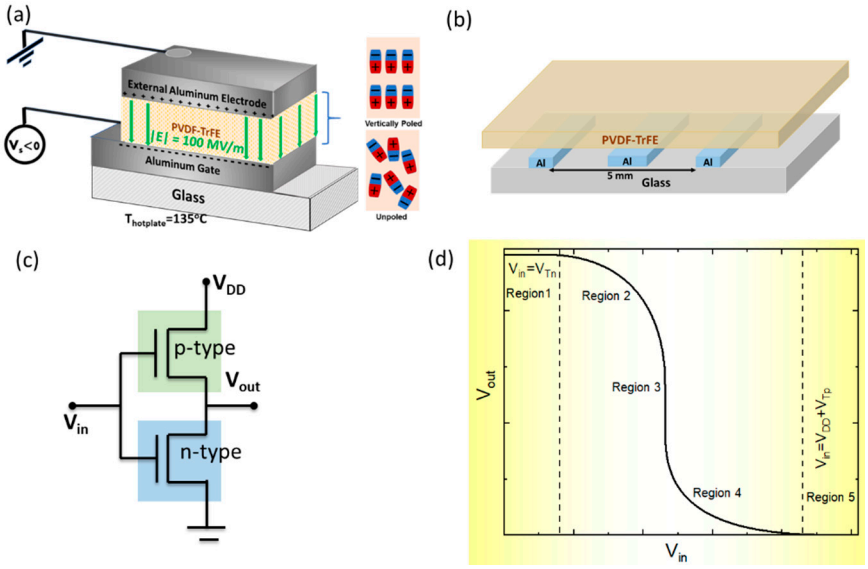

Figure 1. (**a**) Schematic of vertical poling the PVDF-TrFE layer where the dipoles are oriented in a vertical direction. (**b**) Layout of the electrodes below the PVDF-TrFE layer for texture-poling condition. (**c**) Schematic of a voltage inverter comprising a p-field-effect transistor (FET) and an n-FET. (**d**) The five different regions of operation of an inverter circuit. These regions are discussed in the text.

Prior work shows that an application of a lateral electric field parallel to the bottom of the PVDF-TrFE layer after vertical poling reduces the gate leakage current [24]. This texture-poling condition in another sample was achieved by evaporating aluminum electrodes which flank the central gate electrode on either side, as shown in Figure 1b. Following the vertical poling process of PVDF-TrFE, a lateral electric field was applied between these two electrodes while the sample rested on a hotplate at 135 °C. The magnitude of this electric field is small (10^4 V/m) to ensure that the lateral field only acts to reorient the dipoles in the region of the PVDF-TrFE film close to the bottom electrodes. The field only acts to reorient the dipoles close to the gate electrode, the direction of lateral poling does not influence device performance.

DPP-DTT precursor solution was made by dissolving the polymer in equal parts chloroform and 1,2 dichlorobenzene (5.1 mg/mL concentration). A magnetic stirrer was added, and the solution was allowed to stir at room temperature overnight. Then, 75 µL was dynamically spincast onto the PVDF-TrFE layer at 900 rpm for 60 s under a nitrogen atmosphere. The DPP-DTT film was restricted to a small channel during spincasting by applying Teflon tape. After removing the Teflon tape, the film was annealed at 100 °C for an hour and a half under nitrogen atmosphere. Gold electrodes of 50 nm were thermally evaporated onto the substrates which were patterned with a mask for a channel length of 1000 µm and a channel width of 50 µm.

Both n-type ZnO and p-type DPP-DTT devices were fabricated to utilize a bottom-gate, top-contact architecture. The transfer and output characteristics of these devices were measured utilizing a combination of Keithley 2400 and Keithley 236 sourcemeters, each controlled by LabView programs. From the transfer characteristics, we extracted the

mobilities, threshold voltages, and on/off ratios of our devices, with the devices operating in the saturation regime.

2.2. FET and Inverter Model

A complementary n–p inverter circuit was constructed using the ZnO and DPP-DTT FETs. Wires were soldered onto the contacts of the p-type FET, while for the n-type FET, due to the geometry of the contacts, it was easier to attach the probes directly. The basic configuration is shown schematically in Figure 1c. Here, the drain contact of the p-type FET (also known as the "pull-up" transistor in this circuit) is connected to the drain of the n-type FET (the "pull-down" transistor). The gates of both devices are connected together to serve as the input node (V_{in}) of the circuit, and the connection between the drain contacts of the FETs act as the output node (V_{out}) of the circuit. The source of the pull-up transistor is connected to the power supply (V_{DD}), and the source of the pull-down transistor is connected to the ground. From the channel connected to the p- and n-type FETs, the output voltage (V_{out}) could be extracted as V_{in} was swept with a constant V_{DD} applied. Connections between the two FETs as well as between the FETs and the instrumentation was external. The instruments used for the DC inverter characteristics were two Keithley 2400 sourcemeters (providing V_{in} and V_{DD}) as well as the Keithley 236 sourcemeter (which acted as common ground and to measure V_{out}).

Much of the organic FET simulations thus far were conducted in SPICE (Simulation Program with Integrated Circuit Emphasis) using the MOSFET model, and other commercial circuit simulation software. Several of the transistor properties such as carrier mobility (μ), subthreshold swing (SS), and threshold voltage (V_T) may be obtained from the saturation region of the transfer characteristics. In the saturation region:

$$\mu = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \tag{1}$$

where C_i is the dielectric capacitance, W is the channel width, L is the channel length, V_{GS} is the gate-source voltage, I_{DS} is the drain current, and V_{GS} is the drain-source voltage.

As an alternative to SPICE, open-source Python programming allows easy access to coding FET and other circuit characteristics. We evaluated the output curves using two methods. Method 1 used the basic transistor equations [30,31], where the drain-source current in the linear regime ($|V_{DS}| \leq |V_{GS}-V_T|$) is given by:

$$I_{DS} = -\frac{W}{L}\mu C_i\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \tag{2}$$

In the saturation region ($|V_{DS}| \geq |V_{GS}-V_T|$), the drain-source current can be expressed by:

$$I_{DS} = -\frac{W}{2L}\mu C_i(V_{GS} - V_T)^2(1-\lambda(V_{DS}-(V_{GS}-V_T))) \tag{3}$$

where the parameter λ denotes the variation of the conductance with V_{DS} in the saturation region.

We denote Method 2 as the unified model and parameter extraction method by Estrada et al. [32], where the drain currents in the linear and saturation regions are modelled together and given by:

$$I_{DS} = \frac{W}{L}C_i\frac{\mu(V_{GS}-V_T)}{\left(1+R\frac{W}{L}C_i\mu(V_{GS}-V_T)\right)} \times \frac{V_{DS}(1+\lambda V_{DS})}{\left[1+\left[\frac{V_{DS}}{V_{DSsat}}\right]^m\right]^{1/m}} + I_0 \tag{4}$$

In Equation (4), the saturation voltage (V_{DSsat}) is defined by using a modulation parameter, α, $V_{DSsat} = \alpha(V_{GS}-V_T)$; R is the source and drain resistance, I_0 is the leakage current, and m is another fitting parameter which takes into account the sharpness of the knee region. Here, we ignore the gate-field dependence of μ.

There are several reports of organic voltage inverters utilizing all organic p- and n-FETs [33–38] as well as organic p-FETs and ZnO n-FETs [1,4,39–42]. The basic configuration, schematically shown in Figure 1c, comprises the source of the n-FET to be at ground, while the source of the p-FET to be at the voltage, V_{DD}. As the input (gates) are swept, the inverter switches between stable states in which only one device is operating, allowing for the steady states to act as logic "1" and "0". The complementary nature of the two transistors allows only one of them to be conducted in a stable state. Power dissipation is only present while the inverter is switching between states. The sharpness of this transition determines how well the circuit can act as a logic device.

An analytical model has been used by Bode et al. [36] for the five different regimes of operation of the FETs to predict the inverter output characteristics. Figure 1d schematically shows the different regions of the direct current (DC) output characteristics of an inverter circuit with a p-FET (green) and an n-FET (blue) (Figure 1c). For low values of V_{in}, as long as it is lower than the threshold of the n-FET (V_{Tn}), V_{out} is a maximum and is equal to V_{DD}. In this region, the p-FET is operational, and the n-FET is off. Similarly, when the input voltage is high ($>V_{DD} + V_{Tp}$), where V_{Tp} is the threshold voltage of p-FET, the n-FET is operational, and the p-FET is off. Ideally, because only one of the FETs is on in the steady state, there is no static current or power dissipation.

Regions 2–4 may be modelled using an analytical model which relies on the current through the p-FET and n-FET being equal and opposite ($I_{DSn} = -I_{DSp}$). This condition results in a cubic polynomial in regions 2 and 4 [36]. In region 3, because we will be using the criterion that $V_{Tn} > V_{Tp}$, both FETs are in saturation. Here, we simply outline the method in two regions. In region 2, when $V_{in} > V_{Tn}$, and while the n-FET is in saturation and the p-FET is in the linear region, and in region 4, while the p-FET is in saturation and the n-FET is in the linear region, the output voltage has the form:

$$V_{out} = \delta_{2,i} V_{DD} + \sqrt{\frac{-p_i}{3}} \cos(\Theta_i) - \frac{a_i}{3} \tag{5}$$

where

$$\Theta_i = \frac{\arctan\left(\frac{2}{-q_i}\sqrt{-\frac{q_i^2}{4} - \frac{p_i^3}{27}}\right) + n_i \pi}{3} \tag{6}$$

$$p_i = b_i - \frac{a_i^3}{3} \tag{7}$$

$$q_i = c_i + \frac{2a_i^3 - 9a_i b_i}{27} \tag{8}$$

In the above equations, i represents regions 2 or 4 and n_i is a phase factor which is critical to the form of the cubic polynomial. The parameters: a_i, b_i, and c_i vary for the two regions and can be expressed in terms of V_{in}, V_{DD}, and other FET parameters. Along with W, L, carrier mobility, and threshold voltage, the parameter λ, which is found from Equation (3) or (4), is also required to obtain the a, b, and c parameters [36].

3. Results

3.1. P-Type FETs

Figure 2a shows the transfer characteristics from two DPP-DTT/PVDF-TrFE FETs. In one case, the PVDF-TrFE film was V-poled, and in the other case, the dielectric layer was texture-poled, as discussed in Section 2.1. An order of magnitude higher carrier mobility, which was extracted in the saturation region, is seen for the texture-poled device compared to the V-poled device. A similar behavior was observed with TIPS-pentacene on PVDF-TrFE FETs [24], where the texture-poled FETs showed $\mu > 1$ cm^2/Vs without changing the processing condition for TIPS-pentacene; the V-poled TIPS-pentacene FETs show almost an order of magnitude smaller carrier mobilities. Approximately the bottom one-third of the PVDF-TrFE layer had a lateral orientation of the dipole moment in texture-poled

devices; therefore, the gate leakage current and its dependence on the voltage was further reduced [24]. We note that in both V-poled and texture-poled dielectrics, the dipoles were oriented in a similar fashion at the interface of the semiconductor and the dielectric (Figure 1a). These FETs performed much better than unpoled or lateral poled (from the top) FETs, as was also shown using other semiconductors [21]. Lateral poling from the top had the disadvantage that there may be a substantial S-D current even in the absence of any gate voltage due to the presence of a spontaneous parallel polarization field. A slightly high off-current for the textured-poled FET in Figure 2a may have arisen from a penetration of lateral electric field near the semiconductor–dielectric interface.

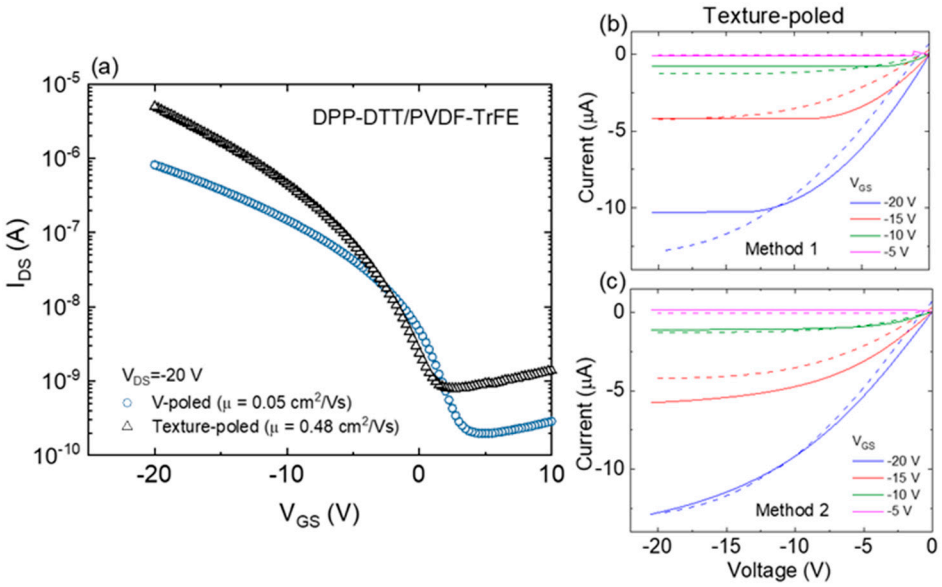

Figure 2. (**a**) Transfer characteristics from two DPP-DTT/PVDF-TrFE FETs, one where the PVDF-TrFE layer was V-poled, and in the other, texture-poled. (**b**,**c**) The output characteristics of the texture-poled DPP-DTT FET. The dotted lines show the experimental data. The bold lines are from the FET models, denoted as Methods 1 and 2, respectively, and discussed in the text.

The threshold voltages for the V-poled and texture-poled DPP-DTT FETs were calculated from the transfer characteristics fitted to be −2.5 V and −6.2 V, respectively. Although the carrier mobility is higher for the texture-poled FET, the off-current is seen to be higher compared to the V-poled device. This could be an issue with texture-poled devices, especially if the lateral poling from the bottom (see Figure 1b for the setup) is too high. If the lateral field during poling penetrates deep into the PVDF-TrFE layer from the bottom, there is the possibility that close to the semiconductor interface, the PVDF-TrFE domains are aligned in the lateral direction, resulting in a spontaneous parallel field, and thus an enhancement of the off-current. For practical considerations, as explained in Section 3.3., the inverter circuits were fabricated with p-type DPP-DTT FETs where the PVDF-TrFE layer was V-poled.

For modelling the inverter circuit, parameters from individual FETs are required. Figure 2b,c show an example. The experimental output characteristics, plotted by the dotted lines, are the same in both, and are from the texture-poled DPP-DTT FET. Equations (2) and (3), which we identified as Method 1, were used to model the output characteristics in Figure 2b, shown by the bold lines. Similarly, Method 2 (using Equation (4)) was used to model the same set of output characteristics, shown in Figure 2c by the bold lines. Apart from some deviations with the experimental data, Method 2 performed better. Both methods, however, yielded similar values of $\lambda = 0.005\ V^{-1}$, which is required as an input parameter for the inverter circuit. The same methods were applied to both FETs discussed in Section 3.3. that were used in the inverter and its modeling.

3.2. N-Type FETs

The solution processability of ZnO allows for flexible and transparent consumer electronics. Solution-processed ZnO films show high n-type carrier mobilities in FET architectures; annealing temperatures of 500 °C have resulted in μ values being as high as 6 cm^2/Vs [43]. These ZnO films are utilized in hydration chemistry for designing benign but highly reactive aqueous precursors. Hydrothermal growth of ZnO film on polymer dielectrics have also shown high FET mobility [44]. The sol–gel films used in this work and other reports use a simpler route of spincoating an organometallic diethylzinc precursor solution and annealing the films in air at relatively low temperatures [45]. Furthermore, by controlling the humidity condition, while annealing ZnO films, one can adjust the intrinsic doping levels, carrier concentration, and thus improve FET performance [46]. There are further reports of using indium ZnO for enhanced FET performance with on/off ratios over 10^7 [47].

ZnO is known to have defects such as oxygen vacancies (V_O), Zn vacancies, and Zn and oxygen interstitial defect sites [48]. V_O can result in charge-trapping mechanisms and thus degrade the performance of FETs. UV light soaking [9] and UV–ozone treatment [10–12] have been shown to reduce oxygen vacancies.

Figure 3a represents the impact of UV–ozone treatment on the structure of ZnO, where oxygen vacancies are filled due to the reaction. In this treatment, UV light of 185 nm first dissociates molecular oxygen (O_2) into atomic triplet oxygen. This triplet oxygen then combines with molecular oxygen to form ozone. A second UV source of 254 nm then dissociates the ozone to form atomic singlet oxygen, which is more reactive and referred to as radical oxygen. This oxygen is then free to react with the ZnO film surface and fill V_O. It should be pointed out that extended exposure may result in interstitial oxygen. ZnO FETs were fabricated using SiO_2 as the dielectric layer. The output characteristics of two such ZnO FETs, where the ZnO film was either left untreated or having undergone a UV–ozone treatment (as discussed in Section 2.1.), are shown in Figure 3b,c. In the untreated film, when the device enters the saturation region, there is a rapid loss in current. This is attributed to the trapping of charge carriers by V_O within the conducting channel. With UV–ozone-treated films, a clear saturation region is observed in the output characteristics. For non-treated ZnO FETs, the median mobility across several devices is 2.5×10^{-5} cm^2/Vs. Some of the high-performing UV–ozone-treated FETs yield mobilities in the 10^{-2} cm^2/Vs range, which were used in the inverter circuit.

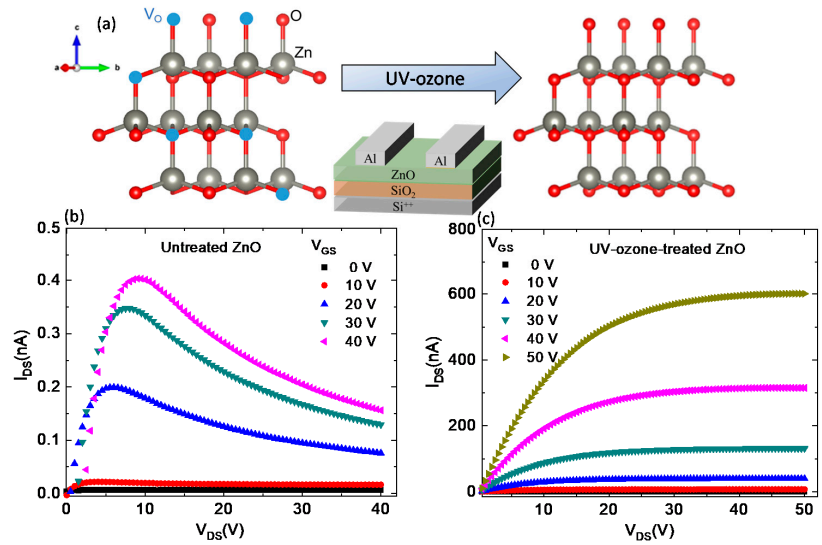

Figure 3. (**a**) A schematic representation of the ZnO structure where the oxygen vacancies (blue circles) are filled upon UV–ozone-treatment. The inset shows the FET architecture. (**b**) Output characteristics of an untreated ZnO FET. (**c**) Output characteristics of a UV–ozone-treated ZnO film.

It has been further observed that a large positive threshold voltage as well as a hysteresis in the transfer characteristics are linked to a high density of interfacial trap states due to V_O. Compared to the untreated ZnO FETs, the UV–ozone-treated FETs show hardly any hysteresis in the transfer characteristics [13].

3.3. Inverter Characteristics

As a proof of concept, sol–gel ZnO FETs were used in an inverter circuit. This was achieved by connecting a DPP-DTT p-FET with a UV–ozone-treated ZnO FET. V-poled DPP-DTT/PVDF-TrFE was used for two reasons: firstly, the p-FET mobility is comparable to ZnO FETs; and secondly, for future integrated circuits, where we plan on integrating the p-FET vertically on top of the ZnO FET, the texture-poling architecture will not be possible and only the V-poling architecture is feasible. The inverter circuit further allowed us to model the DC output characteristics using the analytical model, briefly discussed in Section 2.2. The program was written in open-source Python, eliminating the need for any commercial device simulation software.

Figure 4a,b show the transfer characteristics of the individual DPP-DTT/PVDF-TrFE and ZnO FETs. The PVDF-TrFE was V-poled, and the carrier mobility was higher than the other V-poled FET shown in Figure 2a due to the difference in thickness of the dielectric layer. Another thing to note here is that V_T of the ZnO FET was higher than that of the p-FET, because a low κ (SiO_2) dielectric was used. The inverter output characteristics are shown in Figure 4c at V_{DD} of 20 V and 25 V. A maximum voltage gain ($-dV_{out}/dV_{in}$) of 28 was observed when V_{DD} was held at 25 V. Differential gains of ~20 have been observed in other inverter circuits fabricated with ZnO and p-type FETs [4]. Indium gallium ZnO FETs with p-type polymer FETs have displayed differential gains as high as 40 [49].

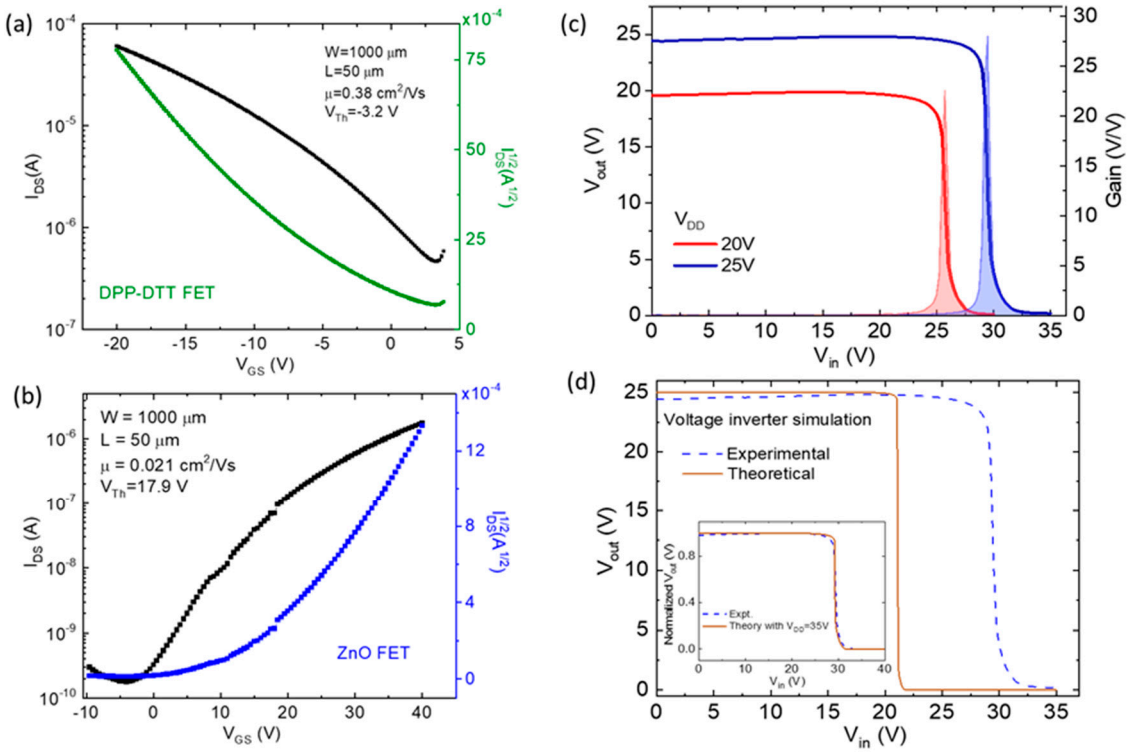

Figure 4. (**a**) Transfer characteristics of DPP-DTT FET using V-poled PVDF-TrFE as the dielectric (V_{DS} = −25 V). (**b**) Transfer characteristics of ZnO FET (V_{DS} = 40 V). Both of these FETs were used in the inverter circuit. (**c**) DC output characteristics of the complementary inverter at V_{DD} of 20 V and 25 V. The corresponding gain is shown by the shaded curves. (**d**) Simulated inverter output characteristics (bold brown line) along with the experimental data (dotted blue line). The inset shows the normalized experimental curve (same as in the main figure) and theoretical simulated curve at V_{DD} = 35 V.

Table 1 shows the parameters used in the inverter model. The theoretical simulations are plotted along with the experimental data in Figure 4d. One can reconcile with the differences. The higher V_T of the n-FET compared with the p-FET extends region 1 to high input voltages, in general. Even then, this region extends to higher voltages in the experimental data compared to the simulated data. Most likely the reason is two-fold: firstly, the magnitude of the current in the n-FET is smaller than the p-FET, requiring a higher input voltage for turning on the n-FET; secondly, the model used here is an ideal inverter without considering any leakage current or parasitic capacitance [34]. Leakage currents should be modelled as a parallel resistor to the inverter, which have not been taken into account in the simulations.

Table 1. The values of the individual parameters of p- and n-FETs used for the inverter model.

Parameter	P-Type	N-Type
L	1000 μm	1000 μm
W	50 μm	50 μm
V_T	−3.2 V	17.9 V
μ	0.38 cm^2/Vs	0.02 cm^2/Vs
λ	0.005 V^{-1}	0.0005 V^{-1}

Furthermore, it is interesting to note when the inverter simulations were performed at V_{DD} = 35 V, and when the experimental and theoretical output characteristics were normalized, as shown in the inset of Figure 4d, both experimental and theoretical curves mimicked each other. Using a very simple argument, this suggests that the additional voltage provides a higher input current to turn the n-FET on, taking into effect some of the leakage current through the FETs.

4. Discussion

The poling condition of the ferroelectric dielectric, PVDF-TrFE, plays a significant role in improving transport properties in organic FETs. Furthermore, the higher κ value of ferroelectric dielectrics compared to other non-ferroelectric polymer dielectrics or oxide dielectrics such as SiO_2 allow DPP-DTT FETs to operate at low voltages.

The sol–gel processing of ZnO results in robust n-type solution processable FETs, allowing the prospect of large-scale printing. We showed that a simple UV–ozone treatment improves the performance of FETs due to the filling of oxygen vacancies, eliminating trapping sites. The feasibility of sol–gel ZnO FETs in complementary inverter circuits was demonstrated. A simple analytical model was used to simulate the DC inverter characteristics using an open-source program. Such models, which may be further improved by incorporating parasitic capacitance and leakage currents, will guide the development of complementary inverter circuits using air-stable and solution-processable ZnO n-FETs.

Reducing V_T in ZnO FETs will improve the inverter characteristics. This may be achieved by using high κ dielectrics such as Al_2O_3. Future fabrication of inverters will involve integrating the p- and n-FETs in a vertical architecture, where the p-FET (with bottom-gate architecture and V-poled PVDF-TrFE) will be deposited on top of the ZnO FET. Selective patterning of the source-drain contacts with differing W/L ratios for both devices can also be used to improve the inverter characteristics. The solution processability of all layers opens up prospects for printing complementary inverter and ring oscillator circuits.

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