A 10-Output, Single-Inductor-Multiple-Output DC–DC Buck Converter With Integrated Output Capacitors for a Sub-mW System-on-Chip

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***Abstract*—Emerging sub-mW near-threshold-voltage system-on-chips require new power management architecture that can create multiple voltage domains with the fewest possible off-chip passives. To fulfill this need, we propose an ultra-low-power single-inductor–multiple-output dc–dc buck converter in a 65-nm CMOS process. Featuring a comparator-based output switch controller and a digital pulse-width modulation controller for ultra-low feedback latency, this dc–dc converter takes 1-V input voltage and produces ten independent output voltages from 0.4 to 0.8 V at the aggregated power delivery of 0.583 mW. It has ten 200-pF on-chip output capacitors and one 82-μH off-chip inductor and achieves the peak power conversion efficiency of 83.4%.**

***Index Terms*—Inductor-based power converters, integrated DC–DC power converters, near-threshold-voltage (NTV), single-inductor–multiple-output (SIMO) power converters, ultra-low power.**

I. Introduction

An emerging sub-mW near-threshold-voltage (NTV) system-on-chip (SoC) integrates multiple cores, embedded SRAM, network-on-chips (NoC), and other building blocks [1], [2]. To create multiple independent voltage domains, SoC architects conventionally employ an off-chip switching converter followed by an array of low-dropout voltage regulators (LDOs). However, this approach becomes less power efficient as the number of independent voltage domains in an ultra-low-power SoC increases and also the output voltage levels spread over an increasingly wider range, e.g., from I/O voltage down to near-/sub-threshold core voltages. This calls for creating new power management architecture that has the fewest possible off-chip components but creates multiple output voltages at high power conversion efficiency (PCE). A single-inductor–multiple-output (SIMO) dc–dc buck converter is a good candidate for this need as it requires potentially only one off-chip inductor [6].

In a typical sub-mW SoC, the silicon area of each voltage domain is not very large and so is the output capacitor that can be integrated/stacked in each domain. For example, [1] has 16 cores, each taking 0.25 mm^2 in a 65 nm. With a 2-fF/μm^2 MIM capacitor, the upper-bound of the on-chip capacitor integration is 100's of pFs. Fortunately, each core in [1] consumes only 20 μW and therefore the requirement of output capacitance is largely relaxed down to the 100's of pF. This renders it potentially feasible to integrate output capacitors.

However, only the reduced power level cannot fully enable the desired output capacitor integration. We have identified that it also requires decent feedback control whose feedback latency might be in the order of a single-digit ns for meeting output ripple size requirement (V_{ripple}). In Fig. 1, we elaborate the impact of the control latency. Suppose that the inductor is supplying current and charging an output capacitor and the output voltage just reaches to a reference level ($V_{\text{ref},i}$). The controller should stop the charging but it can stop only after the feedback control latency $t_{\text{lat,off}}$. During this $t_{\text{lat,off}}$, however, the output voltage ($V_{\text{out},i}$) increases beyond $V_{\text{ref},i}$ by $V_{\text{overshoot}}$. It can be formulated to: $V_{\text{overshoot}} = I_{\text{ind}} \cdot t_{\text{lat,off}}/C_{\text{out},i}$, where I_{ind} is the inductor current and $C_{\text{out},i}$ is the output capacitance. With the target parameter values, namely, $I_{\text{ind}} = 0.8$ mA, $C_{\text{out},i} = 200$ pF, $V_{\text{overshoot}} = 10$ mV, $t_{\text{lat,off}}$ must be less than 2.5 ns. Furthermore, after the charging, the output should wait until all the other outputs are served. During this time, V_{out} falls since it is sustained by the small output capacitor. To reduce this V_{out} fluctuation, i.e., V_{ripple}, we need low-latency feedback control. To achieve this, a prior SIMO converter uses a fast clock (100 MHz) for output control while using a slow clock (2 MHz) for input control [6], [7].

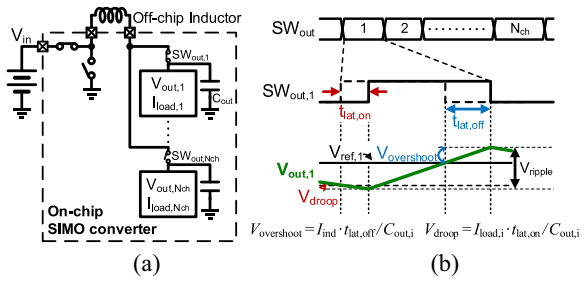

Fig. 1. (a) Concept of the SIMO converter and (b) impact of feedback control latency on V_{ripple}.

However, it is nontrivial to achieve such low latency with the tiny power budget given to the targeted ultra-low-power SIMO converter. For example, if we constrain the power budget of the control to be $< 10\%$ of the total load ($P_{\text{load,tot}}$) and if we assume $P_{\text{load,tot}} = 500$ μW for ten outputs, the power budget for control becomes only 50-μW total or 5 μW per output.

In this letter, we propose an SIMO converter with integrated output capacitors that is customized for a sub-mW SoC. It features: 1) a comparator-based output controller with output charge skipping logic and 2) a fully digital pulse-width modulation (PWM) controller. Both controllers are optimized to achieve high PCE for a large number of outputs (10) under the stringent constrains of C_{out} (200 pF/output) and V_{ripple} ($\pm 10\%$). The converter is prototyped in a 65 nm. It can convert 1-V input voltage (V_{in}) into 10 output voltages ($V_{\text{out},i}$), each independently regulated between 0.4 and 0.8 V. The only off-chip component is an inductor (82 μH) whose size is optimized for reducing C_{out} and increasing PCE. The converter achieves the peak PCE of 83.4%.

II. Proposed Converter Design

Fig. 2 shows the top-level architecture of the proposed SIMO converter. It consists of: 1) a comparator-based output controller; 2) a digital PWM controller; and 3) a zero-current detector (ZCD).

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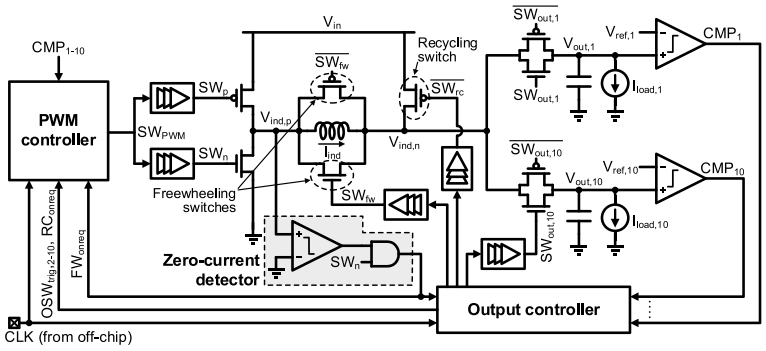

Fig. 2. Proposed SIMO converter architecture.

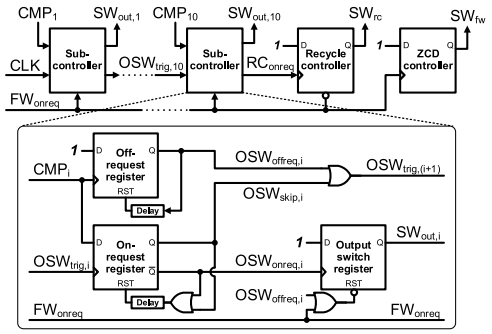

Fig. 3. Event-driven output controller.

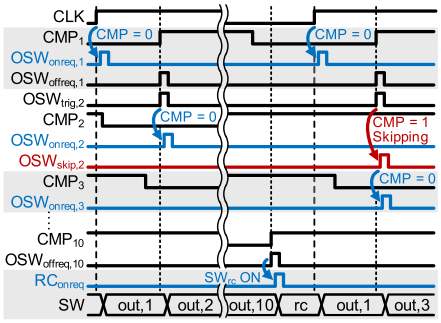

Fig. 4. Output controller timing diagram.

Fig. 3 shows the microarchitecture of the output controller. It contains: 1) ten cascaded subcontrollers controlling ten output switches ($SW_{out,i}$); 2) the recycle controller controlling the recycling switch (SW_{rc}); and 3) a ZCD controller for freewheeling switches (SW_{fw}) and also switching between continuous or discontinuous conduction mode (CCM, DCM) across the load levels.

The operation of the output controller is as follows (Fig. 4). In one inductor-switching period, each subcontroller controls its respective switch only once. Also, the order of these switch controls is fixed from the first to the last output and then to the recycling switch, while each control operation is initiated one by one in an event-driven fashion. After a subcontroller finishes to charge its output, the next subcontroller takes a token and checks its comparator output to decide if it will charge or skip. The skipping logic removes unnecessary charging operation, thereby improving PCE.

The skipping logic, however, can cause cross-regulation since it can modulate the amount of current to source in each input switching period. To prevent this, we employ the recycle controller, which can return any remaining inductor current through the recycling switch (SW_{rc}). It also helps to improve PCE. The recycling operation does not form a current loop, making stability less of concern [8]. The time that the recycling switch is turned on becomes near zero as the PWM controller modulates the duty cycle accordingly.

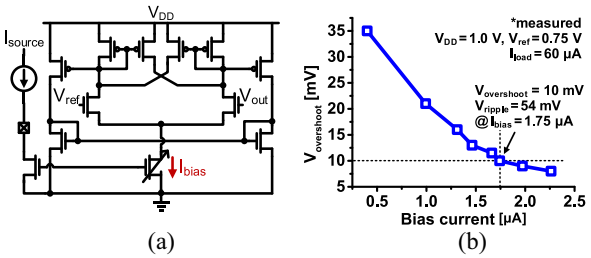

Fig. 5. (a) Schematic of the hysteretic CT comparator and (b) $V_{\text{overshoot}}$ of the comparator across I_{bias}s.

We also employ the ZCD controller whose goal is to prevent negative I_{ind}. It turns on the freewheeling switches (SW_{fw}) if I_{ind} becomes negative. The SW_{fw} forms a loop, but the current flowing in SW_{fw} is in general very small. As a result, this loop does not make severe stability issues [8]. In addition, the comparator-based output control, which our design adopt, may degrade stability if one of the output currents is larger than half the average of the sum of all the output currents, requiring a technique to compensate [9]. However, our converter has a large number of outputs. Also, the average inductor current is highly likely larger than each output current, making the aforementioned case a rare event.

The feedback latency of the output controller is critical for meeting the target V_{ripple}. The total latency is the sum of the latencies of the comparator, a flip-flop, and some logic gates. Parasitic-annotated SPICE simulation shows the comparator latency is dominant. It is ~1.38 ns on average and it contributes 57% of the total latency. While we can reduce the comparator latency by further increasing its bias current (I_{bias}), it would increase the comparator's power dissipation, and thereby degrading PCE. We set the bias current to 1.75 μA, which is small enough as compared to the target load current per output (10's of μA). This allows us to achieve the target V_{ripple} that is set to be less than 10% of $V_{\text{out},i}$ (Fig. 5).

We also designed the digital PWM controller (Fig. 6). Its goal is to modulate the duty cycle of SW_n and SW_p to match the inductor current close to the total load current. It can reduce the conduction loss and shorten or remove the on-time of SW_{rc}. The conventional analog PWM controller consumes non-negligible power [3]. The digital controller consumes ultra-low power and is more suitable for sub-mW SoC applications, especially at low supply voltage (1.0 V) [10]. On the other hand, the PWM controller has less demanding latency requirement. Therefore, we use the conventional synchronous control with slow clock frequency to reduce power consumption.

The PWM controller updates its output $D[k]$ which sets the length of the starved-inverter-based delay lines and thus the duty cycle of SW_{PWM} via the integral control law

$$D[k] = D[k-1] + \sum M_i[k-1] - t_{rc}[k-1]$$

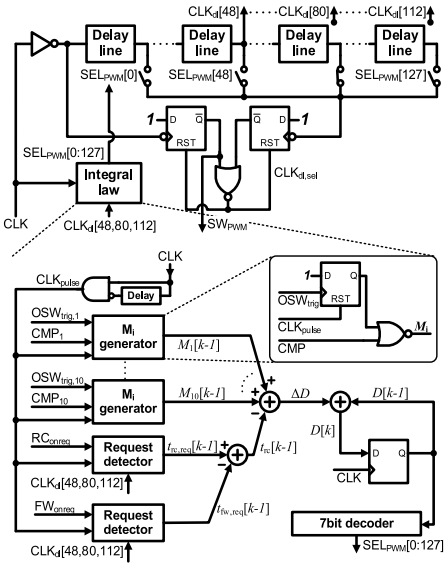

Fig. 6. Digital PWM controller.

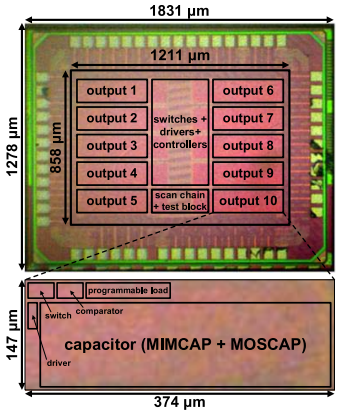

Fig. 7. Chip micrograph.

where $M_i[k] = 1$ represents if the ith output was not charged for the lack of time in the current CLK cycle although it should be. Each M_i generator produces $M_i[k]$ based on the comparator output (CMP) and $\text{OSW}_{\text{trig},i}$. On the other hand, $t_{rc}[k–1]$ represents the duration that the recycling switch was turned on in the previous CLK cycle, which can be formulated to

$$t_{rc}[k-1] = t_{rc,\text{req}}[k-1] - t_{fw,\text{req}}[k-1]$$

which is essentially from the switching time of RC_{onreq} ($t_{rc,\text{req}}$) to that of FW_{onreq} ($t_{fw,\text{req}}$). We design two request detectors, each measuring $t_{rc,\text{req}}$ and $t_{fw,\text{req}}$ with respect to the four time references already-available in the delay lines (CLK, $\text{CLK}_{dl}[48]$, $\text{CLK}_{dl}[80]$, $\text{CLK}_{dl}[112]$), producing the 2-bit digital value for $t_{rc}[k-1]$. We set the integral gain sufficiently low (1/128) to ensure stability.

III. Measurement Results

We prototyped the SIMO converter in a 65-nm process. Fig. 7 shows the chip micrograph. The total area is 1.04 mm^2. We target 10 outputs, which is larger than prior works, to meet the recent trends where a sub-mW SoC demand an increasingly large number of voltage domains [1], [2]. It employs an 82-μH off-chip inductor (Coilcraft 1812PS, 5.87 × 4.98 × 3.81 mm^3). We choose this rather large inductor because it helps to reduce the inductor current slope. This relaxes the requirements of the feedback latency and output capacitor size in the output controller under the target V_{ripple}

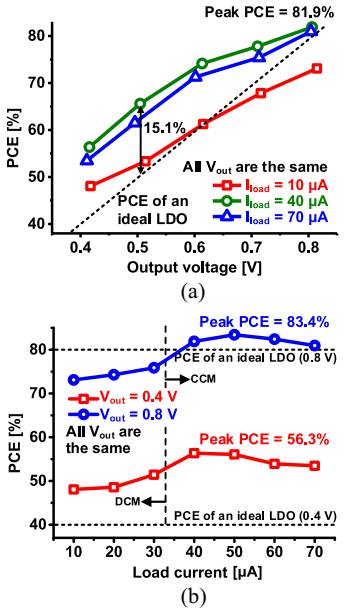

Fig. 8. Power conversion efficiency (PCE). (a) Across different output voltages and (b) across different load currents.

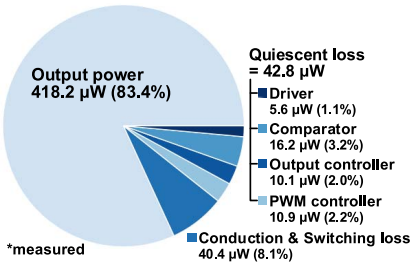

Fig. 9. Power breakdown.

constraint, thereby reducing the control loss and improving PCE. The converter can function with a smaller inductor yet it increases the inductor current slope, demanding short feedback latency and large output capacitor size. This results in lower PCE. The large inductor adopted in this design increases the cost and footprint of the system. Since the inductor size has a tradeoff relationship with the output capacitor size, it is important to carefully size an inductor and output capacitors to assess its suitability for target applications.

We measured PCE across different output voltages [Fig. 8(a)]. We set each of the output current to 10 μA, 40 μA, and 70 μA. We set all the output voltages to be the same while sweeping them from 0.4 to 0.8 V. The converter achieves the PCE of 48.1%–81.9%. This is up to 15.1% better than the PCE of the array of ideal LDOs. Fig. 8(b) shows the measured PCE across different output current. Here, we set all the output voltages to 0.4 and 0.8 V. When the output voltage is 0.4 V, the peak PCE is 56.3% which is 16.3% better than the PCE of the array of the ideal LDOs. The SIMO operates in the DCM mode when the output current becomes lower. In this mode, the quiescent loss makes a more significant impact on PCE. Fig. 9 shows the power breakdown. The quiescent loss is 42.8 μW. The controller hardware consumes 21.0 μW. The conduction and switching losses account for 8.1%.

Fig. 10 shows the measured steady-state waveforms. All outputs produce the targeted voltages (in 0.4–0.8 V) with V_{ripple} that is less than 10% of the output voltage. The first output having full load (70 μA) performs charging every CLK cycle while the fourth output having light load (25 μA) exercises the skipping logic.

Fig. 11 shows the transient response waveforms where $I_{\text{load},2}$ increases from 5 to 70 μA in 1 ns. The load-dependent dc offset (V_{offset}) is measured 13 mV and transient load regulation (dynamic

TABLE I
COMPARISON TABLE

	This work	[3] JSSC '15	[4] TPE '18	[5] VLSI '18	[6] JSSC '15
Design parameters					
Process	65 nm	350 nm	180 nm	180 nm	45 nm
# of outputs	10	10	4	9	5
V_{in}	1.0 V	5.0 V	2.7-3.7 V	1.8-2.5 V	1.6-2.0 V
$V_{out,i}$	0.4-0.8 V	1.8-3.3 V	1.0-1.8 V	0.5-5 V	0.6-1.6 V
Inductor	82 µH	10 µH	4.7 µH	9.9 µH	10-15 µH
$C_{out,i}$ (per output)	200 pF (on-chip)	10 µF (off-chip)	10 µF (off-chip)	2.2 µF (off-chip)	2-4.5 nF (on-chip)
f_{SW}	0.6-7.2 MHz	0.7 MHz	1 MHz	25 MHz	2 MHz (Input) 100 MHz (Output)
Steady-state performance					
Max total $I_{load,tot}/P_{load,tot}$	0.7 mA/0.583 mW	208 mA	203 mA	120 mW	110 mA
Peak PCE @ $P_{load,tot}$	83.4% @ $P_{load,tot}$ = 0.418 mW	88.7% @ $P_{load,tot}$ = 1196 mW	73% @ $P_{load,tot}$ = 195 mW	81.7% @ $P_{load,tot}$ = 120 mW	73% @ $P_{load,tot}$ = 138 mW
Max V_{ripple}	10% of V_{out}	40 mV	30 mV	+/-7% of V_{out}	80 mV
Quiescent loss*	42.8 µW	Not reported	Not reported	Not reported	3 mW
Power density (Inductor excluded)	0.402 mW/mm^2	Off-chip capacitors used	Off-chip capacitors used	Off-chip capacitors used	45.45 mW/mm^2
Transient performance					
Load step ($\Delta I_{load,i}$)	65 µA (93% of Max $I_{load,i}$)	100 mA (100% of Max $I_{load,i}$)	100 mA (100% of Max $I_{load,i}$	Not reported	7.5 mA (50% of Max $I_{load,i}$)
Load-dependent DC offset (V_{offset})	13 mV	17 mV	80 mV	Not reported	50 mV
FoM$_{Voffset}$**	40 ns	1.7 µs	8 µs	Not reported	13.3 ns
Transient load regulation (Dynamic V_{droop})	45 mV	Not reported	Not reported	Not reported	Not reported
Cross regulation	0	0.1 mV/mA	0.24 mV/mA	Not reported	0

* Quiescent loss is the power dissipation of controllers, comparators, and drivers.
** FoM$_{Voffset}$ = V_{offset} · $C_{out,i}$ / $\Delta I_{load,i}$ (The smaller is better)

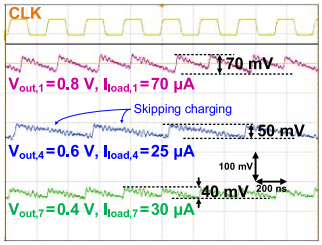

Fig. 10. Steady-state waveforms.

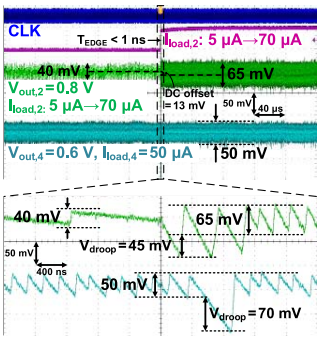

Fig. 11. Transient response waveforms.

V_{droop}) is 45 mV. No visible dc offset from cross-regulation is observed.

Finally, Table I shows the comparisons to the recent SIMO works. Unfortunately, the direct comparison to the existing works is difficult because they targeted 100's of mA of $I_{load,tot}$. To support such large power, they must employ nF to μF output capacitor per output. On the other hand, the large output power of the prior works relaxes the power budget of control hardware up to a few mW [6]. The proposed SIMO targets an emerging sub-mW SoC and aims to integrate all of the output capacitors and consume only tens of μW. With fully integrated output capacitors, it still achieves competitive performances in V_{ripple} (less than 10% of V_{out}), PCE (peak 83.4%), V_{offset} (13 mV), transient load regulation (45 mV), and cross-regulation. To compare with other works, we create V_{offset} figure-of-merit (FoM), which is defined as FoM$_{V offset} = V_{offset} \cdot C_{out,i}/\Delta I_{load,i}$ since V_{offset} increases with $\Delta I_{load,i}/C_{out,i}$. Our SIMO achieves 40 ns, which is competitive to the existing works. Considering the large number of outputs and ultra-low quiescent loss of this SIMO, it can be well utilized for low-power SoC applications.

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