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Sapphire-supported nanopores for low-noise DNA sensing

Pengkun Xia [a,b,c], Jiawei Zuo [a,b,c], Pravin Paudel [a,b], Shinhyuk Choi [a,b,c], Xiahui Chen [a,b,c], Md Ashiqur Rahman Laskar [a,b,c], Jing Bai [a,b], Weisi Song [d], JongOne Im [d,e], Chao Wang [a,b,c,*]

[a] School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA
[b] Center for Photonics Innovation, Arizona State University, Tempe, AZ, USA
[c] Biodesign Center for Molecular Design & Biomimetics, Arizona State University, Tempe, AZ, USA
[d] Biodesign Center for Single Molecule Biophysics, Arizona State University, Tempe, AZ, USA
[e] Curent Address: INanoBio Inc, Scottsdale, AZ, USA

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ABSTRACT

Solid-state nanopores have broad applications from single-molecule biosensing to diagnostics and sequencing. The high capacitive noise from conventionally used conductive silicon substrates, however, has seriously limited both their sensing accuracy and recording speed. A new approach is proposed here for forming nanopore membranes on insulating sapphire wafers to promote low-noise nanopore sensing. Anisotropic wet etching of sapphire through micro-patterned triangular masks is used to demonstrate the feasibility of scalable formation of small (<25 μm) membranes with a size deviation of less than 7 μm over two 2-inch wafers. For validation, a sapphire-supported (SaS) nanopore chip with a 100 times larger membrane area than conventional nanopores was tested, which showed 130 times smaller capacitance (10 pF) and 2.6 times smaller root-mean-square (RMS) noise current (18–21 pA over 100 kHz bandwidth, with 50–150 mV bias) when compared to a silicon-supported (SiS) nanopore (~1.3 nF, and 46–51 pA RMS noise). Tested with 1k base-pair double-stranded DNA, the SaS nanopore enabled sensing at microsecond speed with a signal-to-noise ratio of 21, compared to 11 from a SiS nanopore. This SaS nanopore presents a manufacturable nanoelectronic platform feasible for high-speed and low-noise sensing of a variety of biomolecules.

1. Introduction

Solid-state nanopores (Albrecht 2019; Perez-Mitta et al., 2019) have attracted considerable interest as a potentially high-speed, portable and low-cost solution for detecting a variety of biomolecules, such as proteins (Li et al., 2013; Yusko et al., 2017), RNA (Wanunu et al., 2010) and DNA (Dekker 2007), as well as studying molecular interactions (Kwak et al., 2016). However, the design and manufacturing of low-noise nanopore devices currently face a number of limitations. One major challenge in prevalent silicon-supported (SiS) solid-state nanopores is their large device capacitance due to silicon (Si) conductivity, which introduces a sizeable noise current that becomes particularly acute at high recording frequency, thereby causing serious reading errors. Although the noise can be mitigated by demoting recording bandwidths from 100 kHz to <10 kHz, this measure seriously limits the signal temporal resolution to ~100 μs, making it unable to resolve typical translocation events of a single DNA base pair in the range of 10–1000 ns (Feng et al., 2015). There have been other efforts aiming at slowing down the DNA translocation speed, including reducing its mobility or the effective DNA-driving force (Fologea et al., 2005; He et al., 2011), These efforts, however, have also introduced complexities in the experimentation process and a decrease in signal-collecting throughput. An alternative solution without sacrificing sensor performance is to reduce the device capacitance and noise from the nanopore device as well as the sensing system (Supplementary note 1). To minimize the stray capacitance of the Si chip, which can be as large as nano-farad range (Fig. S1c and Table S1), conventional techniques (Table S2) introduce a thick insulating material at the nanopore vicinity (Balan et al., 2014; Rosenstein et al., 2012). However, these fabrication schemes require complex, and manual processing techniques, such as thick dielectric deposition, selective membrane thinning, silicone/photoresist printing, glass bonding, *etc*, and thus are expensive, slow, and difficult to reproduce. Another approach is to replace conductive silicon with an insulating material, such as glass (Balan et al., 2015; de Vreede et al., 2019; Lee et al., 2014). The amorphous nature of glass substrates, however, prevents the formation of uniform membranes, and involves

* Corresponding author. School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA.
E-mail address: wangch@asu.edu (C. Wang).

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complex fabrication schemes, such as multiple lithography steps, as well as deposition and etching processes on individual chips. Accordingly, the broad availability of such glass-supported nanopore chips is very limited, primarily due to their low fabrication yield, poor reproducibility, and low throughput.

In this study, we demonstrate a new design concept for creating thin membranes and nanopores on crystalline and insulating sapphire wafers as a means to eliminate stray capacitance from substrate conductance for low-noise biosensing. The method involves creating sapphire-supported (SaS) nanopore membranes by wet and anisotropic etching of 2-inch sapphire wafers in concentrated sulfuric and phosphoric acids, a process similar to bulk alkaline etching of Si. Uniquely, we design a triangular window to reproducibly create sapphire chips with triangular membrane dimensions smaller than 25 μm with 6.8 μm deviation, which corresponds to picofarad level chip capacitance even considering nanometer-thin membranes in high-signal-to-noise-ratio (SNR) DNA detection.

2. Materials and methods

2.1. SaS nanopore membrane fabrication

250 μm thick 2-inch c-plane sapphire wafers, purchased from Precision Micro-Optics Inc., were RCA2 cleaned (deionized water: 27% hydrochloric acid: 30% hydrogen peroxide = 6: 1: 1, 70 °C) for 15 min. The RCA2 surface cleaning promotes film adhesion to the substrate, which otherwise can result in film cracking during high-temperature sapphire etching (Fig. S2). One to 3 μm silicon oxide (SiO_2) (thicker is preferred for larger membranes) was then deposited via plasma-enhanced chemical vapor deposition (PECVD, 350 °C, deposition rate 68 nm/min) on both sides, followed by photolithography and reactive-ion-etching (RIE) (PlasmaTherm 790, CHF_3 based chemistry, etching rate 46 nm/min) to form a triangular etching window in SiO_2. Next, hot sulfuric acid and phosphoric acid (3:1, solution temperature ~300 °C) were used to etch through the sapphire wafer (etching rate up to 12 μm/h) and to suspend the SiO_2 membrane. To ensure the safety of handling hot acids, we custom-designed a quartz glassware setup suitable for the high-temperature acid-based sapphire etching process (Fig. S3). The sapphire wafer was intentionally placed vertically in a 2-inch glass boat in the etching container to minimize possible damage to the membrane from the boiling acids. We added acid to the quartz glassware, and then loaded the 2-inch glass boat with the wafer into the quartz glassware. A clamp seal and a condenser column were then installed on top of the glassware to minimize acid vapor leakage. The etching rate was chosen to be relatively slow in this customized container to minimize wafer breakage during etching; however, further increasing the solution temperature is an option to exponentially increase the etching rate and thus allow for larger throughput.

Following sapphire etching, the SiO_2 membrane was thinned down as needed by RIE to <1.5 μm. This was followed by depositing a layer of silicon nitride (SiN) (30–300 nm) onto the SiO_2 membrane via low-pressure chemical vapor deposition (LPCVD) (Tystar TYTAN 4600, 750 °C, deposition rate: 6 nm/min). The unintentionally deposited SiN in the back cavity of the chip was removed by RIE. Next, hydrofluoric acid (8%) was used to etch the SiO_2 layer (90 nm/min) to suspend the SiN layer. The final SiN membrane was thinned down as needed by hot 85% phosphoric acid (etching rate ~2.5 nm/min) to desired thickness.

2.2. SiS nanopore membrane

The SiS nanopore membranes were purchased from SiMPore Inc. The chips were made from 100 mm diameter, 200 μm thick, float-zone Si wafer (resistivity of 1–10 Ω cm) with ~100 nm thermal SiO_2 and ~20 nm LPCVD SiN films, where the thermal SiO_2 from the cavity side was removed to produce an array of suspended SiN membranes of 4–5 μm in diameter. The SiO_2 and SiN film thicknesses were confirmed by M-2000 ellipsometer (J.A. Woollam Co.) as 99 nm and 23 nm, respectively.

2.3. Thickness characterization of small membranes

The thicknesses of membranes were determined by optical reflectance measurement (Filmetrics F40) and by subsequent fitting. An experimentally measured refractive index of the SiN films on a Si monitor sample (Woollam Spectroscopic Ellipsometer) was used to improve fitting accuracy.

2.4. Nanopore drilling

A JEOL 2010F transmission electron microscope (TEM) was used to drill the nanopores. The 5 mm by 5 mm nanopore chips were diced and placed in a customized TEM sample holder. The largest condenser aperture and beam spot size were used for maximum beam current output. After alignment, imaging magnification was maximized (1.5M), followed by 5–15 min beam stabilization. The focus was re-adjusted when beam drifting was severe; beam stabilization was then re-monitored at maximum magnification. Upon stabilization, the beam spot was reduced to ~7 mm and rounded by adjusting the condenser astigmatism. Under the conditions of 7.01 kV anode A2 (focusing anode), 3.22 kV anode A1 (extraction anode), and 30 nm SiN membrane, it typically took 75–90 s to drill through the membrane.

2.5. Noise characterization, DNA preparation, and DNA sensing

The TEM-drilled nanopore chip was treated with UV ozone cleaner (ProCleaner™, BioForce Nanosciences Inc.) for 15 min to improve hydrophilicity. The chip was then mounted onto a customized flow cell (Fig. S4). A solution of 1:1 mixed ethanol and DI water was injected into the flow cell to wet the chip for 30 min. The solution was subsequently flushed away by injection of DI water. Next, 100 mM KCl was injected into the flow cell to test the current-voltage (IV) curve using an Axopatch 200B amplifier and a Digidata 1440A digitizer (Molecular Devices, LLC.). A 1M KCl solution was injected for characterization of the device current.

For DNA sensing, 1k bp dsDNA (Thermo Scientific NoLimits) was diluted using 1M KCl to 5 ng/μL. Poly$(A)_{40}$ ssDNA (Standard DNA oligonucleotides, Thermo Fisher Scientific Inc.) was diluted using 1M KCl to 50 nM, followed by brief vortex mixing. The DNA solution was injected into the flow cell to collect DNA signals under a 10 kHz and 100 kHz low-pass filter with a sampling frequency of 250 kHz at 50, 100, and 150 mV bias voltages. The flow cell was kept in a customized Faraday cage on an anti-vibration table (Nexus Breadboard, Thorlabs, Inc.) to minimize the environment noise during measurement. The DNA signals were observed and recorded with the Clampex software. Finally, an edited MATLAB program was used to convert all the. abf files to. mat files. All the collected DNA signals were then imported to an OpenNanopore program (Raillon et al., 2012) to generate the dwelling time and blockade current amplitude data of each DNA signal for subsequent analysis.

3. Results and discussion

3.1. Silicon oxide (SiO_2) supporting membrane formation

We have devised a new strategy to create suspended dielectric membranes on sapphire by anisotropic wet etching (Fig. 1). PECVD-deposited SiO_2 (Fig. 1b) was used here due to its high-selectivity in masking sapphire etching, which we experimentally determined to be over 500:1. Considering the three-fold symmetry of sapphire crystal, we patterned triangular shaped SiO_2 etching masks and studied how the alignment angle between such masks and sapphire crystal (denoted α) could affect the membrane evolution (Fig. 1 h-i). The process is similar to alkaline etching of Si but more complex given its hexagonal lattice

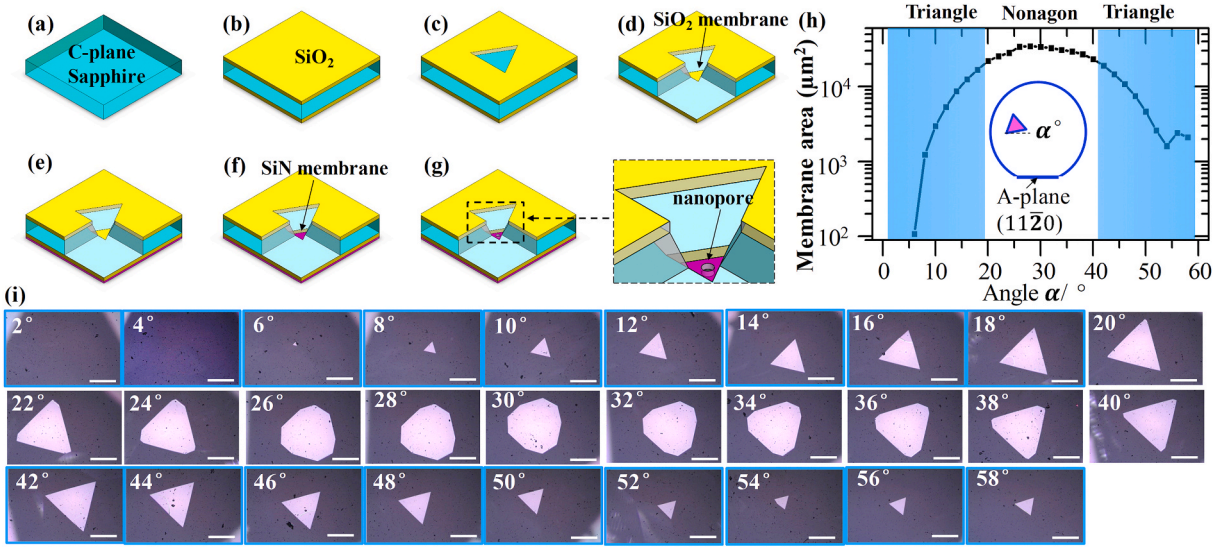

Fig. 1. Nanopore fabrication scheme and experimental data of creating membranes on sapphire. (a–g) Key steps in nanopore sensors fabrication: (a) A 250 μm sapphire wafer is cleaned by solvents and RCA2. (b) A layer of PECVD SiO_2 is deposited on both sides of the sapphire wafer. (c) A window is formed in the top SiO_2 by photolithography and RIE. (d) The sapphire is etched through in hot sulfuric acid and phosphoric acid, forming a suspended SiO_2 membrane. (e) A thin layer of LPCVD SiN is deposited on the bottom SiO_2 membrane, and unintentionally deposited SiN in the cavity is etched by RIE. (f) The thin SiN membrane is formed by first selectively removing the SiO_2 membrane and then optionally thinning the SiN in hot phosphoric acid. (g) A nanopore is drilled by TEM in SiN membrane. One corner of the chip is hidden in schematic d-g to better visualize the central etching cavity. (h) Experimental study showing how the membrane area is affected by the alignment offset angle (α) from the etching window to the sapphire flat. (i) Optical images of formed membranes on sapphire as α changes from 2 to 58°. Scale bar: 100 μm.

nature (Chen et al. 2012, 2013). Interestingly, we found that triangular membranes formed when $0 < \alpha < 20°$ and $40° < \alpha < 60°$, but the two different sets were offset by a rotational angle of ~30° (Fig. 1h and i). In contrast, complex polygon membranes with up to nine sides emerged when $20° < \alpha < 40°$. Additionally, the membrane area was found sensitive to α, yielding an area of more than three orders of magnitude larger when $\alpha \sim 30°$ compared to $\alpha \sim 0°$. Given that the M- and A-planes of sapphire have very slow etching rates and are perpendicular to the c-plane, they are believed to be less relevant in the observed cavity formation. We instead suspect that the formation of and competition between R- and N-planes of the sapphire crystals are most relevant (Xing et al., 2019) in the angle-dependent membrane geometry evolution. We also evaluated the square window designs, which are used in Si etching for the cubic lattice structure; here, we found that they only produced irregular and complex membranes that are much more difficult to control (Fig. S5).

Since sapphire essentially eliminates the stray capacitance through the substrate, the membrane capacitance of the SaS chips, which is highly dependent on membrane area and thickness, largely determines the total chip capacitance and high-frequency noise. Here, we demonstrate fabrication of micrometer-sized membranes that are most attractive for picofarad sensor capacitance and low-noise biosensing (Fig. 2a). To guide the mask layout design, we first performed theoretical calculations to study the relationship between the membrane and the mask dimensions while keeping $\alpha = 0°$. The membrane triangle length L_2 could be engineered by the mask triangle length L_1 following $L_1 = L_2 + \frac{2\sqrt{3}h}{\tan\theta}$ (Supplementary note 2 and Fig. S6b), where h is the sapphire wafer thickness and θ is an effective angle between the exposed facets in the cavity and sapphire c-plane that can be empirically determined. Indeed, by designing L_1 from ~750 μm to ~900 μm, we demonstrated modulation of the SiO_2 membrane size L_2 within a wide range, from 5 to 200 μm (Fig. S6 c-d). Further, by fitting the experimental data with a theoretically calculated L_1-L_2 relationship, we could estimate that the best empirical value for facet angle θ is ~50°. Based on this knowledge, we designed L_1 as 760, 762, 764, and 766 μm and α~0° for wafer-scale fabrication of <20 μm size membranes, which are most attractive for picofarad sensor capacitance and low-noise biosensing (Fig. 2d). Etching two 2-inch sapphire wafers in the same batch, we discovered no wafer or membrane breakage, and successfully obtained 116 suspended micron-sized membranes while having 4 membranes not yet completely etched through. We expected further etching would eventually create these 4 membranes while slightly enlarging the existing ones due to slower lateral etching on exposed facets. From intentionally patterned rectangular dicing marks surrounding the cavity etching windows, trenches were formed in sapphire wafers after acid etching, allowing even-hand dicing of 5 mm square chips (Fig. 2e) despite the hexagonal crystal structure of sapphire. Importantly, this wafer-scale demonstration strongly indicated the scalability of our membrane formation process, which is crucial to future large-scale, cost-effective sensor fabrication. Furthermore, we studied the size reproducibility of the small membranes on the two wafers (Fig. 2f–g and Fig. S7). The average size of all membranes was found to be about L_2= 12.1 μm with a standard deviation of 6.7 μm for wafer 1 and L_2= 9.2± 6.6 μm for wafer 2. We found 41% (48 out of 116) of the membranes were smaller than 10 μm, which corresponds to 2–3 pF chip capacitance even considering nanometer-thin membranes, *e.g.* 2.8 pF, 2.1 pF, and 1.8 pF at 2, 5, and 10 nm thickness (more details in Table S3). Further, a majority of the membranes (91%, 105 out of 116) were <20 μm and all were <25 μm, indicating we should expect 4 pF and 3 pF chip capacitance at 5 nm and 10 nm membrane thicknesses. Such low capacitance is highly desired for high-SNR DNA detection (Rodriguez-Manzo et al., 2015; Wanunu et al., 2010).

When compared to the best available low-noise SiS chips and glass-supported chips (Table S2) that typically have a membrane capacitance of <10 pF (Balan et al. 2014, 2015; de Vreede et al., 2019; Park et al., 2016; Rosenstein et al., 2012), we find that SaS chips are very competitive in their expected small capacitance and corresponding capacitive noise. Noticeably, the low-noise SiS and glass chips all require very complicated fabrication processes. For example, the SiS membranes need to be very carefully engineered to reduce the membrane area and introduce thick insulating layers, demanding processes involving nanolithography, bonding, film deposition, etching, and even silicone painting.

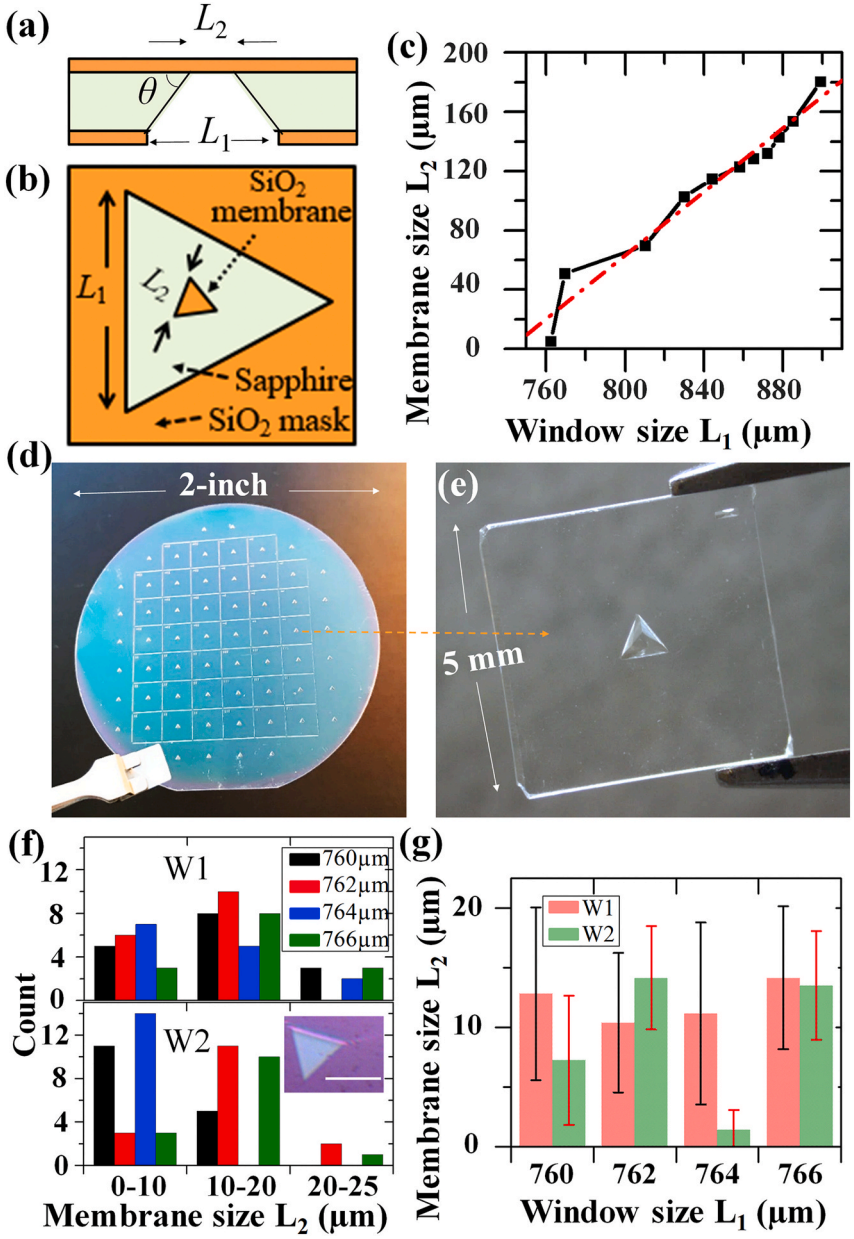

Fig. 2. Experimental demonstration of creating SiO_2 membranes on sapphire wafers. (a–b) Side-view and top-view schematics of a sapphire chip. L_1 and L_2 are the window and the membrane side lengths, respectively. θ is defined as the effective facet angle relative to the c-plane after etching. (c) Quasi-linear relation between L_2 and L_1. (d) An optical image of a 2-inch sapphire wafer with intact SiO_2 suspended membranes formed. (e) An optical image of a 5 mm by 5 mm sapphire chip diced from a 2-inch wafer. (f) SiO_2 membrane dimension distributions on two wafers (W1 and W2) with all smaller than 25 μm. The inset shows an optical image of 5 μm SiO_2 membrane on wafer 2 (scale bar 5 μm). (g) Measured average membrane sizes (L_2) versus different window sizes (L_1) with error bars. Each average value is obtained from measurement of 14 or 16 chips.

The key challenge in fabricating glass chips lies in the reproducibility of creating small membranes on glass, because bulk and isotropic etching of amorphous glass in hydrofluoric acids (HF) has poor dimension control while RIE etching is only applicable at single-wafer or single-chip level with drastically lowered throughput and increased manufacturing cost. Although combining femto-second laser ablation with LPVCD and chemical wet etching could form glass chips with a ~2 pF device capacitance (An et al., 2008; de Vreede et al., 2019), it remains unclear how the membrane uniformity (reported variation from 5 to 40 μm), fabrication throughput, and yield are affected by process fluctuation in laser ablation and chemical etching. We believe our wafer-scale SaS chip design and fabrication strategy presents a new scalable manufacturing alternative to the prevalent manufacturing processes of low-noise sensors that are complicated, time-consuming, low-yield, and costly.

In our demonstration, the observed membrane size variation within the wafer could be attributed to a few factors. First, the sapphire wafers were found slightly thinner (~1 μm) at the edge than at the center, which could cause membrane enlargement at the edge. Second, our customized hot-plate based etching apparatus could leave a temperate gradient in the acid bath that could affect the etching rate. Further, acid convection under boiling condition may produce local variation in acid concentration and etching rate. Lastly, the complex evolution of sapphire facets (Fig. S6a), currently not fully understood but thought to be due to the competition between R- and N-planes of the sapphire crystals, could be sensitive to crystal orientation alignment and the etching bath conditions. In future studies, the membrane uniformity could be improved by compensating etching window sizes over the wafer, utilizing an etching system that provides better temperature control and acid circulation, and further studying the etching mechanism and optimizing the etching window designs.

3.2. SiN thin membrane formation

Using the triangular SiO_2 membranes formed by sapphire etching, we have developed a process to create thin SiN membranes suitable for nanopore formation and DNA sensing (Wanunu et al., 2010). Briefly, we deposited low-stress LPCVD SiN film on suspended SiO_2 membranes,

and then removed the SiO_2 film via selective dry etching and HF based wet etching from the cavity side (Fig. 1f). The use of SiN film allows us to precisely control the membrane thickness and minimizes the impact of SiO_2 film stress on the membrane structural integrity. The SiN film can be further thinned down to desired thickness when necessary by either RIE and/or wet etching in hot phosphoric acid. We found that RIE could cause non-uniformity (Fig. S8a) and might damage the membrane, causing current leakage, as shown by current-voltage (*IV*) characteristics (Fig. S8b). In contrast, wet etching in hot phosphoric acid yielded uniform SiN membrane (Fig. S8c and Fig. S8b) without current leakage (Fig. S8d), and thus preferable for our DNA sensing test. Finally, a nanopore was drilled in the SiN membranes on the sapphire chip (Fig. 3a-b) and the float-zone Si chip (SiMPore Inc., Fig. S9) using TEM (Fig. 1g) for electrical characterization and DNA sensing.

Here we characterize the device capacitance of the SaS and SiS nanopore chips. Noticeably, the SaS nanopore chip had a 100 times larger membrane area ($L_2 = 68$ μm, or ~2000 μm^2 in area) than the SiS chip (4.2 × 4.7 μm square, or ~20 μm^2) and slightly thicker SiN (measured 30 nm for sapphire and ~23 nm for Si). The membrane capacitance C_m was estimated at 3.8 pF for the SaS chip, >70 times greater than that of the SiS chip (0.05 pF), following $C_m = \varepsilon \frac{A}{d}$, where ε is the permittivity of SiN, and A the membrane area and d membrane thickness. Experimentally, C_m was found ~10 pF for the SaS chip, with a deviation from theoretical value possibly attributed to slightly smaller SiN thickness in reality, and much smaller than that of the SiS chip (~1.3 nF) because of the stray capacitance from Si substrate. Clearly, considering SaS and SiS nanopores that both have only the simplest membrane structure, it is clear that insulating sapphire successfully eliminates the dominant capacitance resulting from Si substrate conductivity, thus appealing to low-noise measurement.

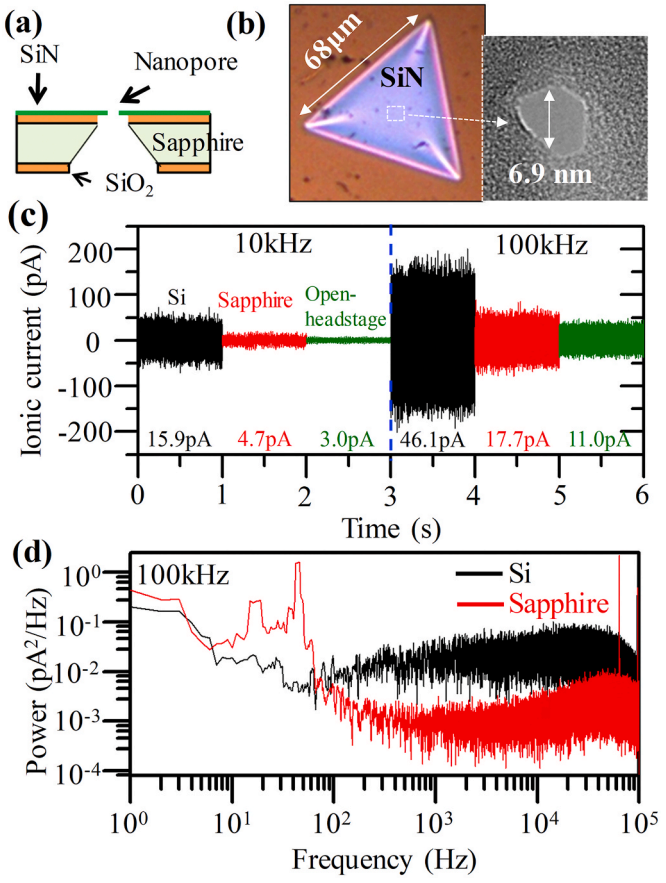

Fig. 3. Ionic current noise analysis of a SaS nanopore and a SiS nanopore. (a) A schematic of the measured SaS nanopore chip. (b) An optical image of the SiN membrane of the SaS nanopore chip and a TEM image of the drilled nanopore. (c) The ionic current noise for the SiS nanopore (black traces), the SaS nanopore (red traces), and the open-headstage state (green traces) under 10 kHz (left three traces) and 100 kHz (right traces) low-pass filter, respectively. The two chips were both measured under 50 mV voltage. The RMS ionic current values were also analyzed and marked for each measurement. (d) Power spectra of the current noise of the SaS nanopore and the SiS nanopore versus frequency under 100 kHz low-pass filter. The two chips were both measured under 50 mV voltage. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

3.3. SaS nanopore noise characterization

We further analyzed the ionic current noise for the SaS nanopore, the SiS nanopore, and the open-headstage system (Axopatch 200B) under 10 kHz and 100 kHz low-pass filter (Fig. 3c). The root-mean-square (RMS) of the measured current of the SaS nanopore chip was ~5 and 18 pA using 10 and 100 kHz filters, which was only slightly higher than the open-headstage system RMS noise (3 and 11 pA), and yet much better than those from our SiS nanopores (~16 and 46 pA). In comparison, the best reported silicone-painted SiS chips (Rosenstein et al., 2012) that utilized a locally thinned membrane (0.25 μm^2 area and 10–15 nm thick in the center) produced ~7 and ~13 pA noise current at 10 kHz and 100 kHz, measured by an optimally designed amplifier that outperforms Axopatch 200B in high-frequency recording. Additionally, we compiled the reported noise current from glass-supported nanopore chips (Table S2). For example, one of the best glass chips with nano-membrane (*e.g.* 100 nm diameter, 0.008 μm^2 in area, and 5–10 pF) measured ~4 and ~13 pA noise current at 10 kHz and 100 kHz, respectively (Park et al., 2016). Glass chips with micro-membranes (25 μm^2 and 70 pF (Lee et al., 2014), and 314 μm^2, ~2 pF de Vreede et al., 2019) measured ~13 and ~19 pA noise current at 10 kHz bandwidth, which is approximately 3–4 times larger than our SaS chip. The above comparison convincingly shows that our SaS chips are successful in suppressing the noise current and are wholly comparable to the best reported Si- and glass-supported nanopore chips.

Additionally, our analysis of the power spectral density (PSD) (Fig. 3d) further demonstrates that the SaS nanopores outperformed the SiS chips, particularly at high bandwidth (*e.g.,* >10 kHz) due to the significantly reduced device capacitance. In the moderate frequency range (*e.g.,* 100 Hz to 10 kHz), the noise power of the SaS nanopore was about one order of magnitude smaller (~10^{-3} pA^2/Hz) than that of our measured SiS nanopore (~10^{-2} pA^2/Hz) and one order of magnitude smaller or comparable to the glass chips and low-noise SiS chips (10^{-2}–10^{-3} pA^2/Hz) (Balan et al., 2014; de Vreede et al., 2019; Lee et al., 2014; Park et al., 2016; Rosenstein et al., 2012) (Table S2), partly attributed to lower dielectric noise and Johnson noise. We note that sapphire has a very small dissipation factor D (~10^{-5}), two to five orders of magnitude smaller than that of typical borosilicate glass (10^{-3} to 10^{-2}) and Si (1–100) and comparable to that of high-purity fused silica (~10^{-6}) (Westphal and Sils 1972). Such a small dissipation factor, together with its small device capacitance, is favorable for minimizing noise related to dielectric loss (Wen et al., 2017) $S_D \propto DC_{chip}f$, where C_{chip} is nanopore chip capacitance and f is the frequency. Additionally, the high resistivity of sapphire (>10^{14} Ω·cm) also served to minimize resistance-related Johnson noise. At very low frequency range (<100 Hz), the noise power of the SaS nanopore was about 10^{-1} pA^2/Hz, one order higher than SiS nanopore (10^{-2} pA^2/Hz), which could be attributed to the flicker noise and could be further improved by surface modification (Tabard-Cossa et al., 2007). From the above analysis, it is again evident that SaS chips are completely comparable to the best available SiS and glass-supported nanopore chips. Our demonstrated batch-processing-compatible design not only significantly simplifies the fabrication process, but also makes it potentially competitive in sensor price compared to the best available low-noise sensors fabricated on low-resistivity silicon and glass (fused silica or quartz) substrates.

3.4. DNA detection

To evaluate the performance of DNA molecule detection capability of our SaS nanopore, 1k bp ds-DNA were translocated through the SaS and the SiS nanopores at 100 kHz (Fig. 4) and 10 kHz (Fig. S10) low-pass filters under 50 mV, 100 mV, and 150 mV bias, respectively. By comparing representative ionic current traces of 1k bp dsDNA (Fig. 4b), we observed that the DNA signals collected by SiS nanopore displayed severe signal distortion, particularly at lower bias voltages. These irregular signals, together with the high baseline noise, made it very challenging to faithfully distinguish DNA signals from the background. In comparison, the SaS nanopore produced easily distinguishable DNA signals with much less distortion or noise at as high as 100 kHz bandwidth. Additionally, low-frequency recording, *e.g.,* at 10 kHz, would result in serious data loss of fast DNA signals, thus presenting only longer and in some occasions distorted signals (Park et al., 2016; Rosenstein et al., 2012). Clearly, SaS nanopores enable high-speed, high--throughput, and high-fidelity detection of DNA signals.

To study the DNA translocation mechanism from the SaS chip, we extracted the DNA signals using the OpenNanopore Program (Raillon et al., 2012), and then scatter-plotted the fractional blockade current I_B ($=i_b/i_0$) and the dwelling time Δt of all the DNA events under 50 mV (Fig. 4c). Here i_b is the blocked-pore current and i_0 is the open-pore current. The use of I_B allows us to eliminate the impact of bias difference on DNA signal analysis. Two distinct populations were observed, as seen separated by the red dashed line in Fig. 4d, and recognized as the translocation events (green oval) and the collision events (pink oval) (Wanunu et al., 2008). Further, we analyzed the current blockade distribution and fitted with Gaussian function (Fig. 4d), producing two distinct I_B populations attributed to translocation and collisions. We further analyzed the dwelling time Δt of each of the two event populations and fitted with exponential decay function (black lines, Fig. 4e). This showed that the translocation events (green, top panel) had a longer tail (decay constant 16.19 μs) than the collision events (decay constant 8.45 μs), consistent with previous studies (Wanunu et al., 2008).

We further applied this signal segregation approach to analyze all the DNA signals collected from the SiS and SaS nanopores (Fig. 5 a-d). By scatter-plotting the normalized DNA blockade signal ($1\text{-}I_B = \Delta I/i_0$) and marking the normalized current noise (I_{RMS}/i_0, dash-dot lines) at each bias voltage (black: 50 mV, red: 100 mV, blue: 150 mV, Fig. 5e and f), we could investigate the SNR (defined here as $\frac{\Delta I}{I_{RMS}} = \frac{1-I_B}{I_{RMS}/i_0}$) of the true DNA translocation signals. The short solid lines represent the average DNA signals ($1\text{-}I_B$) determined from the Gaussian distribution of the translocation events (Fig. 5b, d). The SaS nanopores are seen to produce slightly smaller DNA signal amplitude than SiS nanopores because of their larger pore size and thicker membrane. Noticeably, given the suppressed noise current, the SaS nanopore still evidently outperformed the SiS nanopore in SNR. For example, the SaS nanopore has a SNR of 21 at 150 mV bias, almost twice as good as the SiS nanopore with a SNR of 11. Generally smaller nanopore and thinner membrane are preferred for optimal signals and SNRs. Our experimental data illustrated the impact of pore sizes on the DNA signals for both SiS (*e.g.*, 4 nm, 7 nm) and SaS (*e.g.*, 7 nm, 20 nm) nanopore chips (Fig. S11). Additionally, thinner SiN (*e.g.* down to 5 nm) and few-layer to monolayer 2D materials can be explored as the membrane to improve the signal and SNR.

We further attempted to detect short single-stranded (ss) DNA molecules using SaS nanopores (Fig. S12). Ionic current traces of $Poly(A)_{40}$ ssDNA translocation events were recorded under 100 kHz low-pass filter with the voltages from 100 mV to 150 mV. We performed the same analysis to investigate the SNR of this ssDNA (Fig. S12b and Fig. S13) and obtained a SNR of ~6 for both 100 mV and 150 mV bias voltages. This provided evidence that the SaS nanopores can detect a wide range of biomolecules of different sizes. We expect that SNR can be remarkably enhanced by using thinner membrane thickness and smaller nanopore in future studies.

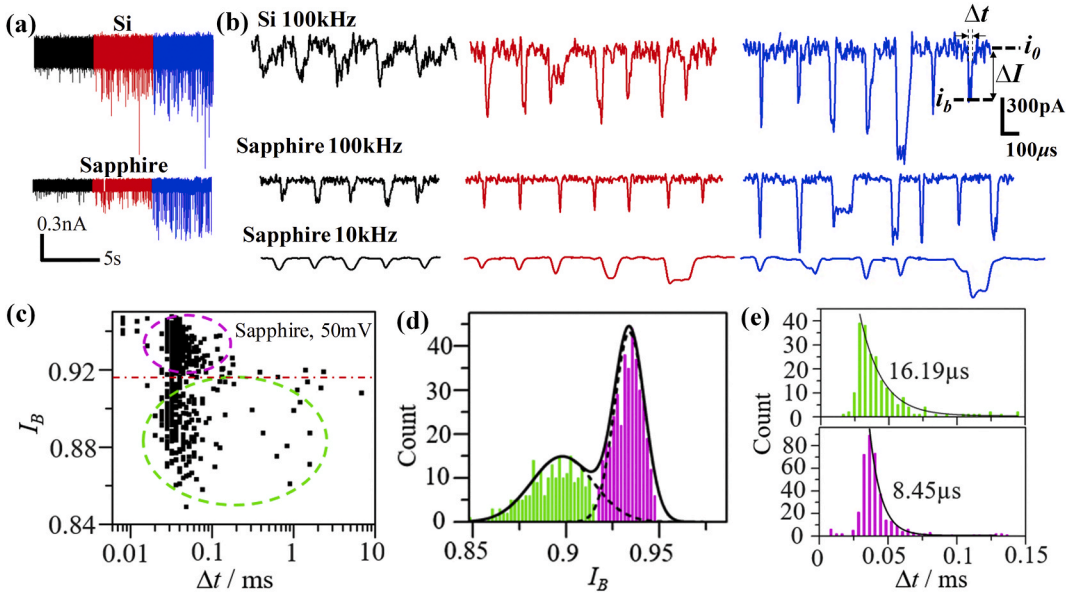

Fig. 4. Analysis of 1k bp dsDNA translocation events for the SaS nanopore (~2000 μm^2 membrane area) and the SiS nanopore (~20 μm^2 membrane area) under 100 kHz filter frequency. (a) The current traces of the DNA translocation events of the SiS nanopore and the SaS nanopore under different voltages (black: 50 mV, red: 100 mV, blue: 150 mV). (b) Representative DNA events for the SiS nanopore and the SaS nanopore at different voltages (black: 50 mV, red: 100 mV, blue: 150 mV) and different recording bandwidth (top two rows: 100 kHz, bottom row: 10 kHz). Δt: event dwelling time; i_0: open-pore current baseline; i_b: block-pore current level; ΔI: blockade current amplitude. (c) Scatter plot of the fractional blockade current I_B ($=i_b/i_0$) versus the dwelling time Δt of all the DNA events from the SaS nanopore under 50 mV. Two distinct populations are separated by the red dashed line as the translocation events (green oval) and the collision events (pink oval). (d) The histograms of I_B of the SaS nanopore under 50 mV displaying two distinct peaks corresponding to the translocation events (green bars) and the collision events (pink bars). The solid and dash black lines indicate the fitting by Gaussian function. (e) Histograms of Δt of the segregated events based on two I_B populations, fitted by exponential function. The translocation events (top panel) has a longer tail (decay constant 16.19 μs) than the collision events (lower panel, decay constant 8.45 μs). (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

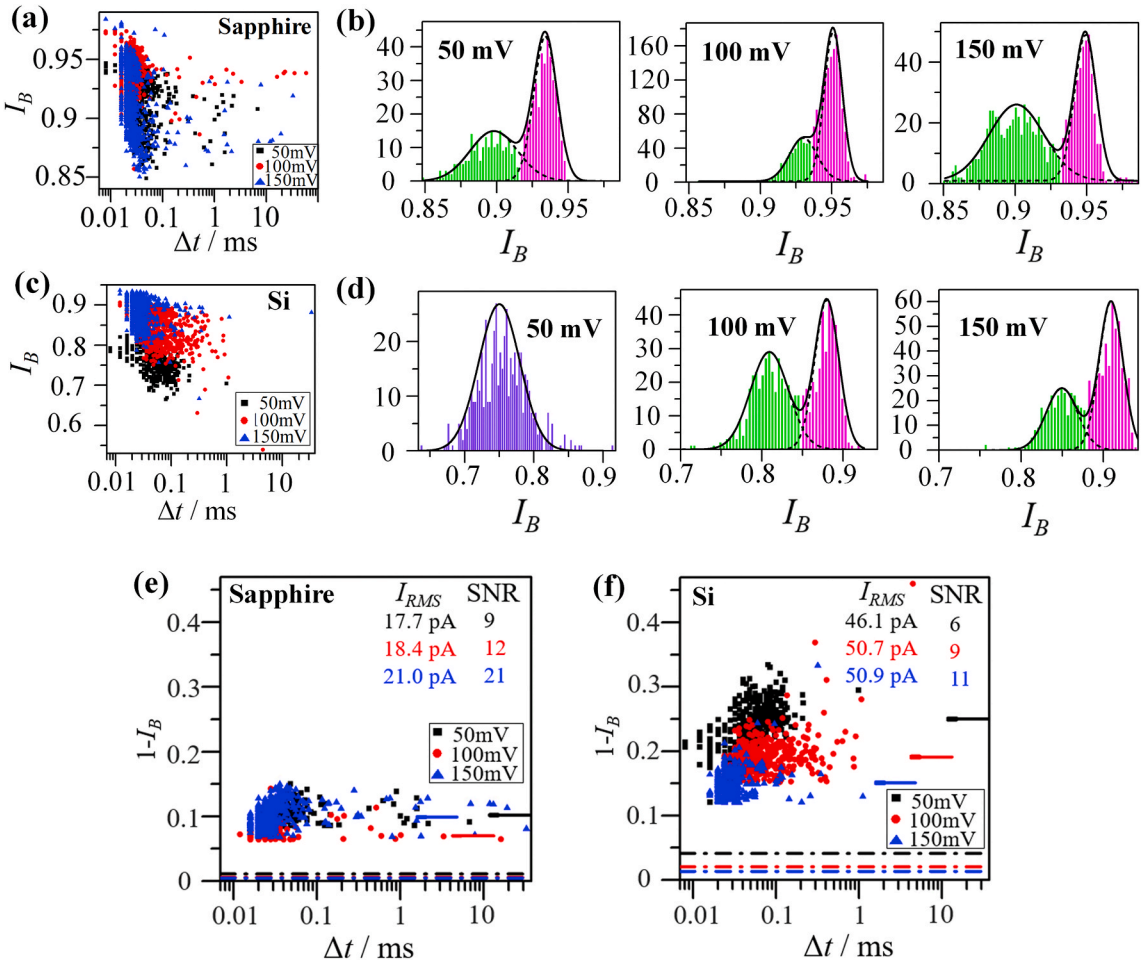

Fig. 5. Signal-to-noise ratio (SNR) comparison between the SaS nanopore and the SiS nanopore under 100 kHz filter frequency. (a) Scatter plot of the fractional blockade current I_B ($=i_b/i_0$) versus the dwelling time Δt of all the DNA events from the SaS nanopore under different bias voltages from 50 mV to 150 mV. (b) The histograms of I_B of the SaS nanopore. Two distinct peaks are observed and fitted by Gaussian function, corresponding to the translocation events (green bars) and the collision events (pink bars). (c) Scatter plot of the fractional blockade current I_B ($=i_b/i_0$) versus the dwelling time Δt of all the DNA events from the SiS nanopore. (d) The histograms of I_B of the SiS nanopore. Two distinct peaks are observed for 100 mV and 150 mV biases and fitted by Gaussian function, corresponding to the translocation events (green bars) and the collision events (pink bars). The signals at 50 mV bias displayed only one obvious peak and not further segregated. (e–f) Scatter plot of 1-I_B ($=\Delta I/i_0$) versus the dwelling time Δt of all the DNA translocation events (collision events removed) from the SaS nanopore (e) and SiS nanopore (f). The dashed lines at the bottom are the values of I_{RMS}/i_0, in which I_{RMS} is the root-mean-square noise at open-pore state. The short solid lines are the peak values of (1-I_B) in the Gaussian distribution of the translocation events in (b) and (d). The error bars of the distribution are added at the left edge of each short solid line. The SNR for each bias voltage is determined by the ratio between the values of the DNA signals, indicated by the short solid lines, and their corresponding noises, represented by the dashed lines of the same color. The values of SNR are also marked in the figures. DNA data are represented by black, red and blue dots in Fig. a, c, e, and f for the collecting bias voltages as 50 mV, 100 mV, and 150 mV. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

4. Conclusion and outlook

We demonstrated a novel design and manufacturable approach to reproducibly create SaS nanopores featuring triangular membranes with <25 μm dimensions on 2-inch sapphire wafers. Completely eliminating the substrate conductivity-induced stray capacitance, these SaS nanopores convincingly produced two-order-of-magnitude smaller device capacitance (10 pF) compared to a measured SiS nanopore (~1.3 nF), despite having a 100 times larger membrane area. Accordingly, the SaS nanopores generated ~2.6 times smaller RMS ionic current noise than the SiS nanopore at 100 kHz bandwidth, which resulted in high-fidelity DNA sensing with two times higher SNR despite a larger nanopore size and thicker SiN membrane. By analyzing the device capacitance, noise current, and power density spectra of the SaS nanopore and comparing to the best reported SiS and glass-supported nanopores, we found our nanopore chips comparable to the best available low-noise sensors. In this work, the nanopore SNR in DNA sensing is mainly limited by the relatively large nanopore size (~7 nm) and relatively thick membranes (~30 nm). Further optimization in creating smaller nanopores (3–5 nm) and reducing membrane thickness, for example by integration with ultrathin 2D materials (Danda et al., 2017; Graf et al., 2019), is expected to greatly increase the sensitivity and boost the SNR. This low-capacitance SaS membrane is also very favorable to future integration with scalable nanopore formation technologies that require ultrafast feedback from voltage/current signals, such as dielectric breakdown (Kwok et al., 2014) and laser based nanopore drilling (Gilboa et al., 2020; Yamazaki et al., 2018). Additionally, this structurally simple and optically transparent platform makes it attractive for coupling optical spectroscopy and fluorescent molecular imaging with electrical signal readout (Gilboa et al., 2020). The SaS nanopore platform will find use in interrogating a variety of other biomolecules at single-molecule level, such as RNA, protein, and extracellular vesicles, and their molecular interactions at improved speed and accuracy. Beyond nanopores, our demonstrated scalable manufacturing of the membrane architecture on sapphire may

serve to inspire new designs in micro-electromechanical systems (MEMS) and optoelectronic devices.

CRediT authorship contribution statement

Pengkun Xia: Formal analysis, Investigation, Data curation, Writing - original draft. **Jiawei Zuo:** Software, Investigation. **Pravin Paudel:** Investigation. **Shinhyuk Choi:** Investigation. **Xiahui Chen:** Investigation. **Md Ashiqur Rahman Laskar:** Investigation. **Jing Bai:** Investigation. **Weisi Song:** Investigation. **JongOne Im:** Investigation. **Chao Wang:** Conceptualization, Methodology, Resources, Writing - original draft, Writing - review & editing, Supervision, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The authors declare no conflict of interest.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.bios.2020.112829.

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