# SAPPHIRE-SUPPORTED NANOPORES FOR LOW-NOISE DNA SENSING

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## ABSTRACT

Solid-state nanopore sensors have broad applications from single-molecule biosensing to diagnostics and sequencing. Prevalent nanopore sensors are fabricated on silicon (Si) substrates through micromachining, however, the high capacitive noise resulting from Si conductivity has seriously limited both their sensing accuracy and recording speed. A new approach is proposed here for forming nanopore membranes on insulating sapphire wafers by anisotropic wet etching of sapphire through micro-patterned triangular masks. Reproducible formation of small membranes with an average dimension of ~10 μm are demonstrated. For validation, a sapphire-supported (SaS) nanopore chip, with a 100 times larger membrane area than silicon-supported (SiS) nanopore, showed 130 times smaller capacitance (10 pF) and ~2.5 times smaller root-mean-square (RMS) noise current (~20 pA over 100 kHz bandwidth). Tested with 1k bp double-stranded DNA, the SaS nanopore enabled sensing at microsecond speed with a signal-to-noise ratio of 21, compared to 11 from a SiS nanopore. This SaS nanopore presents a manufacturable platform feasible for biosensing as well as a wide variety of MEMS applications.

## KEYWORDS

solid-state nanopores, low noise, low capacitance, signal-to-noise ratio, insulating sapphire substrates, MEMS.

## INTRODUCTION

Solid-state nanopores [1] have attracted considerable interest as a potentially high-speed, portable and low-cost solution for detecting a variety of biomolecules, such as proteins and DNA, as well as studying molecular interactions. However, the design and manufacturing of low-noise nanopore devices currently face a number of limitations. One major challenge in prevalent silicon-supported (SiS) solid-state nanopores is their large device capacitance due to Si conductivity, which introduces a sizeable noise current that becomes particularly acute at high recording frequency, thereby causing serious reading errors (Fig. 1a-c). To minimize the stray capacitance of the Si chip, which is the main component of its device capacitance and can be as large as nano-farad range, conventional techniques introduce a thick insulating material at the nanopore vicinity [2]. However, these fabrication schemes require complex, and manual processing techniques, such as thick dielectric deposition, selective membrane thinning, silicone/photoresist printing, glass bonding, *etc*, and thus are expensive, slow, and difficult to reproduce. Another approach is to replace conductive silicon with an insulating material, such as glass [3]. The amorphous nature of glass substrates, however, prevents the formation of uniform membranes, and involves complex fabrication schemes, such as multiple lithography steps, as well as deposition and etching processes on individual chips.

In this study, we demonstrate a new design concept for creating thin membranes and nanopores on crystalline and insulating sapphire wafers as a means to eliminate stray capacitance from substrate conductance for low-noise biosensing. The method involves creating sapphire-supported (SaS) nanopore membranes by wet and anisotropic etching of 2-inch sapphire wafers in concentrated sulfuric and phosphoric acids, a process similar to bulk alkaline etching of Si that has been widely used in MEMS and biosensing applications. Uniquely, we design a triangular membrane by leveraging the three-fold symmetry of the hexagonal c-plane sapphire lattice and developed a controllable process to produce nanopore membranes over a 2-inch wafer with average size as small as 10.6 μm with 6.8 μm deviation, which corresponds to picofarad level chip capacitance even considering nanometer-thin membranes in high-signal-to-noise-ratio (SNR) DNA detection.

## DICUSSION

### Sapphire Etching with Triangular Window Design

We have devised a new strategy to create suspended dielectric membranes on sapphire wafers by anisotropic wet etching (Fig. 2). Briefly, plasma-enhanced chemical vapor deposition (PECVD)-deposited $SiO_2$ (Fig. 2b) was used here due to its high-selectivity in masking sapphire etching, which we experimentally determined to be over 500:1. Considering the three-fold symmetry of sapphire crystal, we firstly adopted triangular shaped $SiO_2$ etching masks and studied how the alignment angle between such masks and sapphire crystal (denoted α) could affect the membrane evolution (Fig. 2 h-i). The process is similar to alkaline etching of Si but more complex given its hexagonal lattice nature. Interestingly, we found that triangular membranes formed when $0 < \alpha < 20°$ and $40° < \alpha < 60°$, but the two different sets were offset by a rotational angle of ~30° (Fig. 3). In contrast, complex polygon membranes with up to nine sides emerged when $20° < \alpha < 40°$. Additionally, the membrane area was found sensitive to α, yielding an area of more than three orders of magnitude larger when α~30° compared to α~0°. Given that the M- and A- planes of sapphire have very slow etching rates and are perpendicular to the c-plane, they are believed to be less relevant in the observed cavity formation. We instead suspect that the formation of and competition between R- and N-planes of the sapphire crystals are most relevant [4] in the angle-dependent membrane geometry evolution. We also evaluated the square window designs, which is used in Si etching for the

cubic lattice structure; here, we found that they only produced irregular and complex membranes that are much more difficult to control (not shown here).

**Wafer-Scale Micron-Sized Membrane Formation**

To guide the mask layout design, we first performed theoretical calculations to study the relationship between the membrane and the mask dimensions while keeping $\alpha = 0°$. The membrane triangle length $L_2$ could be engineered by the mask triangle length $L_1$ following $L_1 = L_2 + \frac{2\sqrt{3}h}{tan\,\theta}$, where $h$ is the sapphire wafer thickness and $\theta$ is an effective angle between the exposed facets in the cavity and sapphire c-plane that was empirically determined by us to be ~50° for this design. Indeed, by designing $L_1$ from ~750 μm to ~900 μm, we could create $SiO_2$ membranes with size $L_2$ from 5 to 200 μm (not shown). Further, we designed $L_1$ from 760 to 766 μm and $\alpha$~0° for wafer-scale fabrication of <20 μm size membranes, which are most attractive for picofarad sensor capacitance and low-noise biosensing (Fig. 4). Etching two 2-inch sapphire wafers in the same batch, we discovered no wafer or membrane breakage, and successfully obtained 116 suspended micron-sized membranes while having 4 membranes not yet completely etched through (Fig. 4a). We expected further etching would eventually create these 4 membranes while slightly enlarging the existing ones due to slower lateral etching on exposed facets. From intentionally patterned rectangular dicing marks surrounding the cavity etching windows, trenches were formed in sapphire wafers after acid etching, allowing even-hand dicing of 5 mm square chips (Fig. 4b) despite the hexagonal crystal structure of sapphire. Importantly, this wafer-scale demonstration strongly indicated the scalability of our membrane formation process, which is crucial to future large-scale, cost-effective sensor fabrication and novel sapphire based MEMS technologies. Furthermore, we studied the size reproducibility of the small membranes on the two wafers (Fig. 4 c-d). The average size of all membranes was found to be about $L_2 = 12.1$ μm with a standard deviation of 6.7 μm for wafer 1 and $L_2 = 9.2 \pm 6.6$ μm for wafer 2. We found 41 % (48 out of 116) of the membranes were smaller than 10 μm, which corresponds to 2-3 pF chip capacitance even considering nanometer-thin membranes, *e.g.* 2.8 pF, 2.1 pF, and 1.8 pF at 2, 5, and 10 nm thickness. Further, a majority of the membranes (91 %, 105 out of 116) were < 20 μm and all were <25 μm.

In our demonstration, the observed membrane size variation within the wafer could be attributed to a few factors. First, the sapphire wafers were found slightly thinner (~1 μm) at the edge than at the center, which could cause membrane enlargement at the edge. Second, our customized hot-plate based etching apparatus could leave a temperate gradient in the acid bath that could affect the etching rate. Further, acid convection under boiling condition may produce local variation in acid concentration and etching rate. Lastly, the complex evolution of sapphire facets, currently not fully understood but thought to be due to the competition between R- and N-planes of the sapphire crystals, could be sensitive to crystal orientation alignment and the etching bath conditions. In future studies, the membrane uniformity could be improved by compensating etching window sizes over the wafer, utilizing an etching system that provides better temperature control and acid circulation, and further studying the etching mechanism and optimizing the etching window designs.

**SaS Nanopore Noise Characterization**

We have developed a process to create thin silicon nitride (SiN) membranes suitable for nanopore formation and DNA sensing. Briefly, we deposited low-stress low-pressure chemical vapor deposition (LPCVD) SiN film on suspended $SiO_2$ membranes, and then removed the $SiO_2$ film via selective dry etching and hydrofluoric acid (HF) based wet etching from the cavity side (Fig. 2e-f). The use of SiN film allows us to precisely control the membrane thickness and minimizes the impact of $SiO_2$ film stress on the membrane structural integrity. The SiN film can be further thinned down to desired thickness when necessary by either RIE and/or wet etching in hot phosphoric acid.

We characterized the device capacitance of the SaS and SiS nanopore chips. Noticeably, the SaS nanopore chip had a 100 times larger membrane area ($L_2$ = 68 μm, or ~2000 $\mu m^2$ in area) than the SiS chip (4.2 × 4.7 μm square, or ~20 $\mu m^2$) and slightly thicker SiN (measured 30 nm for sapphire and ~23 nm for Si) (Fig. 5a-d). The membrane capacitance $C_m$ was estimated at 3.8 pF for the SaS chip, >70 times greater than that of the SiS chip (0.05 pF), following $C_m = \varepsilon \frac{A}{d}$, where $\varepsilon$ is the permittivity of SiN, and A the membrane area and d membrane thickness. Experimentally, $C_m$ was found ~10 pF for the SaS chip, with a deviation from theoretical value possibly attributed to slightly smaller SiN thickness in reality, and much smaller than that of the SiS chip (~1.3 nF) because of the stray capacitance from Si substrate. Clearly, insulating sapphire successfully eliminates the dominant capacitance resulting from Si substrate conductivity, thus appealing to low-noise measurement.

We further analyzed the ionic current noise for the SaS nanopore, the SiS nanopore, and the open-headstage system (Axopatch 200B) under 10 kHz and 100 kHz low-pass filter (Fig. 5e). The root-mean-square (RMS) of the measured current of the SaS nanopore chip is ~5 and 18 pA using 10 and 100 kHz filters, which is only slightly higher than the open-headstage system RMS noise (3 and 11 pA), and yet much better than those from our SiS nanopores (~16 and 46 pA). In comparison, the best reported silicone-painted SiS chips [2] that utilized a locally thinned membrane (0.25 $\mu m^2$ area and 10-15 nm thick in the center) produced ~7 and ~13 pA noise current at 10kHz and 100kHz, measured by an optimally designed amplifier that outperforms Axopatch 200B in high-frequency recording. One of the best glass chips with nano-membrane (*e.g.* 100 nm diameter, 0.008 $\mu m^2$ in area, and 5-10 pF) measured ~4 and ~13 pA noise current at 10 kHz and 100 kHz, respectively [5]. Glass chips with micro-membranes (25 $\mu m^2$ and 70 pF [6], and 314 $\mu m^2$, ~2 pF [7]) measured ~13 and ~19 pA noise current at 10 kHz bandwidth, which is approximately 3-4 times larger than our SaS chip. The above comparison convincingly shows that our SaS chips are successful in suppressing the noise current and are wholly comparable to the best reported Si- and glass-supported nanopore chips.

**DNA Detection**

To evaluate the performance of DNA molecule detection capability of SaS nanopore, 1k bp ds-DNA were translocated through the SaS and the SiS nanopores at 100 kHz (Fig. 6) low-pass filters under 50 mV, 100 mV, and 150 mV bias, respectively. By comparing representative ionic current traces of 1k bp dsDNA (Fig. 6b), we observed that the DNA signals collected by SiS nanopore displayed severe signal distortion, particularly at lower bias voltages. These irregular signals, together with the high baseline noise, made it very challenging to faithfully distinguish DNA signals from the background. In comparison, the SaS nanopore produced easily distinguishable DNA signals with much less distortion or noise at as high as 100 kHz bandwidth. Additionally, low-frequency recording, *e.g.,* at 10 kHz, would result in serious data loss of fast DNA signals, thus presenting only longer and in some occasions distorted signals [2, 5]. Clearly, SaS nanopores enable high-speed, high-throughput, and high-fidelity detection of DNA signals.

**Fabrication Comparison to Prevalent Low-Noise Sensors**

Noticeably, the state-of-art low-noise SiS and glass chips all require very complicated fabrication processes. For example, the SiS membranes need to be very carefully engineered to reduce the membrane area and introduce thick insulating layers, demanding processes involving nanolithography, bonding, film deposition, etching, and even silicone painting. The key challenge in fabricating glass chips lies in the reproducibility of creating small membranes on glass, because bulk and isotropic etching of amorphous glass in HF has poor dimension control while reactive-ion-etching (RIE) etching is only applicable at single-wafer or single-chip level with drastically lowered throughput and increased manufacturing cost. Although combining femto-second laser ablation with LPVCD and chemical wet etching could form glass chips with a ~2 pF device capacitance [7], it remains unclear how the membrane uniformity (reported variation from 5 to 40 µm), fabrication throughput, and yield are affected by process fluctuation in laser ablation and chemical etching. The wafer-scale SaS chip design and batch processing strategy presents a new scalable alternative to the prevalent manufacturing processes of low-noise sensors that are complicated, time-consuming, low-yield, and costly.

## CONCLUSION

We demonstrated a novel design and manufacturable approach to reproducibly create SaS nanopores featuring triangular membranes with <25 µm dimensions on 2-inch sapphire wafers. Completely eliminating the substrate conductivity-induced stray capacitance, SaS nanopores convincingly produced two-order-of-magnitude smaller device capacitance (10 pF) compared to a measured SiS nanopore (~1.3 nF), despite having a 100 times larger membrane area. Accordingly, the SaS nanopores generated ~2.6 times smaller RMS ionic current noise than the SiS nanopore at 100 kHz bandwidth, which resulted in high-fidelity DNA sensing with two times higher SNR despite a larger nanopore size and thicker SiN membrane. By analyzing the device capacitance, noise current, and power density spectra of the SaS nanopore and comparing to the best reported SiS and glass-supported nanopores, we found our nanopore chips comparable to the best available low-noise sensors. In this work, the nanopore SNR in DNA sensing is mainly limited by the relatively large nanopore size (~ 7 nm) and relatively thick membranes (~30 nm). Further optimization in creating smaller nanopores (3-4 nm) and reducing membrane thickness, for example by integration with ultrathin 2D materials [5], is expected to greatly increase the sensitivity and boost the SNR. This low-capacitance SaS membrane is also very favorable to future integration with scalable nanopore formation technologies that require ultrafast feedback from voltage/current signals, such as dielectric breakdown and laser based nanopore drilling. Additionally, this structurally simple and optically transparent platform makes it attractive for coupling optical spectroscopy and fluorescent molecular imaging with electrical signal readout. The SaS nanopore platform will find use in interrogating a variety of other biomolecules, and their molecular interactions at improved speed and accuracy. Beyond nanopores, our batch-processing compatible and potentially cost-effective manufacturing of the SaS membrane architecture, together with the high mechanical strength, chemical resistivity, high temperature stability, and high optical transparency of sapphire, may serve to establish a new fabrication and design strategy in bulk micromachining of sapphire wafers to broaden the applications in MEMS designs and optoelectronic devices.

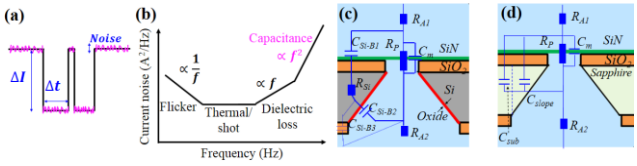


***Figure 1. Design of low-noise nanopores in sapphire****. (a) Hypothetical DNA signals. ΔI is the blockade current, Δt dwelling time. (b) The frequency-dependent current noise components. (c) The equivalent circuit of a SiS nanopore, showing the parasitic capacitance ($C_{Si\text{-}B1}$, $C_{Si\text{-}B2}$ and $C_{Si\text{-}B3}$). (d) The equivalent circuit of a SaS nanopore. Parasitic capacitance is eliminated.*

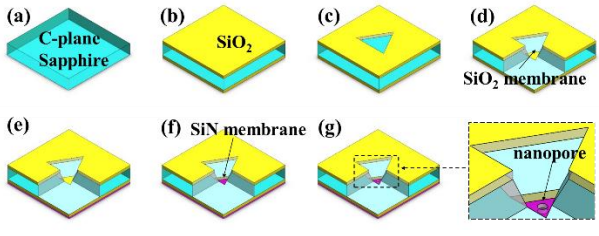


***Figure 2. SaS nanopore fabrication scheme****. (a) A sapphire wafer is RCA2-cleaned. (b) PECVD $SiO_2$ deposited on both sides of the sapphire wafer. (c) A window is formed in the top $SiO_2$. (d) The sapphire is wet etched by hot sulfuric acid and phosphoric acid, forming a suspended $SiO_2$ membrane. (e) A thin LPCVD SiN layer is deposited. (f) The SiN membrane is formed by selectively removing $SiO_2$ in the cavity (and optionally thinning the SiN). (g) A nanopore is drilled by TEM on SiN membrane. One corner is hidden in d-g to show the etching cavity.*

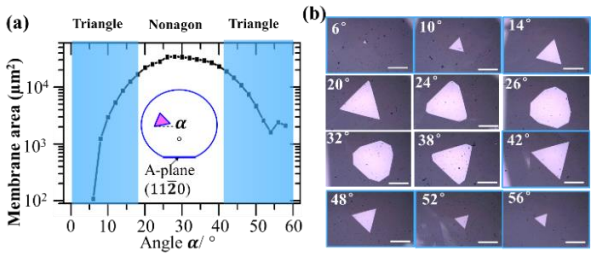


***Figure 3. Experimental data showing the membrane geometry is affected by the alignment offset angle α.*** *(a) Summary of membrane area vs* ***α.*** *(b) Optical images of formed membranes on sapphire as α changes from 2 to 58 degrees. Scale bar: 100 μm.*

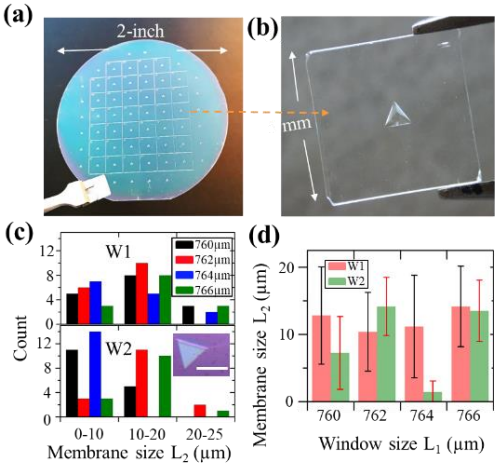


***Figure 4. Ionic current noise analysis.*** *(a) An optical image of a 2-inch sapphire wafer after sapphire being etched through and with intact $SiO_2$ suspended membranes formed. (b) An optical image of a 5 mm by 5 mm sapphire chip diced from a 2-inch wafer. (c) Measurements showing fabricated $SiO_2$ membranes were all smaller than 25 μm on two wafers (W1 and W2). The inset shows a 5 μm $SiO_2$ membrane on wafer 2 (scale bar 5 μm). (d) Average membrane sizes ($L_2$) versus different window sizes ($L_1$) with error bars. Each average value is obtained from measurement of 14 or 16 chips.*

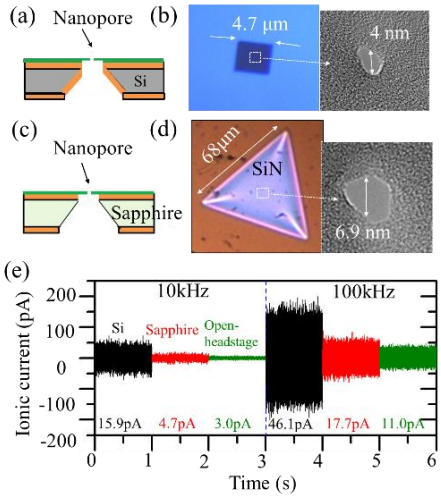


***Figure 5. Ionic current noise analysis.*** *(a-b) SiS Nanopore: (a) cross-sectional schematic, (b) optical image of the membrane and TEM image of nanopore. (c-d) SaS Nanopore: (c) schematic, (d) optical and TEM images. (e) The ionic current noise for the SiS nanopore (black traces), the SaS nanopore (red traces), and the open-headstage state (green traces) under 10 kHz and 100 kHz low-pass filter, respectively. The chips were both measured under 50 mV voltage. The RMS ionic current values were also marked in pA.*

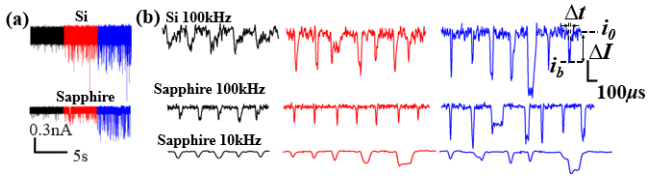


***Figure 6. Analysis of 1k bp dsDNA translocation events.*** *(a) The current traces of the DNA translocation events of the SiS and SaS nanopores under different voltages (black: 50 mV, red: 100 mV, blue: 150 mV). (b) Representative DNA events for the SiS and the SaS nanopores (black: 50 mV, red: 100 mV, blue: 150 mV) and different recording bandwidth (top two rows: 100 kHz, bottom row: 10 kHz). Δt: event dwelling time; $i_0$: open-pore current baseline; $i_b$: block-pore current level; ΔI: blockade current amplitude. The SaS nanopore has a ~2,002 μm² membrane area and the SiS nanopore has ~30 μm² membrane area. The filter was set to 100 kHz.*

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## REFERENCE

[1] C. Dekker, "Solid-state nanopores," *Nature nanotechnology,* vol. 2, p. 209, 2007.

[2] J. K. Rosenstein, M. Wanunu, C. A. Merchant, M. Drndic, and K. L. Shepard, "Integrated nanopore sensing platform with sub-microsecond temporal resolution," *Nature methods,* vol. 9, p. 487, 2012.

[3] A. Balan, C.-C. Chien, R. Engelke, and M. Drndić, "Suspended solid-state membranes on glass chips with sub 1-Pf capacitance for biomolecule sensing applications," *Scientific reports,* vol. 5, p. 17775, 2015.

[4] Y. Xing, Z. Guo, M. A. Gosálvez, G. Wu, and X. Qiu, "Characterization of anisotropic wet etching of single-crystal sapphire," *Sensors and Actuators A: Physical,* p. 111667, 2019.

[5] K.-B. Park, *et al.*, "Noise and sensitivity characteristics of solid-state nanopores with a boron nitride 2-D membrane on a pyrex substrate," *Nanoscale,* vol. 8, pp. 5755-5763, 2016.

[6] M.-H. Lee, *et al.*, "A low-noise solid-state nanopore platform based on a highly insulating substrate," *Scientific reports,* vol. 4, p. 7448, 2014.

[7] L. J. de Vreede, *et al.*, "Wafer-scale fabrication of fused silica chips for low-noise recording of resistive pulses through nanopores," *Nanotechnology,* vol. 30, p. 265301, 2019.

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