

Tuning Supercurrent in Josephson Field-Effect Transistors Using h-BN Dielectric

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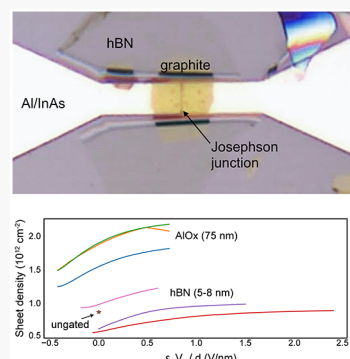
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Supporting Information

ABSTRACT: Epitaxial Al-InAs heterostructures appear as a promising materials platform for exploring mesoscopic and topological superconductivity. A unique property of Josephson junction field effect transistors (JJ-FETs) fabricated on these heterostructures is the ability to tune the supercurrent using a metallic gate. Here, we report the fabrication and measurement of gate-tunable Al-InAs JJ-FETs in which the gate dielectric in contact with the InAs is produced by mechanically exfoliated hexagonal boron nitride (h-BN) followed by dry transfer. We discuss a versatile fabrication process that enables compatibility between layered material transfer and Al-InAs heterostructures that allows us to achieve full gate-tunability of supercurrent by using only 5 nm thick h-BN flakes. Our study shows that pristine properties of epitaxial Josephson junctions, such as product of normal resistance and critical current, $I_c R_n$, are preserved. Furthermore, complementary measurements confirm that using h-BN dielectric changes the channel density less when compared to atomic layer deposition of Al_2O_3 .

KEYWORDS: Josephson junction, two-dimensional materials, hexagonal boron nitride, dielectric, Josephson transistor



Understanding and engineering JJ-FETs fabricated on semiconductors with highly transparent contacts can yield a gate-controllable supercurrent.^{1–9} Tuning the conductivity of the semiconductor part of a JJ-FET affects superconducting properties. For example, JJ-FETs fabricated on Al-InAs have been used for tunable superconducting qubits, the so-called “gatemon”, where the qubit frequency, which depends on the value of the supercurrent, can be tuned in situ with an applied electric field.¹⁰ Furthermore, since InAs has large spin–orbit coupling, the Al-InAs system can host topological superconductivity and Majorana bound states.^{11–13} In this work we discuss a novel fabrication process for gating semiconductor-based JJ-FETs with 2D h-BN dielectric to study their quantum transport properties. This hybrid approach can reduce the unintentional doping of JJ-FETs similar to earlier work in 2D materials using h-BN encapsulation in graphene¹⁴ and MoS_2 devices.¹⁵

JJ-FET devices on III–V materials above the superconducting critical temperature behave practically like a III–V transistor. Historically, performance enhancement of these devices has been achieved through shrinking the gate length of transistors. However, the constant electrostatic scaling rule was not sufficient when the gate lengths of transistors reached the nanoscale. To revive the voltage scaling in order to reduce the power consumption of the integrated circuits, new materials for the gate dielectric were explored. The advent of high- k dielectrics offered one encouraging solution. However, it was

found out that special care had to be taken to produce devices with sufficiently low density of charge traps at the interface of the surface channel and dielectric for reliable device operation. While the standard atomic layer deposition of high- k oxides, e.g., Al_2O_3 , is widely used and optimized, the research for minimizing the trap states on III/V materials continues.^{16–19}

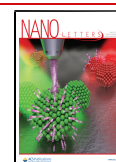
The ability to pick and place an ultrathin insulator flake with no chemical bonding to the InGaAs/InAs channel can minimize the trap states at the interface. In addition small flakes could be very useful when Al_2O_3 lift off is impractical. This can be used for example as a solution for using tunable elements in microwave circuits and Gatemon qubits.^{10,20–22} Among two-dimensional (2D) materials, h-BN, with a bandgap of 5.9 eV, has been widely used as an insulating layer. It has dangling-bond-free surface, low density of charge traps, high surface optical phonon frequency, and low microwave absorption.^{23–27} In this Letter, we integrate h-BN as a gate dielectric for epitaxial Al/InAs JJ-FETs.

The InAs heterostructures are grown on semi-insulating InP (100) substrates using a modified Gen II molecular beam

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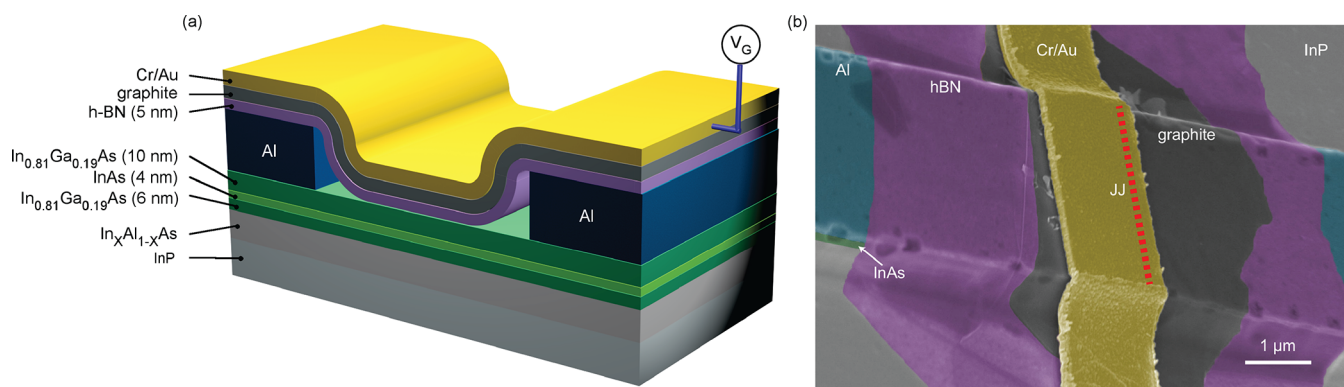


Figure 1. (a) Schematic of the gated JJ-FET geometry. The gate stack comprises a thin layer of h-BN as a gate dielectric with Cr/Au-contacted graphite as the gate electrode. (b) Scanning electron microscopy image of the JJ-FET. The location of the JJ-FET channel is shown by the red dashed line.

epitaxy machine. The step graded buffer layer, $\text{In}_x\text{Al}_{1-x}\text{As}$, is grown at low temperature to minimize dislocations formation due to the lattice mismatch between the active region and the InP substrate.^{28,29} The quantum well consists of a 4 nm layer of InAs grown on a 6 nm layer $\text{In}_{0.81}\text{Ga}_{0.19}\text{As}$. The surface InAs quantum wells have relatively low electron mobilities mostly due to the direct contact of electrons to scattering impurities at the surface. A top InGaAs barrier can improve the situation by separating the quantum well from the Al interface. InGaAs is a suitable choice because it provides a soft confinement, allowing sufficient overlap of electrons with superconductor for proximity effect as well as moving the wave function away from the surface resulting in a mobility increase.³⁰ In this study, 10 nm of $\text{In}_{0.81}\text{Ga}_{0.19}\text{As}$ is grown on an InAs strained quantum well. After the quantum well is grown, the substrate is cooled to below zero centigrade to promote the growth of epitaxial Al (111).³¹

The JJ-FET fabrication process is performed by electron beam lithography using poly(methyl methacrylate) (PMMA) as the resist. Device mesas are defined and etched using Transene type-D Al etchant followed by a III–V etch solution (see the Supporting Information (SI) for additional details). In the active region of the junction, the mesa is 4 μm wide. In a second step, the gap between superconducting contacts of the JJ was patterned by selective etching of Al over InGaAs/InAs using Transene type-D. All presented samples have a gap of ~ 100 nm. To form the gate stack, h-BN and graphite flakes were mechanically exfoliated from bulk crystals onto 90 nm SiO_2/Si substrates at 100 $^\circ\text{C}$ using a heated exfoliation method. Using an optical microscope, we selected appropriate graphite (~ 30 nm) and thin h-BN (~ 6 nm) flakes based on optical contrast and thickness uniformity. The gate stack was then transferred onto the JJ and finally contacted on top by Cr/Au. Figure 1(a) illustrates the JJ-FET schematics from substrate to the gate stack using h-BN. Voltage (V_G) can be applied to the graphite top gate (gray in Figure 1(a)) which controls the carrier density of the InAs surface channel. Figure 1(b) shows a scanning electron microscope image of the JJ-FET device with false color representing the schematic layers.

During initial device fabrication attempts, a stamp made of a thin polycarbonate (PC) film on polydimethylsiloxane (PDMS) was used to construct the graphite/h-BN stack and transfer it onto aluminum contacts. However, the chloroform used to remove the PC after transfer etched the aluminum contacts and destroyed the Al/InAs junctions, likely because of

a small concentration of HCl created in the chloroform by a reaction with oxygen. To eliminate chloroform from the fabrication process, a modified version of this technique was used to create stamps with polypropylene carbonate (PPC), which was dissolved in anisole.

Here, we focus on two JJ-FET devices A and B fabricated on nominally identical heterostructures. The only difference between these two samples is the gate dielectric. In sample A, 6 nm of hBN are used as the gate dielectric while sample B has 50 nm of Al_2O_3 instead. The 2DEGs in these heterostructures were characterized separately by magneto-resistance measurements in van der Pauw geometry. Both samples have a density of $7 \times 10^{11} \text{ cm}^{-2}$. They also have an estimated mean free path l_e of 200 nm. As a consequence with the superconducting electrode gap of $L = 100$ nm both samples are expected to be close to the ballistic regime $L < l_e$. The superconducting gap of the Al was estimated to be about 210 μeV from the critical temperature of the film in both samples ($T_c \sim 1.4$ K). In both samples, the Thouless energy $E_{\text{Thouless}} = \frac{\hbar v_F l_e}{2L^2}$, where v_F is the Fermi velocity and L the gap of the JJ, is larger than 1 meV, which implies that our junctions are in the short limit ($\Delta = E_{\text{Thouless}}$).

Figure 2a shows the differential resistance (dV/dI) versus measured dc bias current as a function of applied top gate voltage at 30 mK. We observed that the critical current remains nearly unchanged above $V_G > 1$ V while it decreases below this value, similar to JJ-FET devices with Al_2O_3 as the gate dielectric.¹ As we tune the gate voltage toward more negative values, the window with zero resistance state (dark blue) becomes narrower and reaches zero at $V_G = -3$ V. Figure 2b shows the differential resistance as a function of bias current extracted from panel (a). The line traces in blue and red are for $V_G = 1$ V and -1.5 V, respectively. The critical current shows an asymmetric behavior that can be associated with the JJ hysteresis (see SI). The critical current is consistently higher on the cold branch where the cold branch goes from zero bias to high bias and corresponds to a lower effective electronic temperature before the transition out of the superconducting state. For example, at $V_G = 1$ V, the critical current exhibits $-2 \mu\text{A}$ on the hot branch and $2.7 \mu\text{A}$ on the cold branch. We observe several peaks and valleys in the region above the critical current. In the Supporting Information, we plot the conductance as a function of the voltage which allows us to interpret those as multiple Andreev reflection processes up to the fourth order.^{32,33} These observations support a highly

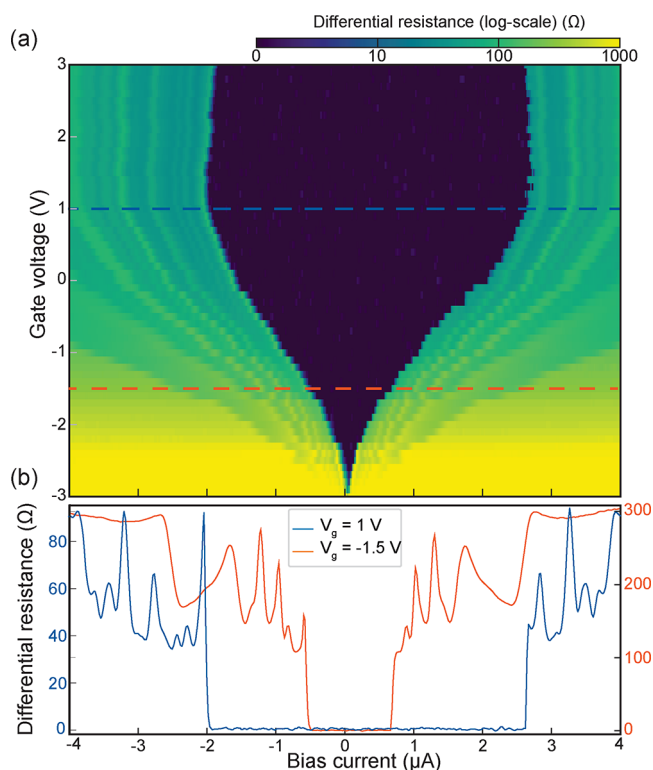


Figure 2. (a) Differential resistance (dV/dI) of the JJ as a function of bias current and gate voltage. (b) Two line traces of panel (a) at $V_G = 1$ and -1.5 V shown in blue and red, respectively.

transparent boundary with the superconducting contacts. In each Andreev reflection, two electrons are transferred across the junction and contribute to the current to drop the resistance, with peaks in resistance corresponding to transitions between successive orders of reflection processes in the high-transparency limit.³² These reflections are observed across the whole range of gate voltages and only disappear around $V_G = -2.5$ V, just above when supercurrent in the JJ ceases, $V_G = -3$ V.

Figure 3a shows the dc transport measurement of voltage versus bias current as a function of top gate voltage. As the gate is used to deplete the 2DEG, by tuning the gate voltage from 3 V toward -2 V (color coded from blue to brown), the voltage increases and the critical current decreases. A figure of merit of JJ devices is considered to be their product of critical current multiplied by their normal state resistance. Theoretically this product is related to the induced superconducting gap and can reach π for a ballistic junction with perfect interfaces.^{34,35} Figure 3b illustrates the gate dependence of the $I_c R_n$ products for sample A. The negative voltage trend is very similar to JJ devices with Al_2O_3 dielectrics.¹ Data presented in the Supporting Information suggests that the induced gap does not vary widely with gate and is close to the parent Al gap, which allows us to evaluate the maximum of the product $I_c R_n / \Delta_{\text{Al}} \sim 1.7$. While we cannot resolve changes in the induced gap, high-order MAR appear to be affected by gate voltage, suggesting that the decrease of the $I_c R_n$ product we observe may be imparted both to the reduced mobility of the 2DEG at low density and to reduced transparency between the gated and Al-covered sections of the 2DEG.

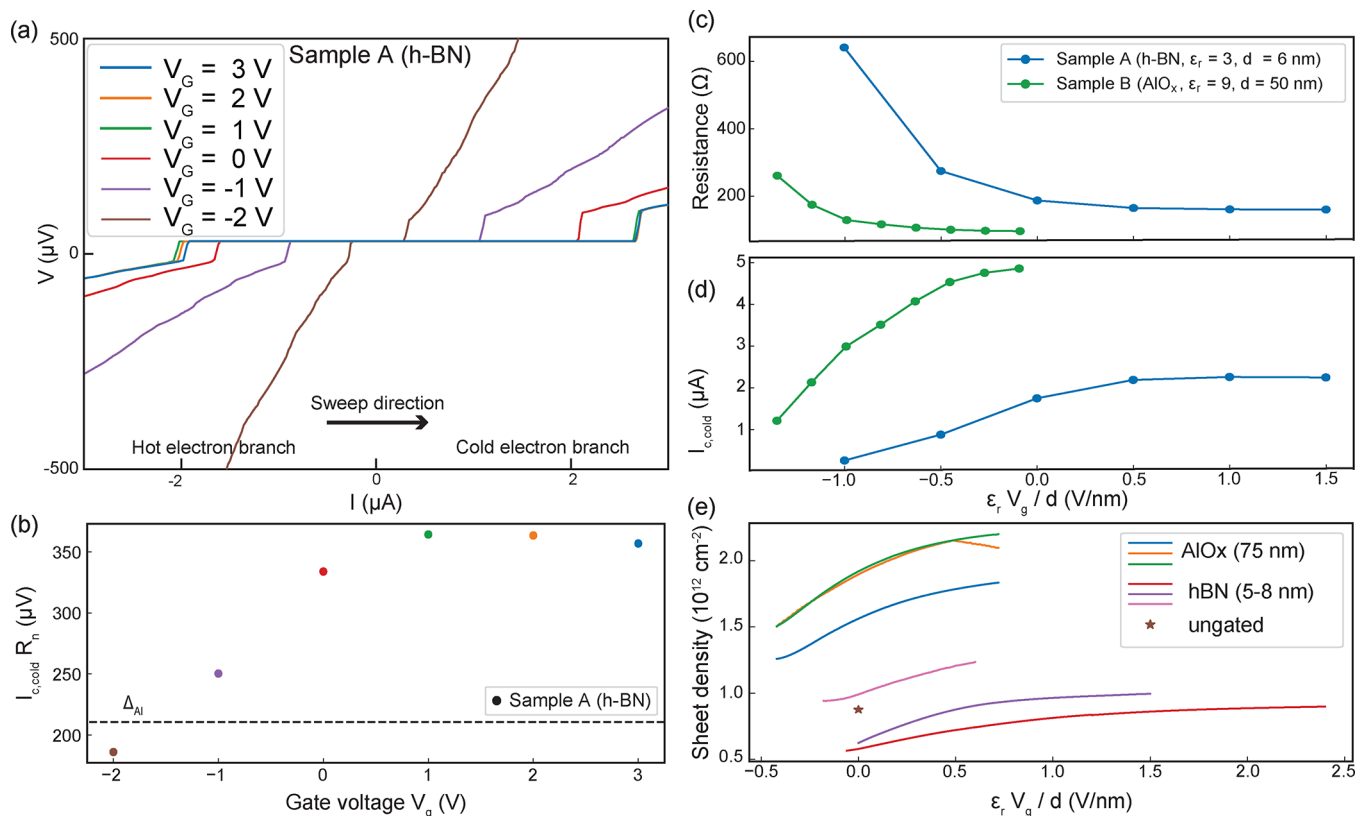


Figure 3. (a) Voltage–current curve as a function of gate voltages from 3 V to -2 V in 1 V steps. (b) $I_{c,\text{cold}} R_n$ as a function of gate voltage for sample A. (c) R_n as a function of gate voltage for sample A with h-BN and sample B with Al_2O_3 dielectrics. (d) $I_{c,\text{cold}}$ as a function of gate voltage for sample A with h-BN and sample B with an Al_2O_3 dielectrics.

For comparison we provide data from sample B with 50 nm of Al_2O_3 dielectric. Figure 3c makes a comparison between gate dependence of normal resistance (at high current bias) of two JJ-FETs with h-BN (sample A) and Al_2O_3 (sample B) dielectric. Sample B shows a smaller normal resistance compared to Sample A, which suggests a higher density for Sample B. The gate efficiency of the device defined by $\delta I_c / \delta V_G$ can also be evaluated by plotting supercurrent as a function of electric displacement field (to normalize for different thicknesses and dielectric constants of h-BN and Al_2O_3) which is shown in Figure 3d. Although the supercurrent is smaller in the h-BN device by a factor of 2, the overall $I_c R_n$ values are closer (within 30%) due to higher R_n . In terms of efficiency while h-BN can be made a few monolayers, the low dielectric constant of h-BN makes the gate efficiency similar to Al_2O_3 . While the curves overall look similar, the shift in the electric field is evident. At zero gate bias, the device with Al_2O_3 dielectric places the curve in saturation (as seen in Figure 3c and d) while the device with h-BN dielectric is away from this region. This could be the result of a higher density in devices with Al_2O_3 dielectric. To test whether Al_2O_3 deposition and h-BN modify the carrier density of 2DEGs, we have made multiple small Hall bars and have deposited Al_2O_3 and transferred larger flakes of h-BN on them. We have described the details of the Hall bar samples in the Supporting Information. The summary of our study is shown in Figure 3e. For reference, we have also added a data point from a Hall bar with no dielectric noted as ungated, which matches another measurement made on an ungated van der Pauw. While there are some variations, devices with Al_2O_3 dielectric show an increase in density compared to the ungated reference sample up to 2-fold. On the other hand, the devices with h-BN dielectric show a smaller density change, some above and some below the reference sample. This confirms our hypothesis that h-BN introduces less doping through interface states compared to Al_2O_3 . This becomes an important factor in the study of device physics and especially in study of topological superconductivity where interfaces play a crucial role.

By applying an external magnetic field to the junction, the critical current of the junction is found to follow a characteristic Fraunhofer pattern. As illustrated in Figure 4 for sample A, the differential resistance oscillates as a function of the out-of-plane magnetic field. The pattern is periodic with a double-width central lobe, which suggests that the current is distributed uniformly in the junction and is not affected by distortion or wrinkles in the h-BN dielectric. We observe a slight increase of the period with the magnetic field which we

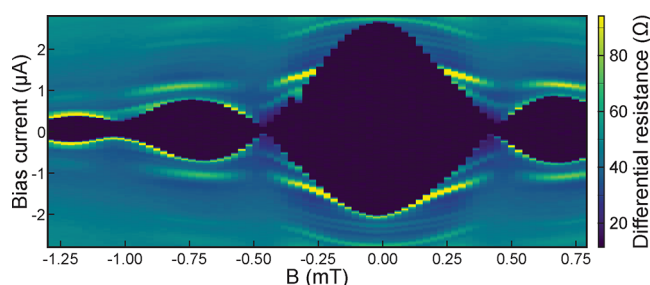


Figure 4. Differential resistance of sample A as a function of the bias current and out-of-plane magnetic field. The critical current presents the typical Fraunhofer pattern of a JJ in the presence of an out-of-plane magnetic field.

attribute to the reduction of the field focusing effect caused by the Al contacts. Similar observations have been reported in ref 36 and can be attributed to the large width of our contacts.

In conclusion, we have demonstrated a versatile fabrication of thin h-BN flakes with Al-InAs JJ-FET with a h-BN/graphite gate stack. These JJ-FET devices with h-BN dielectric exhibit equally pristine Josephson properties when compared to JJ-FET with Al_2O_3 dielectric. Through complementary Hall bar studies we show that while the Al_2O_3 deposition process increases the density of the 2DEG channel the h-BN transfer is introducing less dopants. The small footprint of the process and its flexibility in positioning the flakes together with minimal perturbation of the 2DEG density make these new devices useful for applications in superconducting logic³⁷ and quantum information technologies.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acs.nanolett.0c03183>.

Additional details regarding the fabrication process along with additional measurements supporting our conclusions (PDF)

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Notes

The authors declare no competing financial interest.

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